

**Introduction**

As high speed DACs migrate into digital receivers and transmitters, spectral specifications become more important to the system designer. Specifications like Signal to Noise Ratio (SNR), Total Harmonic Distortion (THD), and Spurious Free Dynamic Range (SFDR) describe the frequency content of the non-ideal converter and how it will operate in a given system. SFDR has become one of the more important specifications that systems designers use to qualify a device for a given design.

**SFDR Definition**

Spurious Free Dynamic Range is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from DC to the full Nyquist bandwidth (half the DAC sampling rate, or  $f_s/2$ ). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. Figure 1 shows how SFDR is measured correctly (SFDR is usually specified in dBc).

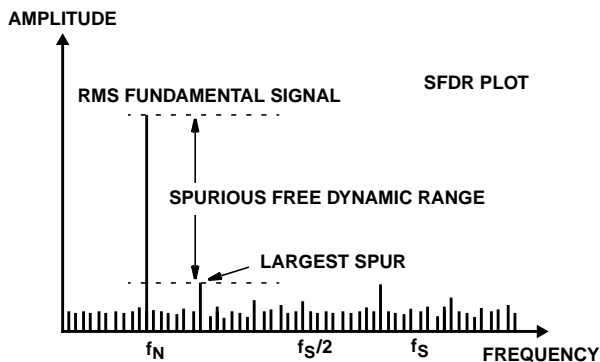


FIGURE 1. MEASURE OF SPURIOUS FREE DYNAMIC RANGE

**The IDEAL Converter**

For a given D/A converter, what should a designer expect for a reasonable SFDR specification? In an ideal system, the worst case Signal to Noise Ratio is calculated by Equation 1:

$$SNR_{IDEAL} = 6.02 (N) + 1.76 \quad (EQ. 1)$$

where N is the number of bits of the converter.

The worst case Signal to Noise Ratio for a 10-bit ideal digital system is -62dB. This is the worst case spurious noise of the system with the assumption that the quantization noise is uniformly distributed. A digital system does not have spurious noise or distortion influencing spectral performance so SFDR equals the worst case Signal to Noise Ratio.

Unlike digital systems, D/A converters have many factors that detract from optimum spectral performance such as total harmonic distortion, non linearity, glitch, power supply noise, board layout, etc. For a D/A converter, the SFDR will always be less than the ideal SNR figure. For example, an SFDR of -58dBc is considered average performance for a real-world 10-bit DAC.

**SFDR Within a Window**

Many manufacturers of high speed converters specify SFDR over a frequency spectrum that is less than the Nyquist bandwidth. By picking an arbitrary window size, the 2nd or 3rd harmonic are often not included in the measurement. Because many systems designers intend to use a narrow band pass filter around the fundamental signal, they are more interested in the spectral performance within a band that the filter will pass. However, having full knowledge of a DAC's spectral performance is essential to the selection of an appropriate band pass filter to remove the harmonics.

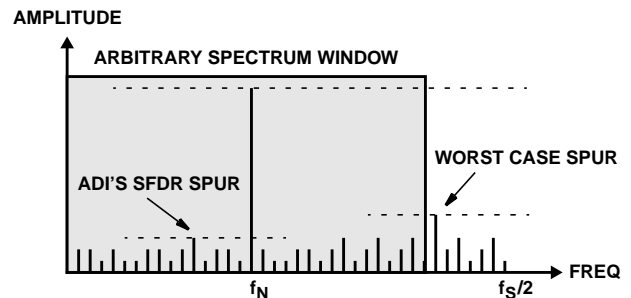


FIGURE 2. COMPETITORS SFDR

Figure 2 shows the method used by some DAC suppliers to measure SFDR. Utilizing this method, the fundamental frequency of  $f_N$  and the span used to measure SFDR does not include the 2nd harmonic.

So what is valid for a true SFDR specification? The answer is both methods have merit and should be considered. A systems designer needs to know the full spectral performance of a given DAC up to the Nyquist bandwidth. The best way to show a DAC's actual performance is with a typical performance curve, showing spurs and spectral performance up to Nyquist. Curves, showing the arbitrary windows used by some DAC suppliers, are also of interest to many designers.

Figure 3 shows a typical performance plot of the Intersil HI5721 10-bit DAC from DC to the full Nyquist bandwidth. Testing was performed with a 100MHz sample clock yielding a Nyquist bandwidth of 50MHz. The fundamental signal is sited at 5.0MHz and is attenuated by 20dB. The SFDR under these conditions was measured at -64dBc. The second harmonic is the only in-Nyquist band harmonic.

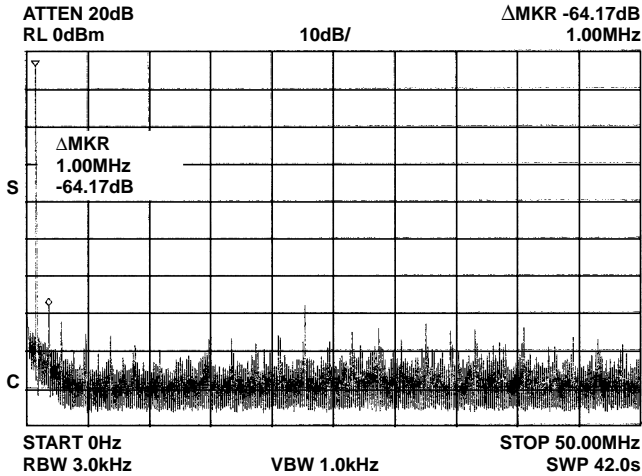


FIGURE 3. SFDR TO NYQUIST

Figure 4 shows a typical performance plot of the HI5721's SFDR within a window span of 5MHz. You will notice that all of the harmonically related spurs are outside this window. In this span the noise floor is down -81dBc.

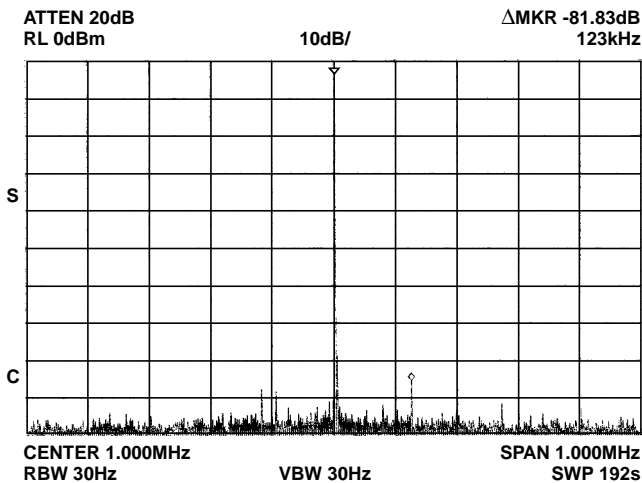


FIGURE 4. SFDR WITHIN A 1MHz SPAN

### How to Improve SFDR

SFDR is directly related to linearity and glitch performance of a DAC. The quantization noise of the converter (i.e., the number of bits) the converter can accurately represent will limit the overall dynamic range.

Glitch is a broad spectral event that has spurs throughout the Nyquist band starting at DC and continues up through the sampling frequency. Eliminating glitch is a difficult task at best. Designers can simplify their system design, by choosing a low-glitch DAC like the HI5721.

Other ways to improve SFDR are to slow down data and clock edge rates. A 50Ω shunt termination resistor on the clock line reduces the clock step size and provides proper termination. Since any noise on the clock line will degrade the DAC's performance dramatically, make clock lines as short as possible, and use proper termination.

Bypassing the converter is another method to improve overall SFDR performance in a DAC. A 0.01μF capacitor paralleled with a 0.1μF capacitor on all power supply pins provides the best decoupling and noise reduction solution. Surface mount components give the best results since they have less lead inductance and stray capacitance.

### Summary

The Spurious Free Dynamic Range of a D/A converter needs to be specified over the full Nyquist bandwidth as well as over the band of interest for a given application. Only this way can a system designer obtain a complete picture of the converter's spectral performance and determine its impact to their system's performance. Selecting a low glitch, linear converter helps to significantly reduce spurs. Proper board layout and termination rules must be followed so as not to introduce undue system noise into the DAC. The HI5721 was designed to provide superior SFDR performance over the full Nyquist bandwidth and is one of the highest performance 10-bit DACs available today.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### Sales Office Headquarters

**NORTH AMERICA**  
Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (321) 724-7000  
FAX: (321) 724-7240

**EUROPE**  
Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

**ASIA**  
Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029