RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A149A/E	Rev.	1.00
Title	Additions and corrections to descriptions of the I/O ports and electrical characteristics in the RX113 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX113 Group	Lot No. All	Reference Document	RX113 Group User's Manual: Hardware Rev.1.02 (R01UH0448EJ0102)		

This document describes additions and corrections to descriptions of the I/O ports and electrical characteristics in the RX113 Group User's Manual: Hardware.

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Handling of unused pins in Table 18.5 is modified as follows.

Before correction

Table 18.5 Handling of Unused Pins

Pin Name	Description
	(Omitted)
Port 0 to 3, 5, 9, A to F, H, J (for pins that exist on products with fewer than 100 pins)	・Set these pins to input (PORTn.PDR.bit = 0) and connect each of them to VCC via a pull-up resister or to VSS via a pull-down resister.*1 ・Set these pins to output (PORTn.PDR.bit = 1), set the output data to 0 (PORTn.PODR.bit = 0) and leave them open.*1, *2
Port 4 (for pins that exist on products with fewer than 100 pins)	・Set these pins to input (PORTn.PDR.bit=0) and connect each of them to AVCC0 via a pull-up resister or to AVSS0 via a pull-down resister.*1
Port 0 to 5, 9, A to F, H, J (for pins that do not exist on products with fewer than 100 pins)	・Set these pins to output (PORTn.PDR.bit = 1), set the output data to 0 (PORTn.PODR.bit = 0) and leave them open.*1, *2
	(Omitted)

After correction

Table 18.5 Handling of Unused Pins

Pin Name	Description
	(Omitted)
VCC_USB	Connect this pin to VCC
VSS_USB	Connect this pin to VSS
Ports 0 to 3, 5, A to F, H, and J (PJ0, PJ2, PJ3)	・Set these pins to input (the PORTn.PDR bit = 0) and connect each of them to VCC via a pull-up resistor or to VSS via a pull-down resistor.*1 ・Set these pins to output (the PORTn.PDR bit = 1), set the output data to 0 (the PORTn.PODR bit = 0) and leave the pins open. *1, *2
Port 4, 9, J (PJ6, PJ7)	・Set these pins to input (the PORTn.PDR bit = 0) and connect each of them to AVCC0 via a pull-up resistor or to AVSS0 via a pull-down resistor. *1 ・Set these pins to output (the PORTn.PDR bit = 1), set the output data to 0 (the PORTn.PODR bit = 0) and leave the pins open.*1, *2
Ports 0 to 5, 9, A to F, H, and J (PJ3) (for pins that do not exist on products with fewer than 64 pins)	・Set these pins to output (the PORTn.PDR bit = 1), set the output data to 0 (the PORTn.PODR bit = 0) and leave the pins open. *1, *2 (Refer to section 18.4, Initialization of Port Direction Resister (PDR).)
	(Omitted)
AVCC0	Connect this pin to VCC when not using the 12-bit A/D converter or D/A converter
AVSS0	Connect this pin to VSS when not using the 12-bit A/D converter or D/A converter

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The row of input voltage in Table 42.1 Absolute Maximum Ratings is modified as follows.

Before correction

Table 42.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
(omitted)			
Input voltage (except for ports 5V tolerant*1)	V_{in}	-0.3 to VCC +0.3	V
Input voltage (ports 5V tolerant*1)	V_{in}	-0.3 to +6.5	V
(omitted)			

After correction

Table 42.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
(omitted)				
Input voltage	Ports 5V tolerant*1	V_{in}	-0.3 to +6.5	V
	Ports P40 to P44, P46, P90 to P92, PJ6, and PJ7	V_{in}	-0.3 to AVCC0 + 0.3	V
	Ports other than the above	V_{in}	-0.3 to VCC + 0.3	V
(omitted)				

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The note of caution regarding 5V tolerant is modified as follows.

Before correction

Caution

(omitted)

Note 1. Ports 16, 17, A6 and B0 are 5V tolerant.

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and abnormal current that passes in the device at this time may cause degradation of internal elements.

After correction

Caution

(omitted)

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and abnormal current that passes in the device at this time may cause degradation of internal elements.If input voltage (within the specified range from -0.3 to + 6.5V) is applied to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 16, 17, A6 and B0 are 5V tolerant.

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The row of the analog power supply voltages in Table 42.2 Recommended Operating Conditions is modified as follows.

Before correction

Table 42.2 Recommended Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
(omitted)						
Analog power supply voltages	AVCC0*1 to *3		1.8	-	3.6	V
	AVSS0		-	0	-	V

After correction

Table 42.2 Recommended Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
(omitted)						
Analog power supply voltages	AVCC0*1 to *3		1.8	-	3.6	V
	AVSS0		-	0	-	
	VREFH0		1.8	-	AVCC0	
	VREFL0		-	0	-	
	VREFH		1.8	-	AVCC0	
	VREFL		-	0	-	

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Increment for LPT operation and increment for IWDT operation are added to Table 42.8. DC Characteristics (6) as follows.

Before correction

Table 42.8 DC Characteristics (6)

Item		Symbol	Typ. *3	Max.	Unit	Test Conditions
(omitted)						
Supply Current *1	Increment for RTC operation *4	I_{CC}	0.31	-	μA	RCR3.RTCDV[2:0] = 010b
			1.09	-		RCR3.RTCDV[2:0] = 100b

After correction

Table 42.8 DC Characteristics (6)

Item		Symbol	Typ. *3	Max.	Unit	Test Condition
(omitted)						
Supply Current *1	Increment for RTC operation *4	I_{CC}	0.31	-	μA	RCR3.RTCDV[2:0] = 010b
			1.09	-		RCR3.RTCDV[2:0] = 100b
	Increment for LPT operation		0.37	-		The LPTCR1.LPCNTCKSEL bit is 1 when the IWDT dedicated on-chip oscillator is selected
	Increment for IWDT operation		0.37	-		

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Operating current for LVD1, LVD2 and CTSU are added to Table 42.11. DC Characteristics (9) as follows.

Before correction

Table 42.11 DC Characteristics (9)

Item		Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
(omitted)							
Temperature sensor*6		I_{TEMP}	-	75	-	µA	
(omitted)							

After correction

Table 42.11 DC Characteristics (9)

Item		Symbol	Min.	Typ.*7	Max.	Unit	Test Condition
(omitted)							
LVD1, LVD2	Per channel	I_{LVD}	-	0.15	-	µA	
Temperature sensor*6		I_{TEMP}	-	75	-	µA	
(omitted)							
CTSU operating current	During measurement (CPU is in sleep mode) Base clock: 2 MHz Pin capacity: 50 pF	I_{CTSU}	-	150	-	µA	
(omitted)							

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Output voltage range and conditions in Table 42.43 D/A Conversion Characteristics (1) are modified as follows.

Before correction

Table 42.43 D/A Conversion Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 1.8 to 3.6V, VSS = AVSS0 = VREFL = VSS_USB = 0V
Ta = -40 to +105°C
Reference voltage = VREFH or VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Condition
(omitted)					
Output voltage range*1	0.35	-	AVCC0-0.47	V	
(omitted)					

After correction

Table 42.43 D/A Conversion Characteristics (1)

Conditions: 1.8V ≤ VCC = VCC_USB ≤ 3.6V, 1.8V ≤ AVCC0 ≤ 3.6V, 1.8V ≤ VREFH ≤ AVCC0, VSS = AVSS0 = VREFL = VSS_USB = 0V、Ta = -40 to +105°C
Reference voltage = VREFH and VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Condition
(omitted)					
Output voltage range*1	0.35	-	AVCC0-0.47	V	AVCC0-0.47V < VREFH
	0.35	-	VREFH	V	VREFH ≤ AVCC0 - 0.47V
(omitted)					

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