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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0281A/E	Rev.	1.00
Title	Errata Regarding Setting of the RCR4.RCKSEL Bit for the RX671 Group MCU		Information Category	Technical Notification		
Applicable Product	RX671 Group	Lot No.	Reference Document	RX671 Group User's Manual: Hardware Rev.1.10 (R01UH0899EJ0110)		
		All				

This document describes corrections to the flowcharts in section 9.10.6, Notes on Sub-Clock Oscillator, section 31.3.2, Clock and Count Mode Setting Procedure, and section 31.6.8, Initialization Procedure When the Realtime Clock is Not to be Used in RX671 Group User's Manual: Hardware.

• Purpose of Corrections

The procedure for setting the sub-clock is described in parts of both sections 9 and 31: section 9.10.6, Notes on Sub-clock Oscillator, section 31.3.2, Clock and Count Mode Setting Procedure, and section 31.6.8, Initialization Procedure When the Realtime Clock is Not to be Used. Although writing to the RCR4.RCKSEL bit should only proceed once, a value is set in the bit in the flowcharts in each of the sections stated above.

For this reason, setting of the RCR4.RCKSEL bit should only proceed in accord with the flowchart from the Realtime Clock section and the step should be omitted from the sub-clock setting procedures.

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The following deletions are made in Figure 9.15, Example Flowchart of Initialization when the Sub-Clock is to be Used as the Source to Drive Counting by the Realtime Clock.

- The RCR4.RCKSEL bit setting
- Note 2

The title of Figure 9.15 is also modified.
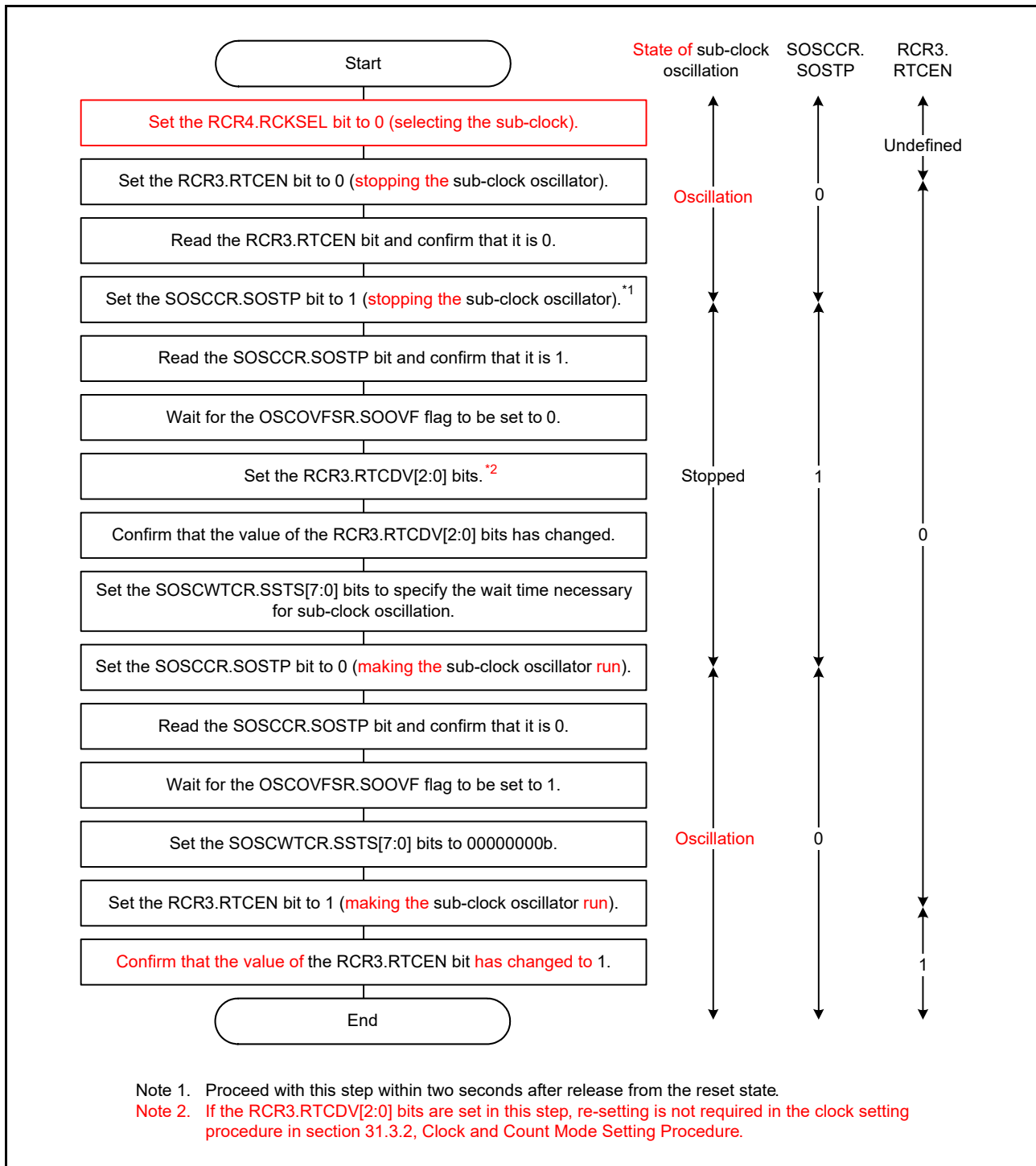
Before correction

Figure 9.15   **Example Flowchart of Initialization when the Sub-Clock is to be Used as the Source to Drive Counting by the Realtime Clock**

After correction

| | Sub-clock oscillation state | SOSCCR. SOSTP | RCR3. RTCEN |

Start

Set the RCR3.RTCEN bit to 0 (sub-clock oscillator is stopped).

Read the RCR3.RTCEN bit and confirm that it is 0.

Set the SOSCCR.SOSTP bit to 1 (sub-clock oscillator is stopped). [*1]

Read the SOSCCR.SOSTP bit and confirm that it is 1.

Wait for the OSCOVFSR.SOOVF flag to be set to 0.

Set the RCR3.RTCDV[2:0] bits.

Confirm that the value of the RCR3.RTCDV[2:0] bits has changed.

Set the SOSCWTCR.SSTS[7:0] bits to specify the wait time necessary for sub-clock oscillation.

Set the SOSCCR.SOSTP bit to 0 (sub-clock oscillator is operating).

Read the SOSCCR.SOSTP bit and confirm that it is 0.

Wait for the OSCOVFSR.SOOVF flag to be set to 1.

Set the SOSCWTCR.SSTS[7:0] bits to 00000000b.

Set the RCR3.RTCEN bit to 1 (sub-clock oscillator is operating).

Read the RCR3.RTCEN bit and confirm that it is 1.

End

Column states (right side annotations):
- RCR3.RTCEN: Undefined → 0 → 1
- Sub-clock oscillation state: Oscillating → Stopped → Oscillating
- SOSCCR.SOSTP: 0 → 1 → 0

Note 1.   Proceed with this step within two seconds after release from the reset state.

Figure 9.15   Example of Initialization Flowchart for Running the Sub-Clock in Software Standby Mode and Deep Software Standby Mode

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The following deletions are made in Figure 9.16, Example Flowchart for Initialization when the Sub-Clock is to be Used only as the System Clock.

- The RCR4.RCKSEL bit setting
- Note 2

The title of Figure 9.16 is also modified.

<u>Before correction</u>
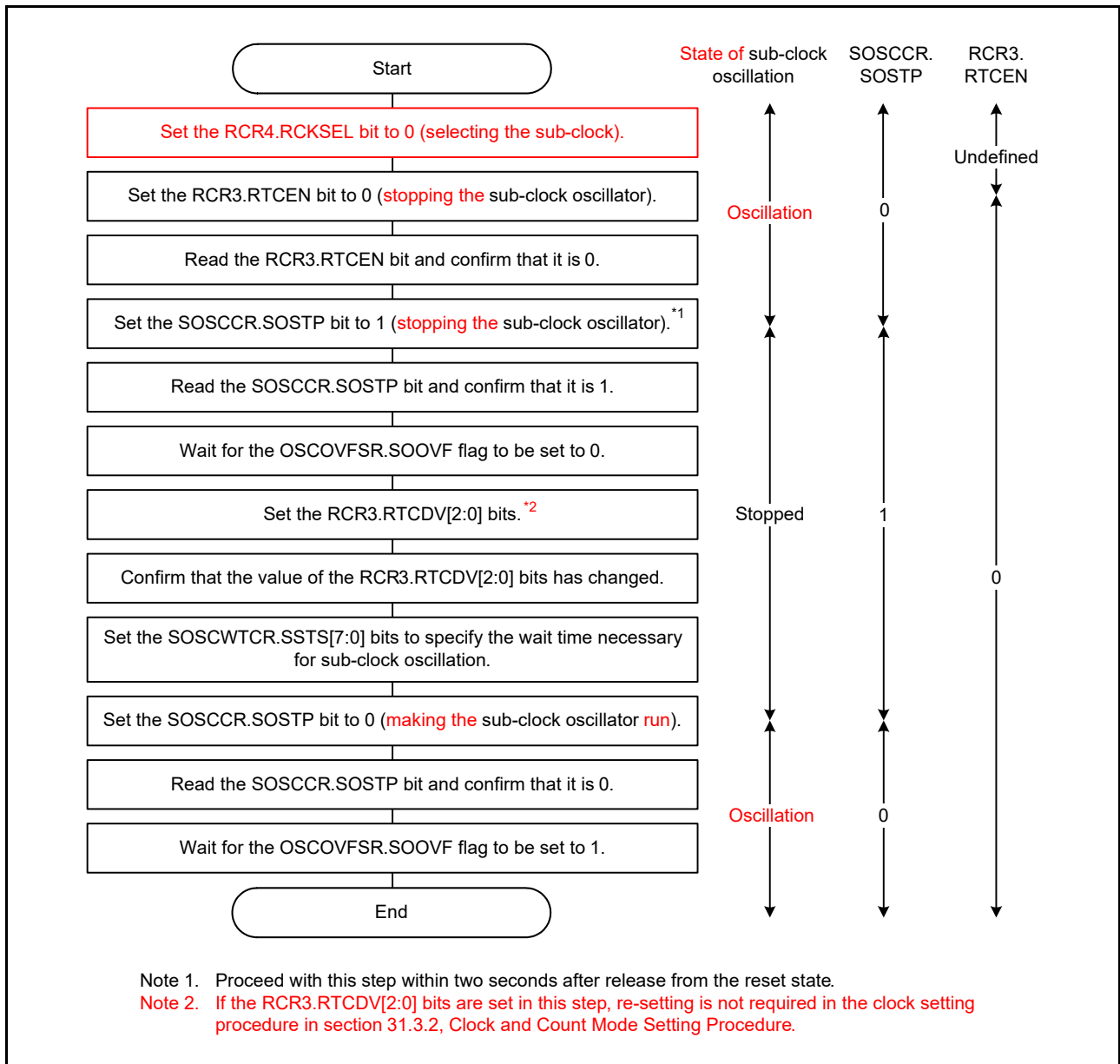
Figure 9.16   Example Flowchart for Initialization when the Sub-Clock is to be Used only as the System Clock
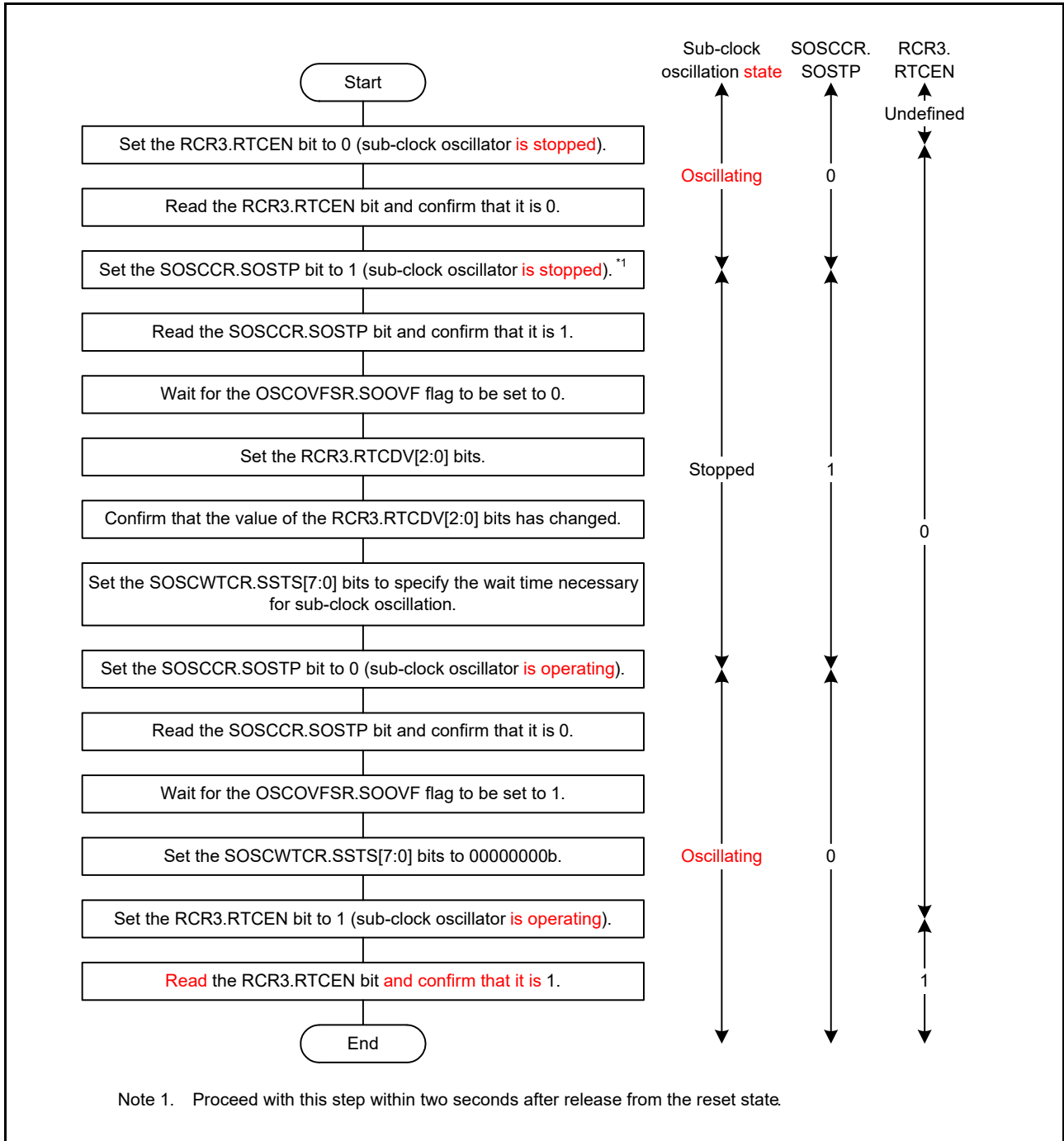
After correction
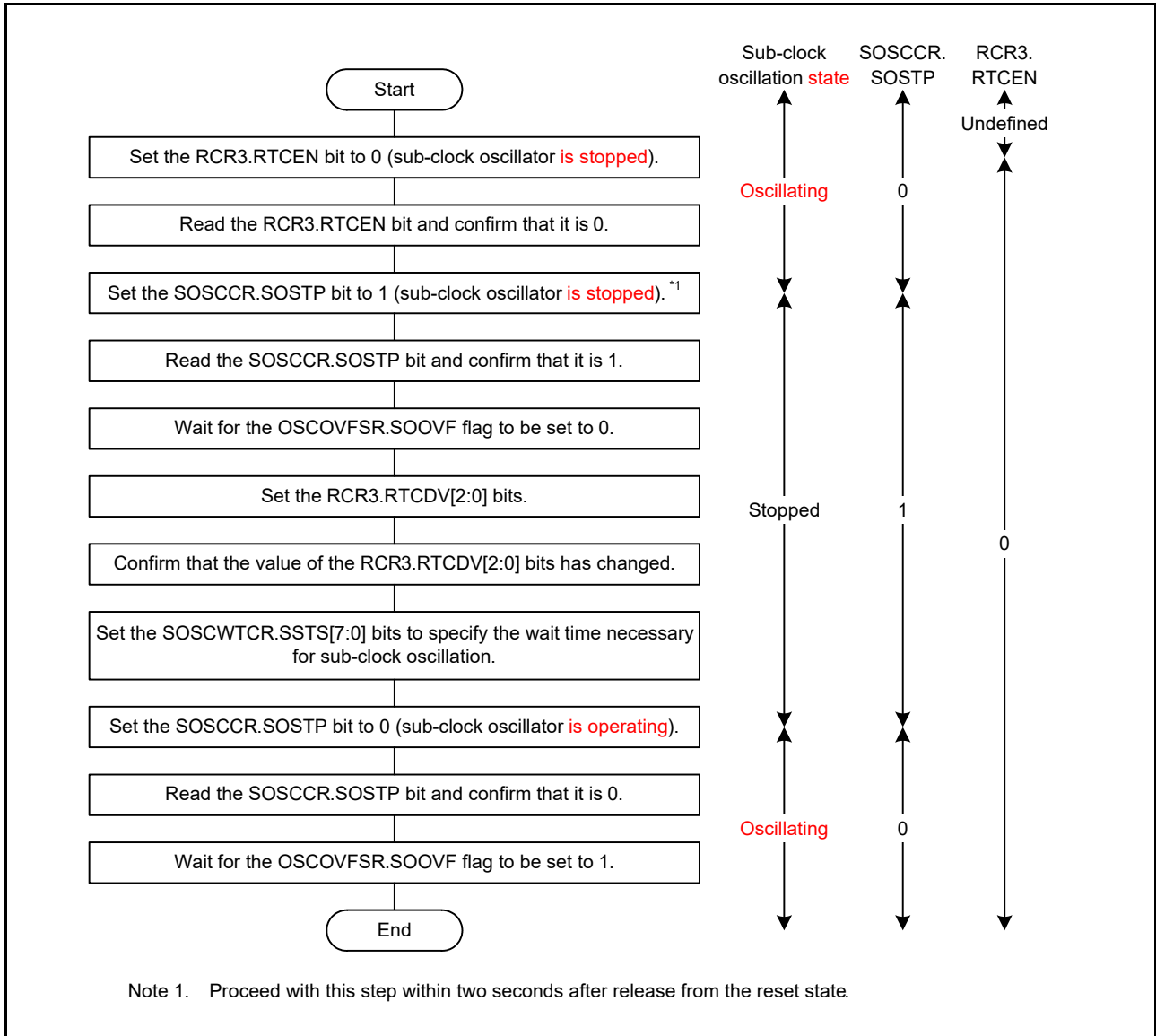
Figure 9.16   Example of Initialization Flowchart for Stopping the Sub-Clock in Software Standby Mode and Deep Software Standby Mode

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The following deletion is made in Figure 9.17, Example Flowchart for when the Sub-Clock is not to be Used.

- The RCR4.RCKSEL bit setting

<u>Before correction</u>
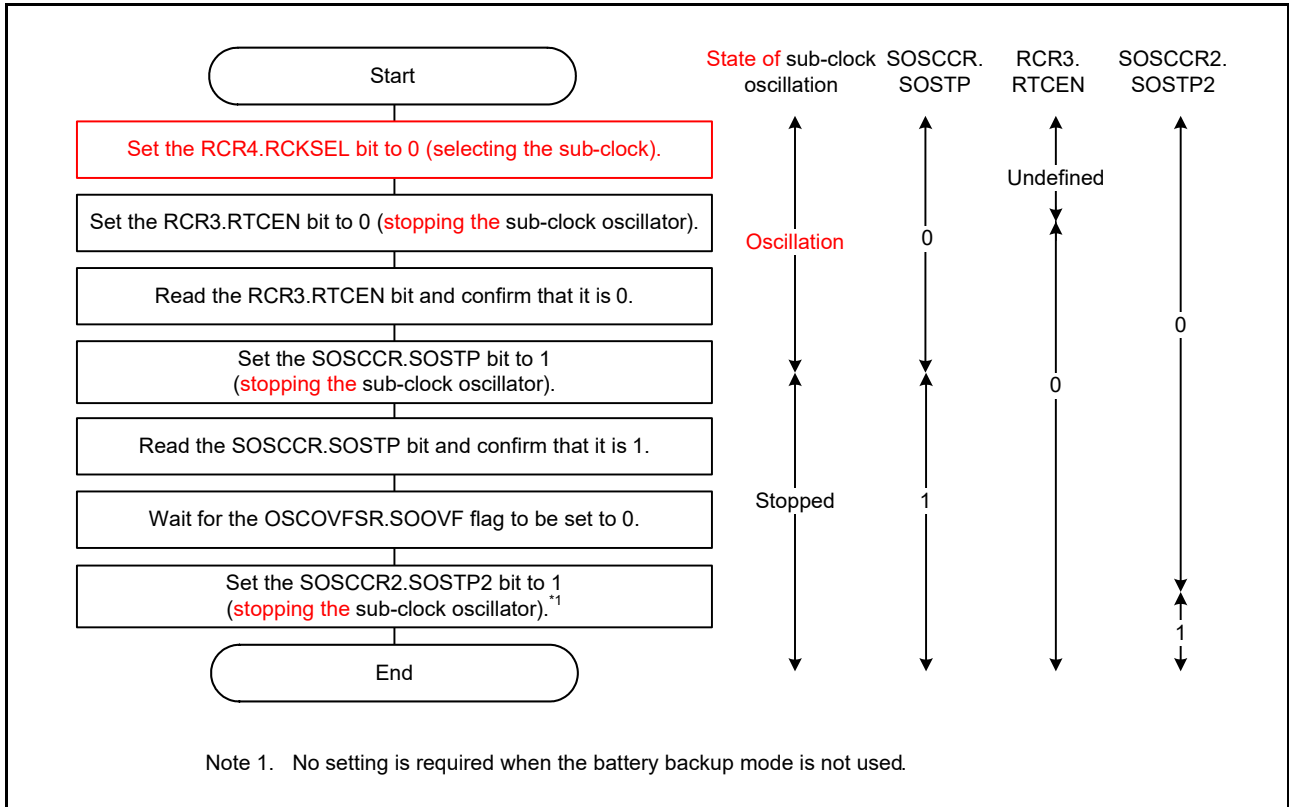
Figure 9.17   Example Flowchart for when the Sub-Clock is not to be Used

After correction
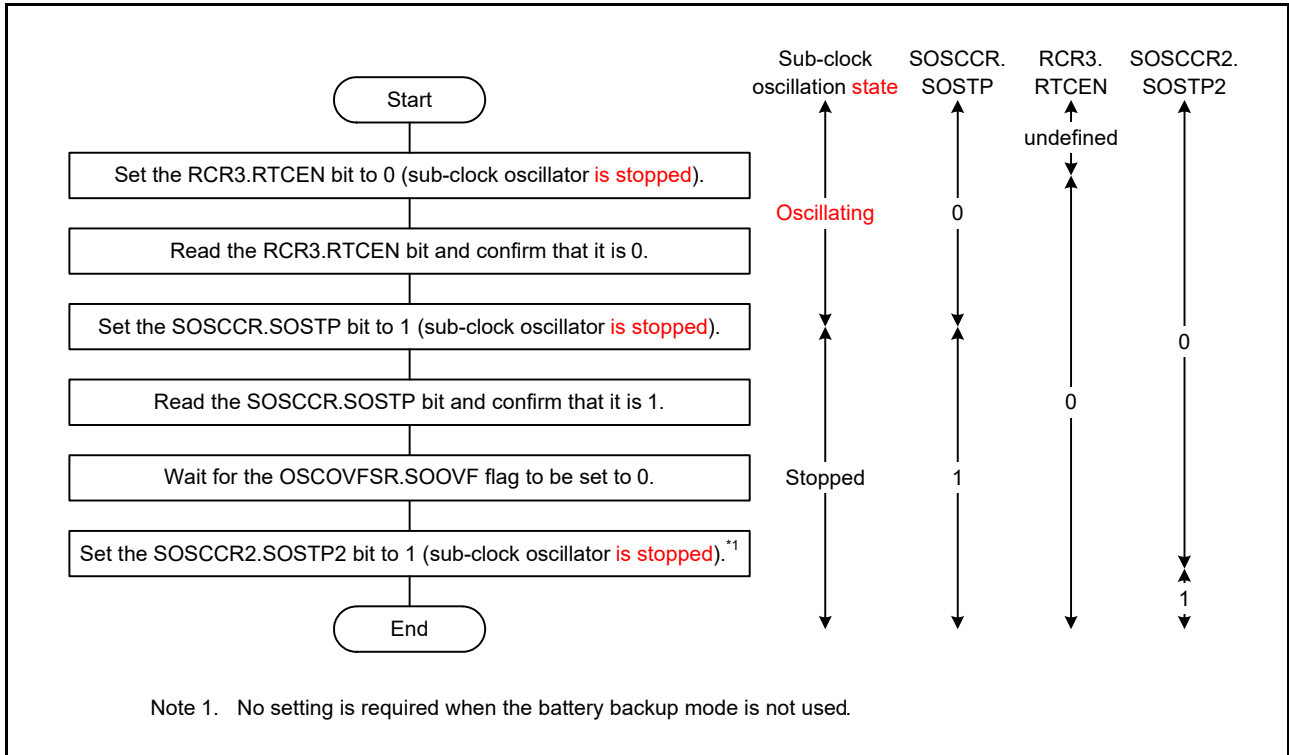
Figure 9.17   Example of Initialization Flowchart When the Sub-Clock Is Not to Be Used

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Figure 31.3, Clock and Count Mode Setting Procedure, in section 31.3.2, Clock and Count Mode Setting Procedure, is separated into two flowcharts as follows to suit the clock that is in use.
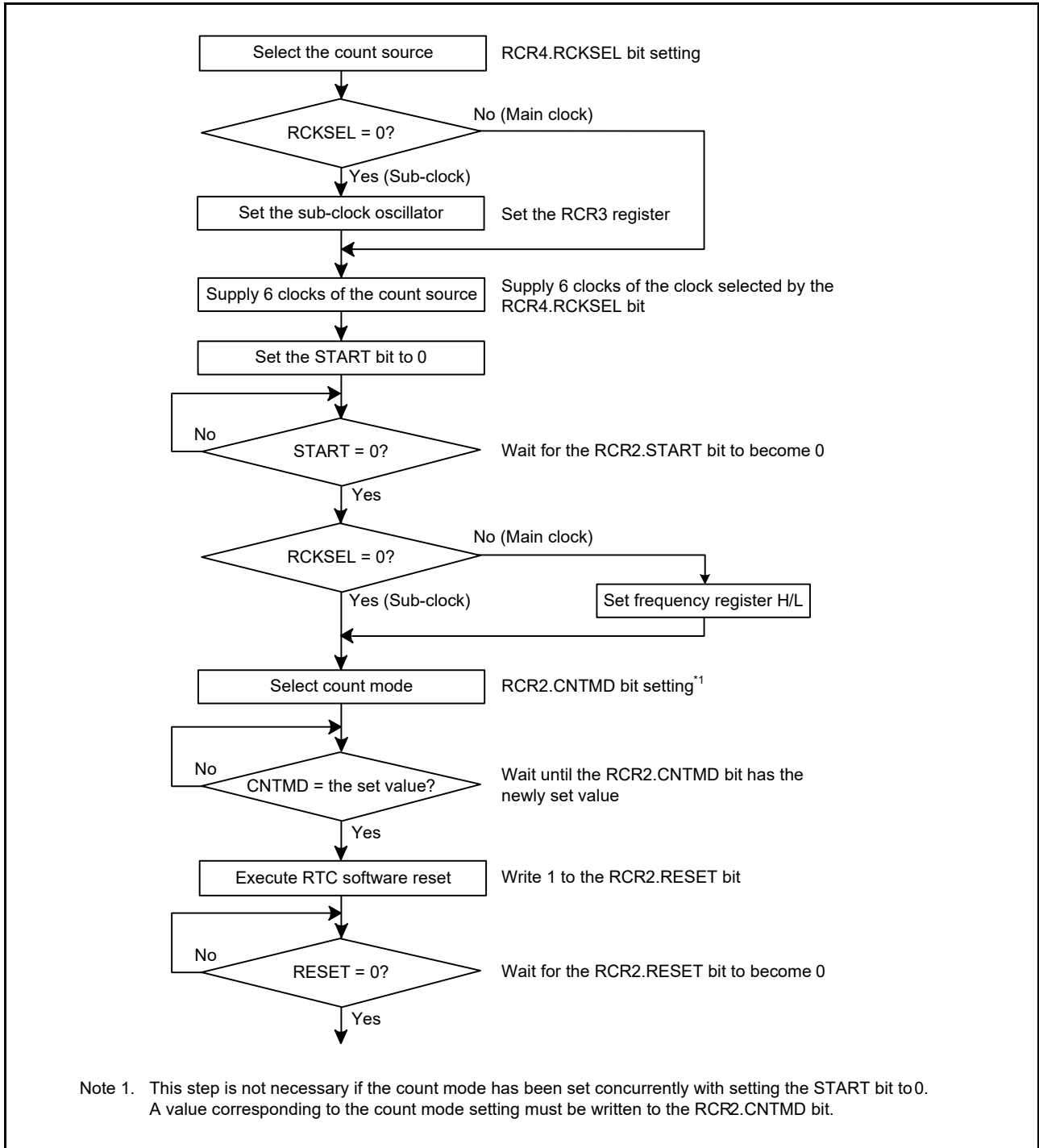
Before correction

Figure 31.3   Clock and Count Mode Setting Procedure

After correction

Start

RCR4.RCKSEL bit = 1 — Select main clock as the clock source[1]

Supply 6 clocks of the main clock

RCR2.START bit = 0

RCR2.START bit = 0? — No / Yes — Wait for the RCR2.START bit to become 0

Set the RFRH and RFRL registers

Select count mode — RCR2.CNTMD bit setting[2]

RCR2.CNTMD bit = the set value? — No / Yes — Wait until the RCR2.CNTMD bit has the newly set value

Execute RTC software reset — Write 1 to the RCR2.RESET bit

RCR2.RESET bit = 0? — No / Yes — Wait for the RCR2.RESET bit to become 0

End

Note 1. Only write to the RCR4.RCKSEL bit at this point in the flow.
Note 2. This step is not necessary if the count mode has been set concurrently with setting the RCR2.START bit to 0.
A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Figure 31.3   Clock and Count Mode Setting Procedure (When Using Main Clock)

```
                              ┌─────────────┐
                              │    Start    │
                              └─────────────┘
                                     │
                    ┌────────────────────────────────┐
                    │      RCR4.RCKSEL bit = 0        │      Select sub-clock as the clock source*1
                    └────────────────────────────────┘
                                     │
                    ┌────────────────────────────────┐
                    │   Set the sub-clock oscillator*2│      Set the SOSCCR, RCR3, and SOSCWTCR registers
                    └────────────────────────────────┘
                                     │
                    ┌────────────────────────────────┐
                    │   Supply 6 clocks of the sub-clock │
                    └────────────────────────────────┘
                                     │
                    ┌────────────────────────────────┐
                    │      RCR2.START bit = 0         │
                    └────────────────────────────────┘
                                     │
          No         ◇────────────────────────────◇
         ┌───────────│      RCR2.START bit = 0?     │      Wait for the RCR2.START bit to become 0
         │           ◇────────────────────────────◇
         │                        │ Yes
                    ┌────────────────────────────────┐
                    │      Select count mode         │      RCR2.CNTMD bit setting*3
                    └────────────────────────────────┘
                                     │
          No         ◇────────────────────────────◇
         ┌───────────│    RCR2.CNTMD bit            │      Wait until the RCR2.CNTMD bit has the newly set value
         │           │    = the set value?          │
         │           ◇────────────────────────────◇
         │                        │ Yes
                    ┌────────────────────────────────┐
                    │   Execute RTC software reset   │      Write 1 to the RCR2.RESET bit
                    └────────────────────────────────┘
                                     │
          No         ◇────────────────────────────◇
         ┌───────────│     RCR2.RESET bit = 0?      │      Wait for the RCR2.RESET bit to become 0
         │           ◇────────────────────────────◇
         │                        │ Yes
                              ┌─────────────┐
                              │     End     │
                              └─────────────┘
```

Note 1. Only write to the RCR4.RCKSEL bit at this point in the flow.
Note 2. For the procedure for setting up a sub-clock oscillator, refer to section 9, Clock Generation Circuit.
Note 3. This step is not necessary if the count mode has been set concurrently with setting the RCR2.START bit to 0.
         A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Figure 31.4   Clock and Count Mode Setting Procedure (When Using Sub-Clock)

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Figure 31.14, Initialization Procedure, in section 31.6.8, Initialization Procedure When the Realtime Clock is Not to be Used, is separated into two flowcharts as follows to suit the clock that is in use. A step of clearing the interrupt status flags is also added to both flowcharts.
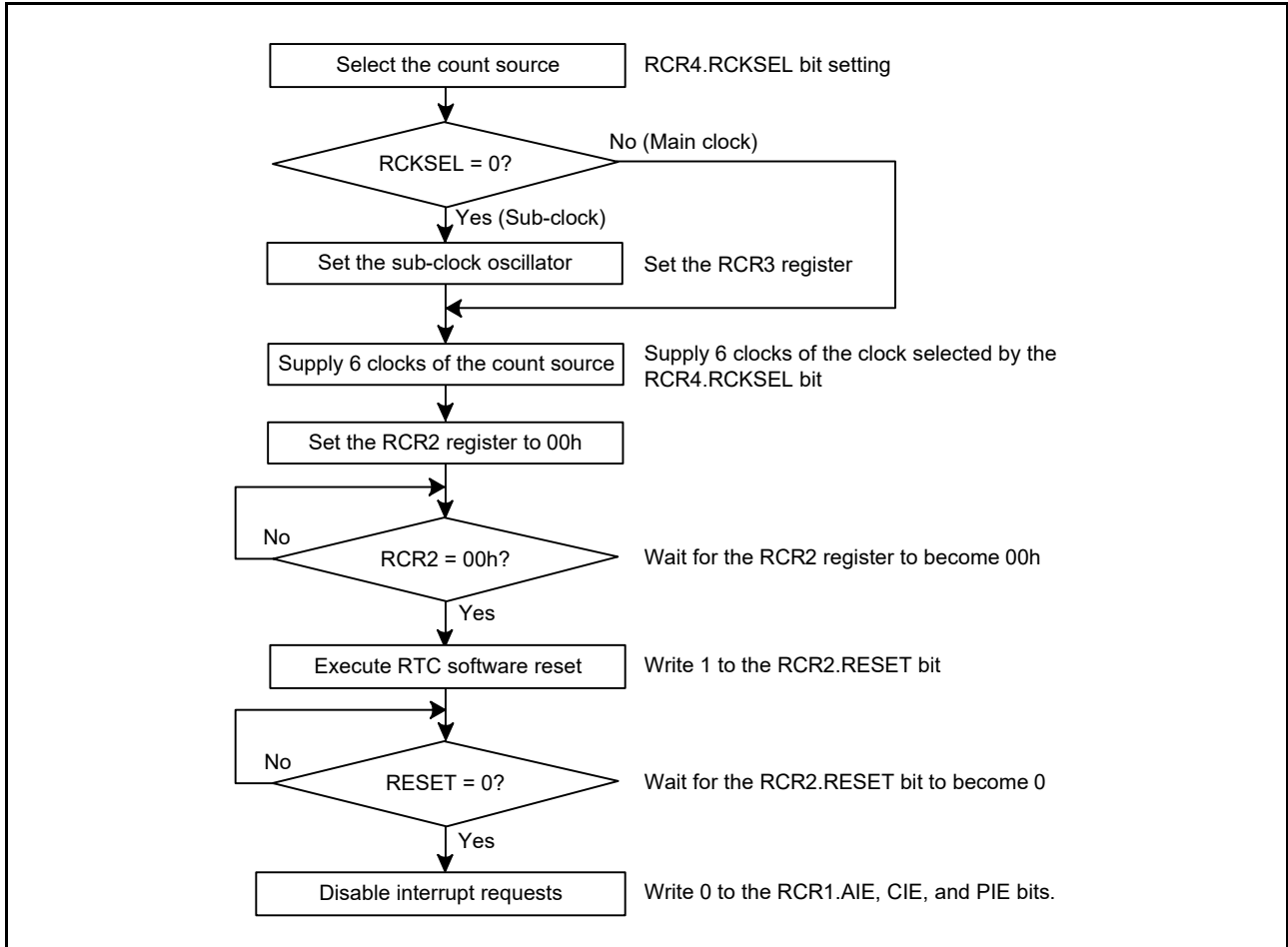
Before correction

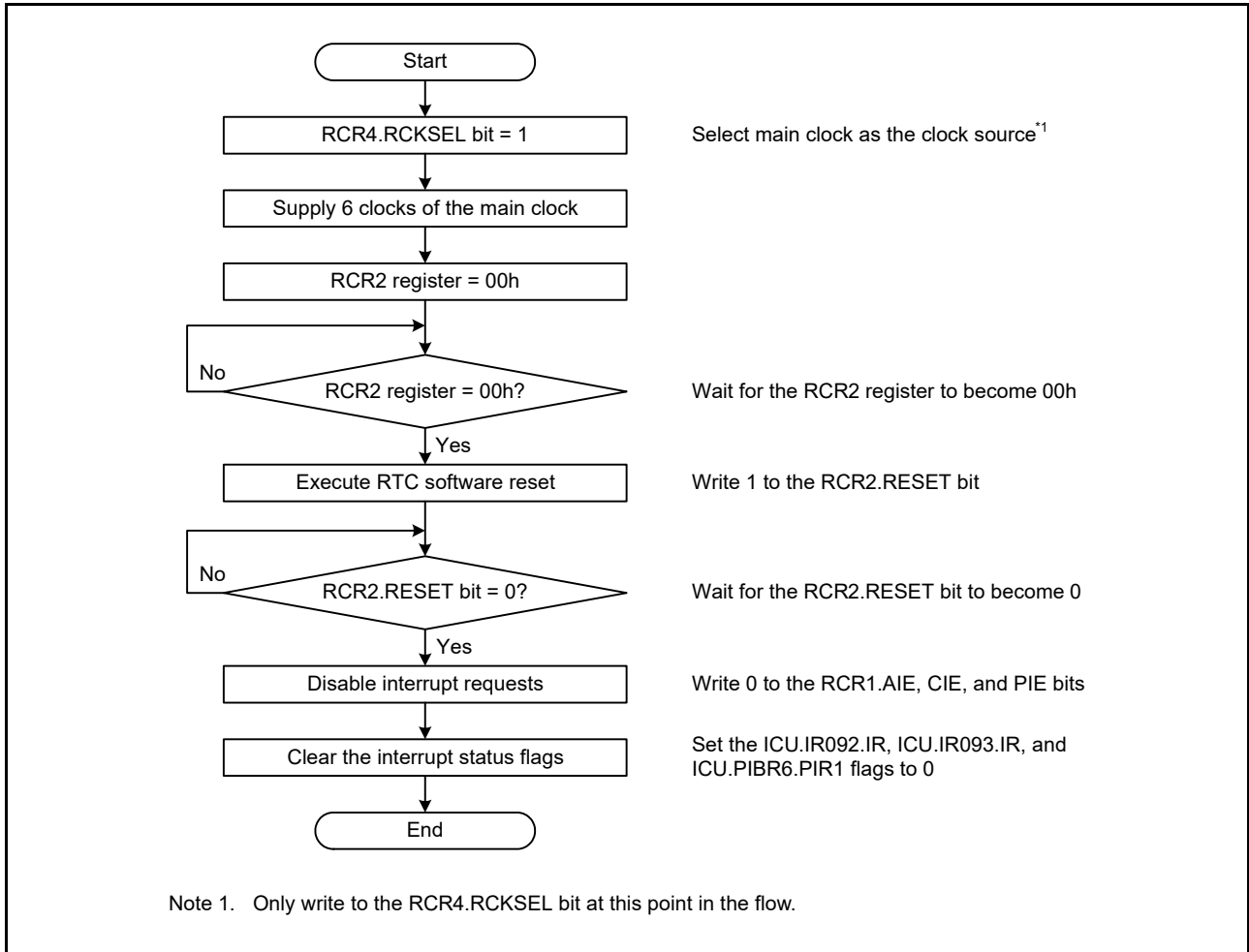**Figure 31.14   Initialization Procedure**

After correction

Note 1.   Only write to the RCR4.RCKSEL bit at this point in the flow.

Figure 31.14   Initialization Procedure (When Using Main Clock)

```
                          ┌──────────────┐
                          │    Start     │
                          └──────┬───────┘
                                 │
                    ┌────────────▼────────────┐
                    │   RCR4.RCKSEL bit = 0    │        Select sub-clock as the clock source*1
                    └────────────┬────────────┘
                                 │
                    ┌────────────▼────────────┐
                    │ Set the sub-clock       │        Set the SOSCCR, RCR3, and SOSCWTCR registers
                    │ oscillator*2            │
                    └────────────┬────────────┘
                                 │
                    ┌────────────▼────────────┐
                    │ Supply 6 clocks of the  │
                    │ sub-clock               │
                    └────────────┬────────────┘
                                 │
                    ┌────────────▼────────────┐
                    │  RCR2 register = 00h    │
                    └────────────┬────────────┘
                                 │
                    ◄────────────┤
               No   ┌────────────▼────────────┐
              ┌─────│  RCR2 register = 00h?   │        Wait for the RCR2 register to become 00h
              └─────►└────────────┬────────────┘
                              Yes │
                    ┌────────────▼────────────┐
                    │ Execute RTC software    │        Write 1 to the RCR2.RESET bit
                    │ reset                   │
                    └────────────┬────────────┘
                                 │
               No   ┌────────────▼────────────┐
              ┌─────│  RCR2.RESET bit = 0?    │        Wait for the RCR2.RESET bit to become 0
              └─────►└────────────┬────────────┘
                              Yes │
                    ┌────────────▼────────────┐
                    │ Disable interrupt       │        Write 0 to the RCR1.AIE, CIE, and PIE bits
                    │ requests                │
                    └────────────┬────────────┘
                                 │
                    ┌────────────▼────────────┐
                    │ Clear the interrupt     │        Set the ICU.IR092.IR, ICU.IR093.IR, and
                    │ status flags            │        ICU.PIBR6.PIR1 flags to 0
                    └────────────┬────────────┘
                                 │
                          ┌──────▼───────┐
                          │     End      │
                          └──────────────┘
```

Note 1.   Only write to the RCR4.RCKSEL bit at this point in the flow.
Note 2.   For the procedure for setting up a sub-clock oscillator, refer to section 9, Clock Generation Circuit.
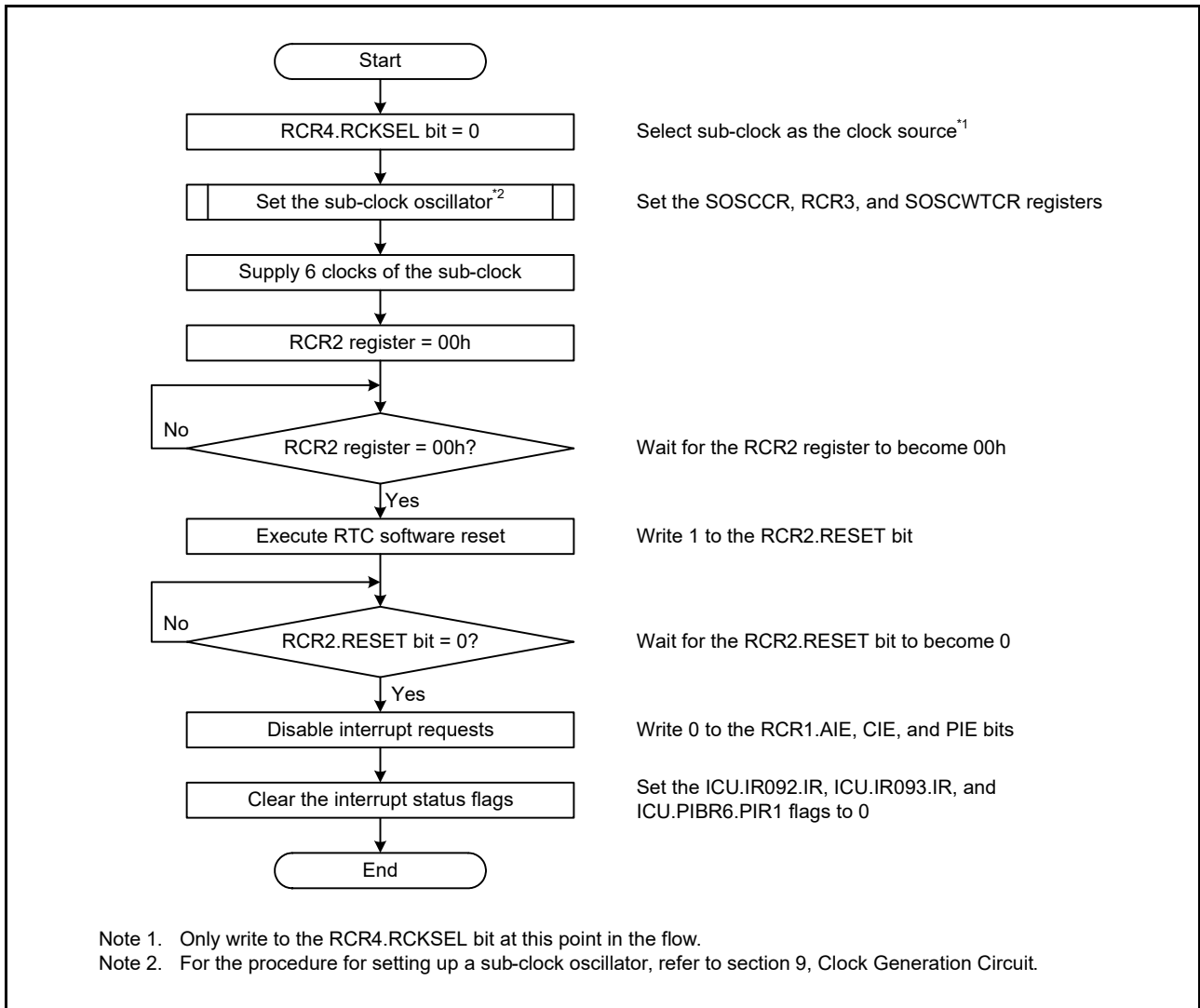
Figure 31.15   Initialization Procedure (When Using Sub-Clock)