[Product Generation Change]

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RENESAS TECHNICAL UPDATE

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Product Category	SRAM		Document No.	TN-M62-A135B/E	Rev.	2.00
Title	Notice about the generation change of 256Kbit LP SRAM series		Information Category	Product Generation Change		
Applicable Product	256Kbit Low Power SRAM ; M5M5256D series	Lot No. All shipped lots after '11/4	Reference Document	Nothing		

Please be informed that we, Renesas will be proceeding with the product generation change of 256Kbit LP SRAM from "M5M5256D series" to "R1LV5256E series" or "R1LP5256E series". We already have produced the new generation products: "R1LV5256E series and R1LP5256E series".

So your acceptance of paper qualification and your kind understanding are greatly appreciated.

<Generation Change>

This generation change is to shrink die with 0.15um technology, in order to improve the production efficiency.

All packages' outline is completely same.

We make use of Renesas original technology with adoption of memory cell with TFT load and capacitor structure for this part. By adopting the original technology, we could offer an excellent high reliability against Soft error and latch-up phenomenon.

<Objective parts>

256Kb (x8) 5V, SOP : from M5M5256DFP series to R1LP5256ESP series

256Kb (x8) 5V, TSOP(normal bend) : from M5M5256DVP series to R1LP5256ESA series

256Kb (x8) 3V, SOP : from M5M5256DFP-xxG series to R1LV5256ESP series

256Kb (x8) 3V, TSOP(normal bend) : from M5M5256DVP-xxG series to R1LV5256ESA series

<Document and Sample availability>

Data sheet : Available

CS sample : Available

Reliability report : Available

<Launch date of this "generation change">

We already have started to ship out new generation parts. There is a possibility to ship out both current parts series (M5M5256D) and new parts series (R1LP5256E or R1LV5256E) in parallel, because of our inventory of current parts series.

<replaced part name list on this generation change>

1) replaced part name on this generation change

<256Kb Low Power SRAM(3V version)>

Package	Current part name	Replaced part name
SOP	Not available	R1LV5256ESP-5SR
	Not available	R1LV5256ESP-5SI
	M5M5256DFP-70G	R1LV5256ESP-7SR
	M5M5256DFP-70XG	R1LV5256ESP-7SR
	M5M5256DFP-70GI	R1LV5256ESP-7SI

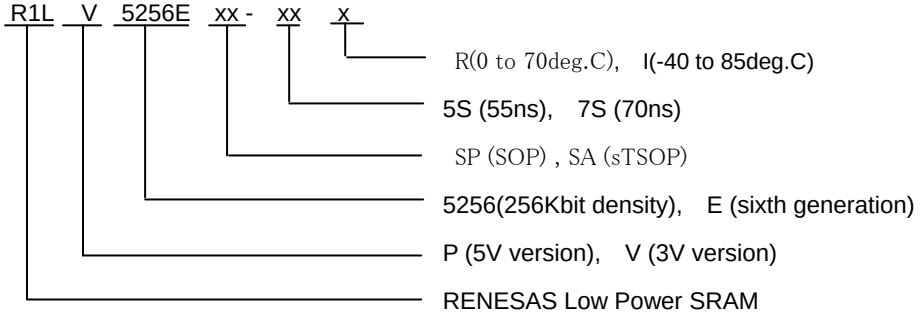
Package	Current part name	Replaced part name
TSOP (normal bend)	Not available	R1LV5256ESA-5SR
	Not available	R1LV5256ESA-5SI
	M5M5256DVP-70G	R1LV5256ESA-7SR
	M5M5256DVP-70XG	R1LV5256ESA-7SR
	M5M5256DVP-70GI	R1LV5256ESA-7SI

<256Kb Low Power SRAM(5V version)>

Package	Current part name	Replaced part name
SOP	M5M5256DFP-55LL	R1LP5256ESP-5SR
	M5M5256DFP-55XL	R1LP5256ESP-5SR
	Not available	R1LP5256ESP-5SI
	M5M5256DFP-70LL	R1LP5256ESP-7SR
	M5M5256DFP-70XL	R1LP5256ESP-7SR
	M5M5256DFP-70LLI	R1LP5256ESP-7SI

Package	Current part name	Replaced part name
TSOP (normal bend)	M5M5256DVP-55LL	R1LP5256ESA-5SR
	M5M5256DVP-55XL	R1LP5256ESA-5SR
	Not available	R1LP5256ESA-5SI
	M5M5256DVP-70LL	R1LP5256ESA-7SR
	M5M5256DVP-70XL	R1LP5256ESA-7SR
	M5M5256DVP-70LLI	R1LP5256ESA-7SI

2) Explanation about part name



Basically each correspondence follows above the list, however we'd like to ask you all to check data sheet of new part and to confirm whether all characteristics satisfy you or not.

<Comparison table between current parts series and new parts series>

Circuit	M5M5256D series	R1LV5256E / R1LP5256E series
Memory cell structure	High-resistance load	TFT load capacitor cell
Peripheral circuit	CMOS	CMOS

Process	M5M5256D series	R1LV5256E / R1LP5256E series
Wafer process layer	3poly, 1metal	8poly, 2metal, 1tungsten
Design rule	0.6um	0.15um
Gate oxide thickness	14nm	<For R1LP5256E series> Memory cell : 6.5nm peripheral circuit : 12nm <For R1LV5256E series> Memory cell / peripheral circuit : 6.5nm
Gate oxide material	SiO2	SiO2
Passivation thickness	0.75um	0.75um
Passivation material	p-SiN	p-SiN

Assembly	M5M5256D series	R1LV5256E / R1LP5256E series
Resin material	Epoxy Resin	Epoxy Resin
Frame material	Fe-Ni 42 alloy	Fe-Ni 42 alloy
Lead frame plating	Sn/Cu	Sn/Cu
Inner wire material	Au	Au
Die bond material	Resin	Resin

Sincerely yours.

<Renesas 256Kb LPSRAM's comparison table between M5M5256D series and R1LP5256E series>

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL	Symbol	R1LP5256Exx-xSR/SI
Memory cell structure		High-resistance load		TFT load + capacitor cell
Peripheral circuit		CMOS		<--
Design rule		0.6um		0.15um
Package		SOP 28pin(17.5mm x 11.93mm)		<--
		TSOP 28pin(13.4mm x 8mm)		<--

DC condition

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL		Symbol	R1LP5256Exx-xSR/SI	
Supply voltage	Vcc	4.5V to 5.5V		Vcc	<--	
Operating temperature range	Ta	55LL/70LL	0deg.C to 70deg.C	Ta	5SR/7SR	<--
		70LLI	-40deg.C to 85deg.C		5SI/7SI	<--
Input high voltage	VIH	2.2V(min.)/Vcc+0.3V(max.)		VIH	<--	
Input low voltage	VIL	-0.3V(min.)/0.8V(max.)		VIL	<--	

DC characteristics

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL		Symbol	R1LP5256Exx-xSR/SI	
Average operating current	Icc2(TTL, Cycle=55ns)	50mA(max.)/30mA(typ.)		Icc1(TTL, Cycle=55ns)	35mA(max.)/25mA(typ.)	
	Icc1(MOS, Cycle=1us)	4mA(max.)/2mA(typ.)		Icc2(MOS, Cycle=1us)	<--	
Standby current	Icc4(TTL input)	3mA(max.)		ISB(TTL input)	<--	
	Icc3(MOS input) (Vcc=5.5V)	up to 25deg.C	LL/LLI:2uA(max.)	ISB1(MOS input) (Vcc=5.5V)	up to 25deg.C	2uA(max.)/1uA(typ.)
			XL:0.4uA(max.)/0.1uA(typ.)			
		up to 40deg.C	LL/LLI:6uA(max.)		up to 40deg.C	3uA(max.)
			XL:1.2uA(max.)			
		up to 70deg.C	LL/LLI:20uA(max.)		up to 70deg.C	8uA(max.)
			XL:5uA(max.)			
		up to 85deg.C	LLI:40uA(max.)		up to 85deg.C	10uA(max.)
Output high voltage	VOH	2.4V(min.)		VOH	<--	
Output low voltage	VOL	0.4V(max.)		VOL	<--	

Capacitance

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL	Symbol	R1LP5256Exx-xSR/SI
Input capacitance	CI	6pF(max.)	C in	<--
Input/Output capacitance	CO	8pF(max.)	C I/O	<--

AC characteristics

Read Cycle

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL		Symbol	R1LP5256Exx-xSR/SI	
Read cycle time	tCR	55LL	55ns(min.)	tRC	5SR/5SI	<--
		70LL/70LLI	70ns(min.)		7SR/7SI	<--
Address access time	ta(A)	55LL	55ns(max.)	tAA	5SR/5SI	<--
		70LL/70LLI	70nm(max.)		7SR/7SI	<--
Chip select access time	ta(S)	55LL	55ns(max.)	tACS	5SR/5SI	<--
		70LL/70LLI	70nm(max.)		7SR/7SI	<--
Output enable to output valid	ta(OE)	55LL	30ns(max.)	tOE	5SR/5SI	<--
		70LL/70LLI	35ns(max.)		7SR/7SI	<--
Output hold from address change	tv(A)	55LL	10ns(min.)	tOH	5SR/5SI	<--
		70LL/70LLI	10ns(min.)		7SR/7SI	<--
Chip select to output in low-Z/ Output enable to output in low-Z	ten(S,OE)	55LL	5ns(min.)	tCLZ, tOLZ	5SR/5SI	<--
		70LL/70LLI	5ns(min.)		7SR/7SI	<--
Chip disable to output in high-Z/ Output disable to output in high-Z	tdis(S,OE)	55LL	20ns(max.)	tCHZ, tOHZ	5SR/5SI	<--
		70LL/70LLI	25ns(max.)		7SR/7SI	<--

Write Cycle

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL		Symbol	R1LP5256Exx-xSR/SI	
Write cycle time	tCW	55LL	55ns(min.)	tWC	5SR/5SI	<--
		70LL/70LLI	70ns(min.)		7SR/7SI	<--
Address valid to end of write time	tsu(A-WH)	55LL	50ns(min.)	tAW	5SR/5SI	<--
		70LL/70LLI	65ns(min.)		7SR/7SI	<--
Chip select to end of write	tsu(S)	55LL	50ns(min.)	tCW	5SR/5SI	<--
		70LL/70LLI	65ns(min.)		7SR/7SI	<--
Write pulse width	tw(W)	55LL	40ns(min.)	tWP	5SR/5SI	<--
		70LL/70LLI	50ns(min.)		7SR/7SI	<--
Address setup time	tsu(A)	55LL	0ns(min.)	tAS	5SR/5SI	<--
		70LL/70LLI	0ns(min.)		7SR/7SI	<--
Write recovery time	trec(W)	55LL	0ns(min.)	tWR	5SR/5SI	<--
		70LL/70LLI	0ns(min.)		7SR/7SI	<--
Data to write time overlap	tsu(D)	55LL	25ns(min.)	tDW	5SR/5SI	<--
		70LL/70LLI	30ns(min.)		7SR/7SI	<--
Data hold from write time	th(D)	55LL	0ns(min.)	tDH	5SR/5SI	<--
		70LL/70LLI	0ns(min.)		7SR/7SI	<--
Output enable from end of write	ten(W, OE)	55LL	5ns(min.)	tOW	5SR/5SI	<--
		70LL/70LLI	5ns(min.)		7SR/7SI	<--
Output disable to output in high-Z	tdis(OE,W)	55LL	20ns(max.)	tOHZ,tWHZ	5SR/5SI	0ns(min.)/20ns(max.)
		70LL/70LLI	25ns(max.)		7SR/7SI	0ns(min.)/25ns(max.)

Data retention characteristics

Item	Symbol	M5M5256Dxx-xxLL/LLI/XL		Symbol	R1LP5256Exx-xSR/SI	
Vcc for data retention	Vcc(PD)	2.0V(min.)		VDR	<--	
Data retention current	Icc(PD) (Vcc=3.0V)	up to 25deg.C	LL/LLI:1uA(max.)	IccDR (Vcc=3.0V)	up to 25deg.C	2uA(max.)/1uA(typ.)
			XL:0.2uA(max.)/0.05uA(typ.)			
		up to 40deg.C	LL/LLI:3uA(max.)		up to 40deg.C	<--
			XL:0.6uA(max.)			
		up to 70deg.C	LL/LLI:10uA(max.)		up to 70deg.C	8uA(max.)
			XL:2uA(max.)			
		up to 85deg.C	LLI:20uA(max.)		up to 85deg.C	10uA(max.)
Chip deselect to data retention time	tsu(PD)	0ns(min.)		tCDR	<--	
Operation recovery time	trec(PD)	55ns/70ns(min.)		tR	5ms(min.)	

<Renesas 256Kb LPSRAM's comparison table between M5M5256D series and R1LV5256E series>

Item	Symbol	M5M5256Dxx-70G/GI/XG	Symbol	R1LV5256Exx-7SR/SI
Memory cell structure		High-resistance load		TFT load + capacitor cell
Peripheral circuit		CMOS		<--
Design rule		0.6um		0.15um
Package		SOP 28pin(17.5mm x 11.93mm)		<--
		TSOP 28pin(13.4mm x 8mm)		<--

DC condition

Item	Symbol	M5M5256Dxx-70G/GI/XG		Symbol	R1LV5256Exx-7SR/SI	
Supply voltage	Vcc	3.0V to 3.6V/4.5V to 5.5V		Vcc	2.7V to 3.6V(*)	
Operating temperature range	Ta	70G	0deg.C to 70deg.C	Ta	7SR	<--
		70GI	-40deg.C to 85deg.C		7SI	<--
Input high voltage	VIH	Vcc=3.3 +/- 0.3V	2.0V(min.)/Vcc+0.3V(max.)	VIH	<--	
		Vcc=5.0 +/- 0.3V	2.2V(min.)/Vcc+0.3V(max.)		-	
Input low voltage	VIL	Vcc=3.3 +/- 0.3V	-0.3V(min.)/0.6V(max.)	VIL	<--	
		Vcc=5.0 +/- 0.3V	-0.3V(min.)/0.8V(max.)		-	

(*) 5V product is R1LP5256E series.

DC characteristics

Item	Symbol	M5M5256Dxx-70G/GI/XG		Symbol	R1LV5256Exx-7SR/SI	
Average operating current	Icc2(TTL, Cycle=70ns)	Vcc=3.3 +/- 0.3V	25mA(max.)/14mA(typ.)	Icc1(TTL, Cycle=70ns)	<--	
		Vcc=5.0 +/- 0.3V	45mA(max.)/25mA(typ.)		-	
	Icc1(MOS, Cycle=1us)	Vcc=3.3 +/- 0.3V	3mA(max.)/1.5mA(typ.)	Icc2(MOS, Cycle=1us)	5mA(max.)/2mA(typ.)	
		Vcc=5.0 +/- 0.3V	4mA(max.)/2mA(typ.)		-	
Standby current	Icc4(TTL input)	Vcc=3.3 +/- 0.3V	0.33mA(max.)	ISB(TTL input)	<--	
		Vcc=5.0 +/- 0.3V	3mA(max.)		-	
	Icc3(MOS input) (Vcc=3.6V)	up to 25deg.C	G/GI:1.2uA(max.)	ISB1(MOS input) (Vcc=3.6V)	up to 25deg.C	2uA(max.)/1uA(typ.)
			XG:0.3uA(max.)/0.05uA(typ.)			
		up to 40deg.C	G/GI:3.6uA(max.)		up to 40deg.C	3uA(max.)
			XG:0.8uA(max.)			
		up to 70deg.C	G/GI:12uA(max.)		up to 70deg.C	8uA(max.)
			XG:2.4uA(max.)			
		up to 85deg.C	GI:24uA(max.)		up to 85deg.C	10uA(max.)
	Icc3(MOS input) (Vcc=5.5V)	up to 25deg.C	G/GI:2uA(max.)	Icc3(MOS input) (Vcc=5.5V)	-	
			XG:0.4uA(max.)/0.1uA(typ.)			
		up to 40deg.C	G/GI:6uA(max.)			
			XG:1.2uA(max.)			
		up to 70deg.C	G/GI:20uA(max.)			
			XG:5uA(max.)			
		up to 85deg.C	GI:40uA(max.)			
Output high voltage	VOH	2.4V(min.)		VOH	<--	
Output low voltage	VOL	0.4V(max.)		VOL	<--	

Capacitance

Item	Symbol	M5M5256Dxx-70G/GI/XG	Symbol	R1LV5256Exx-7SR/SI
Input capacitance	CI	6pF(max.)	C in	<--
Input/Output capacitance	CO	8pF(max.)	C I/O	<--

AC characteristics

Read Cycle

Item	Symbol	M5M5256Dxx-70G/GI/XG	Symbol	R1LV5256Exx-7SR/SI
Read cycle time	tCR	70ns(min.)	tRC	<--
Address access time	ta(A)	70ns(max.)	tAA	<--
Chip select access time	ta(S)	70ns(max.)	tACS	<--
Output enable to output valid	ta(OE)	35ns(max.)	tOE	<--
Output hold from address change	tv(A)	10ns(min.)	tOH	<--
Chip select to output in low-Z/ Output enable to output in low-Z	ten(S,OE)	5ns(min.)	tCLZ, tOLZ	<--
Chip disable to output in high-Z/ Output disable to output in high-Z	tdis(S,OE)	25ns(max.)	tCHZ, tOHZ	<--

Write Cycle

Item	Symbol	M5M5256Dxx-70G/GI/XG		Symbol	R1LV5256Exx-7SR/SI
Write cycle time	tCW	70ns(min.)		tWC	<--
Address valid to end of write time	tsu(A-WH)	65ns(min.)		tAW	<--
Chip select to end of write	tsu(S)	65ns(min.)		tCW	<--
Write pulse width	tw(W)	Vcc=3.3 +/- 0.3V	55ns(min.)	tWP	50ns(min.)
		Vcc=5.0 +/- 0.3V	50ns(min.)		-
Address setup time	tsu(A)	0ns(min.)		tAS	<--
Write recovery time	trec(W)	0ns(min.)		tWR	<--
Data to write time overlap	tsu(D)	30ns(min.)		tDW	<--
Data hold from write time	th(D)	0ns(min.)		tDH	<--
Output enable from end of write	ten(W, OE)	5ns(min.)		tOW	<--
Output disable to output in high-Z	tdis(OE,W)	25ns(max.)		tOHZ,tWHZ	0ns(min.)/25ns(max.)

Data retention characteristics

Item	Symbol	M5M5256Dxx-70G/GI/XG		Symbol	R1LV5256Exx-7SR/SI	
Vcc for data retention	Vcc(PD)	2.0V(min.)		VDR	<--	
Data retention current	Icc(PD) (Vcc=3.0V)	up to 25deg.C	G/GI:1uA(max.)	IccDR (Vcc=3.0V)	up to 25deg.C	2uA(max.)/1uA(typ.)
			XG:0.2uA(max.)/0.05uA(typ.)			
		up to 40deg.C	G/GI:3uA(max.)		up to 40deg.C	3uA(max.)
			XG:0.6uA(max.)			
		up to 70deg.C	G/GI:10uA(max.)		up to 70deg.C	8uA(max.)
			XG:2uA(max.)			
		up to 85deg.C	GI:20uA(max.)		up to 85deg.C	10uA(max.)
Chip deselect to data retention time	tsu(PD)	0ns(min.)		tCDR	<--	
Operation recovery time	trec(PD)	70ns(min.)		tR	5ms(min.)	