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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0567B/E	Rev.	2.00
Title	RH850 G3M stuck Issue		Information Category	Technical Notification		
Applicable Product	RH850/C1H, C1M RH850/D1M1A, D1M1H, D1M2 RH850/E1L, E1M-S RH850/F1H RH850/P1H-C, P1M-C	Lot No. All	Reference Document	See related documents below.		

We confirmed that the G3M CPU gets stuck while running a certain program code.

1. Overview

For the following RH850 products equipped with the G3M core, it has been confirmed that when executing specific program code and simultaneously accessing Code Flash with the instruction fetch access by CPU and one or more bus masters (including the accessing data by CPU executing the program), a conflict occurs between "branch prediction" and "instruction fetch" within the CPU core, causing the CPU to stop (CPU Stuck).

The only way to recover from this "CPU Stuck" is to reset.

Applicable Product: RH850/C1H, C1M, D1M1A, D1M1H, D1M2, E1L, E1M-S, F1H, P1H-C, P1M-C

Non-Applicable Product: RH850/D1L1, D1L2, D1M1, D1M1-V2, D1S1, F1M, P1L-C, P1M, P1M-E

2. Occurrence Conditions

If All below condition are applicable to source code, source code has possibility to generate issue.

Condition 1: Branch to backward address

[Branch instruction A] Bcond, JR, LOOP

Condition 2: [Branch instruction B] place to after jump target of [Branch instruction A]. And, each instruction address are place to different cache line (16-byte placement block) and adjacent.

[Branch instruction B] BR, JR, JARL, JMP

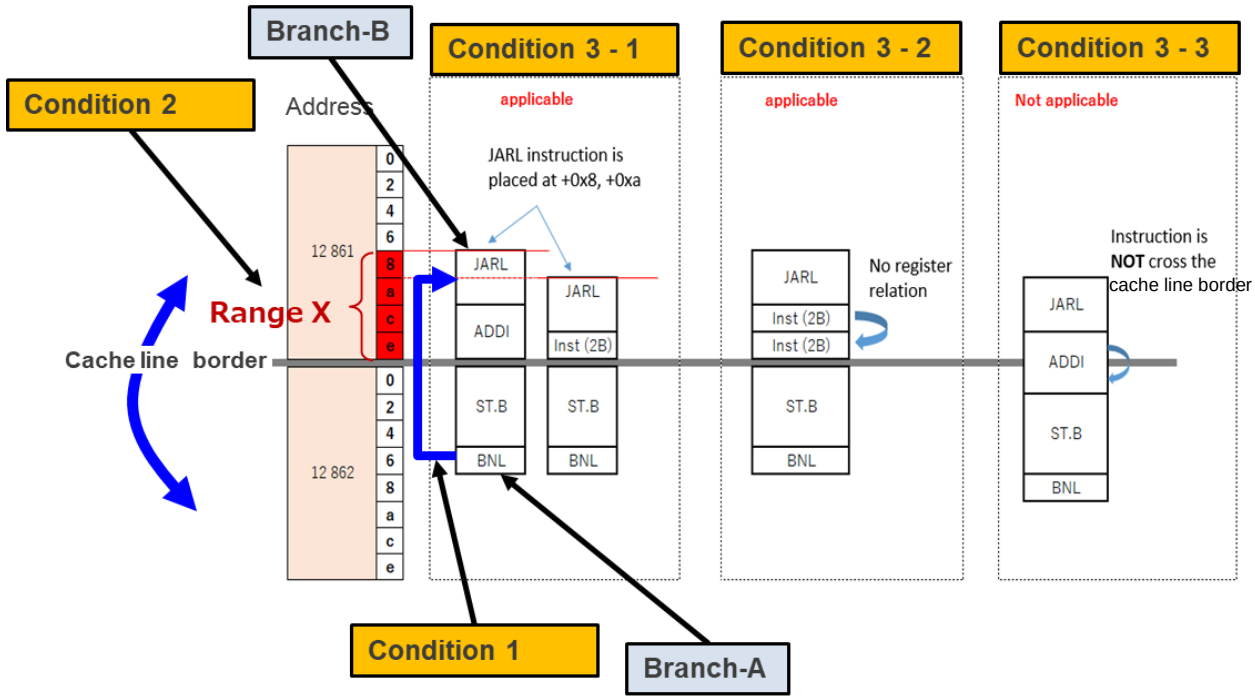
Condition 3:

3-1. [Branch Instruction B] is placed to address +0x8 ~ +0xf [Range X]

3-2. 1 or 2 instruction are placed between [Branch instruction B] and cache line border except following condition

- [1 instruction]: SYNCI
- [2 instruction]: 2 instruction doesn’t use same register (doesn’t occur conflict of register)
  or either instruction is NOP/SYNCI/SYNCP/SYNCM/part of FPU instruction

3-3. Instruction doesn’t cross the cache line (16-byte placement block) in [Range X]



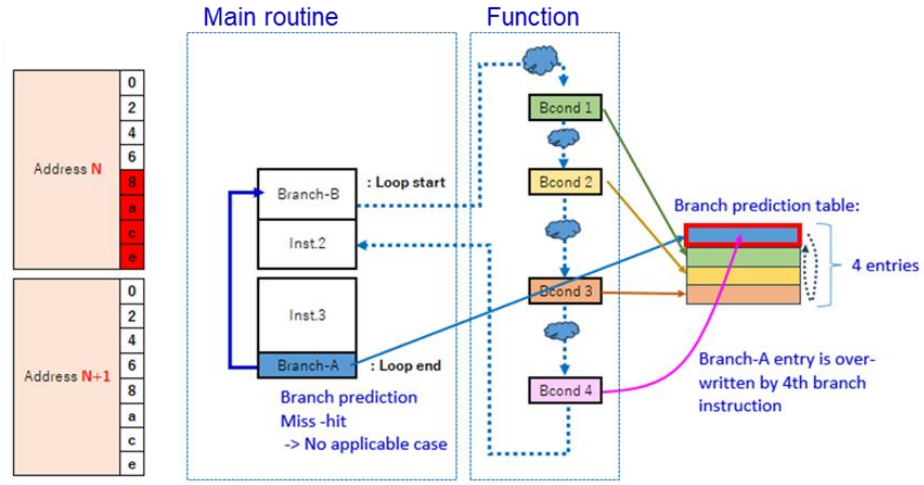
Code that satisfies static conditions may not be applicable due to dynamic conditions.

One of the dynamic conditions is the number of branches in the code sequence from [Branch instruction B] (the call to "Function")

- From the viewpoint of the HW mechanism, one of the applicable conditions is that "the branch prediction when [Branch instruction A] is executed is a hit".
- If the "function" called from [Branch instruction B] has four or more branch instructions (Bcond 1,2,3,4) <*1> the branch prediction table entry for [Branch instruction A] will be lost by re-executing the [Branch instruction A], and it will not be applicable.

<*1> Bcond, JR, Branch prediction function for LOOP instructions

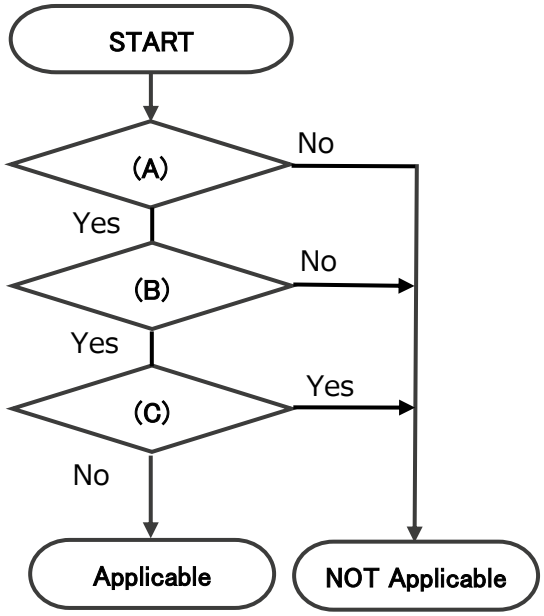
➢ Branch Prediction Entry Status



3. Judgement flow

3.1 Single-core product

< Judgement Flow >



	Content
(A)	Is the product applicable (●) in the table below?
(B)	Were applicable parts detected by the checker tool?
(C)	Can you say that all detected applicable parts were mistakenly detected?

Product	Bus masters that simultaneously access the Code Flash (Description of Bus Master 1,3,4 is written in the table below)			
Product Name	Bus Master 1 only	Bus Master 1+3	Bus Master 1+4	Bus Master 1+3+4
C1M	●	N/A	●	N/A
D1M1A, D1M1H, D1M2		N/A	●	N/A
E1L (160MHz)				●
E1L (240MHz)	●	●	●	●
E1M-S	●	●	●	●
P1M-C (120/160MHz)		●	●	●
P1M-C (240MHz)	●	●	●	●

● : Product subject for judgement flow

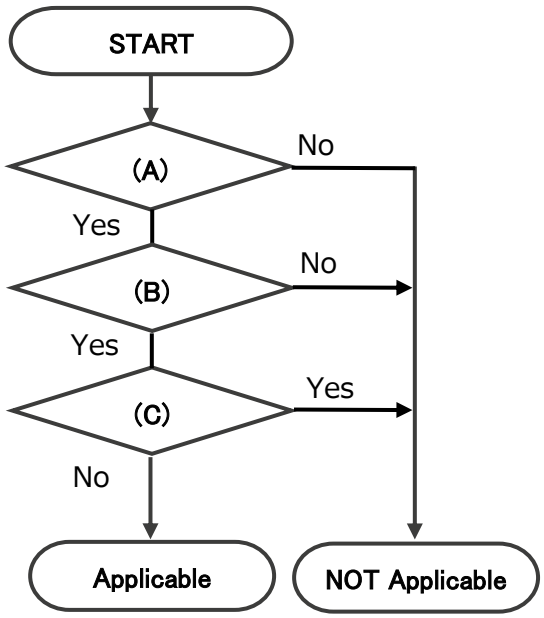
N/A : No relevant combination

Bus Master 1	CPU1
Bus Master 2	not implement
Bus Master 3	PCU or ICU-M
Bus Master 4	1 or more Bus Masters excluding the ones above（DMA and others）

For the Bus Master of each product, refer to section 5, Bus Master List.

3.2 Multi-core product, CPU1 and CPU2 access the same Bank of Code Flash

< Judgement Flow >



	Content
(A)	Is the product applicable (●) in the table below?
(B)	Were applicable parts detected by the checker tool?
(C)	Can you say that all detected applicable parts were mistakenly detected?

Bus masters that simultaneously access the same Bank of Code Flash (Description of Bus Master 1,2,3,4 is written in the table below)				
Product Name	Bus Master 1+2	Bus Master 1+2+3	Bus Master 1+2+4	Bus Master 1+2+3+4
C1H	●	N/A	●	N/A
F1H		●	●	●
P1H-C (160MHz)	●	●	●	●
P1H-C (240MHz)	●	●	●	●

● : Product subject for judgement flow

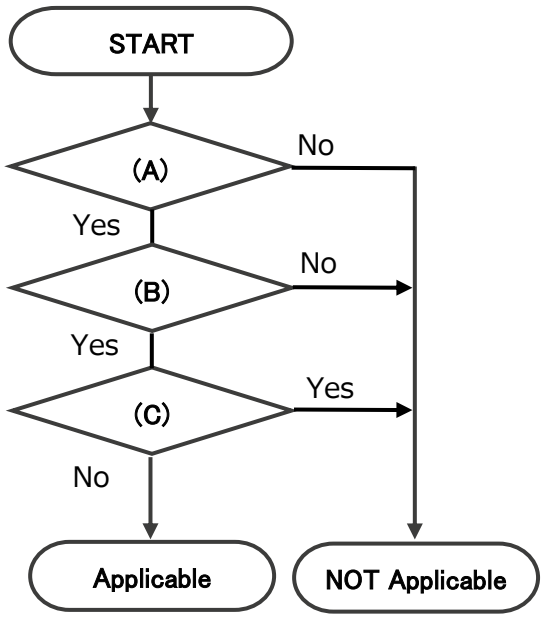
N/A : No relevant combination

Bus Master 1	CPU1
Bus Master 2	CPU2
Bus Master 3	ICU-M
Bus Master 4	1 or more Bus Masters excluding the ones above（DMA and others）

For the Bus Master of each product, refer to section 5, Bus Master List.

3.3 Multi-core product, CPU1 and CPU2 access the different Bank of Code Flash

< Judgement Flow >



	Content
(A)	Is the product applicable (●) in the table below?
(B)	Were applicable parts detected by the checker tool?
(C)	Can you say that all detected applicable parts were mistakenly detected?

Bus masters that simultaneously access the same Bank of Code Flash (Description of Bus Master 1,2,3,4 is written in the table below)				
Product Name	Bus Master (1or2) only	Bus Master (1or2)+3	Bus Master (1or2)+4	Bus Master (1or2)+3+4
C1H	●	N/A	●	N/A
F1H				●
P1H-C (160MHz)		●	●	●
P1H-C (240MHz)	●	●	●	●

● : Product subject for judgement flow

N/A : No relevant combination

Bus Master 1	CPU1
Bus Master 2	CPU2
Bus Master 3	ICU-M
Bus Master 4	1 or more Bus Masters excluding the ones above（DMA and others）

For the Bus Master of each product, refer to section 5, Bus Master List.

4. Workaround

If there is a problem, please do one of the following.

(1) Disable the “branch prediction function” of the CPU core.

(2) Prevent branch prediction hit against [Branch instruction A].

How to disable the “branch prediction function”

The G3M "Branch Prediction" feature is enabled after a reset (default) and can be disabled with bit 0 of the Branch Prediction Control Register (BPCR). It is not available in the current users manual.

Register No. (regID, selID)	Symbol	Function	Access Permission
SR8,12	BPCR	Branch prediction control	SV

BPCR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BPCLR	BPEN

Value after reset 0000 0001H

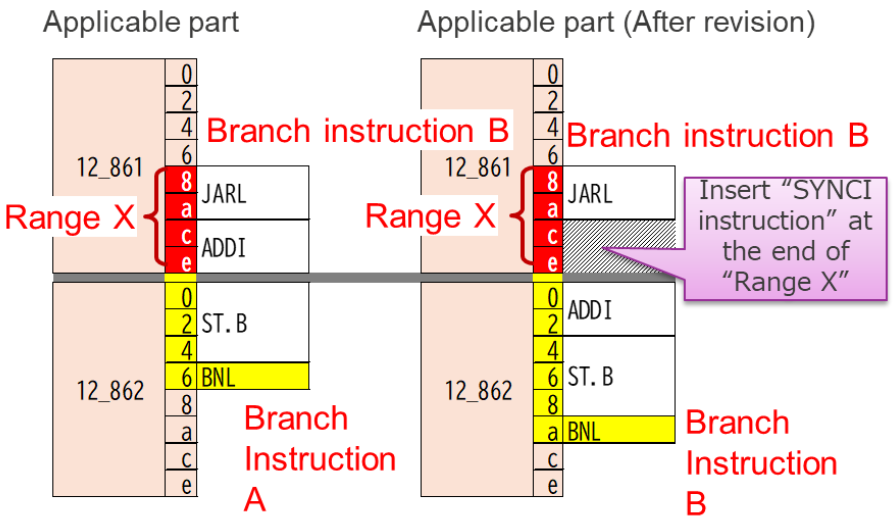
Table BPCR Register Contents

Bit	Name	Description	R/W	Value after Reset
31 to 2	-	(Reserved for future expansion. Be sure to set to 0.)	R	0
1	BPCLR	When this bit is set to 1, the entire branch prediction entry is cleared. After this bit is set to 1, it is read as 1 until clearing is completed. The bit is cleared to 0 once clearing is completed. This function is no supported. Be sure to set to 0.	R/W	0
0	BPEN	This bit indicates valid/invalid status of branch prediction function. 0: Branch prediction is invalid 1: Branch prediction is valid This bit is read as the previous value until the setting is actually reflected in the branch prediction function.	R/W	1

Workaround: Clear the BPEN bit to 0 to disable Branch Prediction

(2) How to disable the branch prediction capability

Insert SYNCI instruction at the end of “Range X” in all relevant parts.



5. Bus Master List

Product	Bus Master 1	Bus Master 2	Bus Master 3	Bus Master 4					
C1H	CPU1	CPU2	-	DMA	-	-	-	-	-
C1M	CPU1	-	-	DMA	-	-	-	-	-
D1M1A	CPU1	-	-	DMA	SPEA (XC0)	ETNB (XC1)	GPU2D (XC1)	JCUA (XC1)	NFMA (XC1)
D1M1H	CPU1	-	-	DMA	SPEA (XC0)	ETNB (XC1)	GPU2D (XC1)	JCUA (XC1)	
D1M2	CPU1	-	-	DMA	SPEA (XC0)	ETNB (XC1)	GPU2D (XC1)	JCUA (XC1)	MLBB (XC1)
E1L	CPU1	-	PCU	DMA	-	-	-	-	-
E1M-S	CPU1	-	PCU	DMA	FlexRay (H-Bus)	-	-	-	-
F1H	CPU1	CPU2	ICUMB	DMA	FLXA (H-Bus)	ETNB (H-Bus)	-	-	-
P1H-C	CPU1	CPU2	ICUMC	DMA	FLX0/1 (H-Bus)	ETNA (H-Bus)	HS-USRT (H-Bus)	-	-
P1M-C	CPU1	-	ICUMC	DMA	FLX0/1 (H-Bus)	ETNA (H-Bus)	HS-USRT (H-Bus)	-	-

<Reference Documents>

Series	Group	Documents Title	Rev.	Document Number
RH850	C1H/C1M	RH850/C1x User's Manual: Hardware	1.60	R01UH0414EJ0160
RH850	D1M1A/D1M1H/ D1M2	RH850/D1L/D1M Group User's Manual: Hardware	2.20	R01UH0451EJ0220
RH850	E1L	RH850/E1L User's Manual: Hardware	1.20	R01UH0468EJ0120
RH850	E1M-S	RH850/ E1M-S User's Manual: Hardware	1.20	R01UH0466EJ0120
RH850	F1H	RH850/ F1H Group User's Manual: Hardware	1.12	R01UH0445EJ0112
RH850	F1H-100	RH850/F1H PREMIUM 100pin Version User's Manual: Hardware	1.00	R01UH0631EJ0100
RH850	P1H-C/P1M-C	RH850/P1x-C Group User's Manual: Hardware	1.40	R01UH0517EJ0140
RH850		RH850G3M User's Manual: Software	1.40	R01US0123EJ0140