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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A006A/E	Rev.	1.00
Title	RZ/A1L Group: Notes about DMA transfer function of UBS2.0 host/function module		Information Category	Technical Notification		
Applicable Product	RZ/A Series RZ/A1L Group	Lot No. All	Reference Document	RZ/A1L Group User's Manual: Hardware Rev 1.00 (R01UH0437EJ0100)		

In RZ/A1L Group, description deficiency of specification about DMA transfer function of USB 2.0 host/function module is found. The detail of description deficiency is shown in below. According to this update, relevant manual will be revised.

1. The detail of description deficiency of specification

The procedure when access mode to FIFO buffer will be set to 16-byte continuous access mode, or 32-byte continuous access mode is not described in section 28.3.6 (DMAn-FIFO Bus Configuration Registers (D0FBCFG, D1FBCFG)) of the User's Manual.

This procedure is unified specification of RZ/A1H Group, RZ/A1M Group, and RZ/A1L Group. And in RZ/A1H Group and RZ/A1M Group, this specification is already described in User's Manual Rev 1.00. In RZ/A1L Group, this specification will be described in User's Manual Rev 2.00.

2. The effect of description deficiency of procedure

If the procedure to be set in 16-byte continuous access mode or 32-byte continuous access mode described in "3. Additional specification details" is not performed, DMA transfer is not completed successfully.

3. Additional specification details

The User's Manual will be modified as follows. (additional portion is described in red)

28.3.6 DMAn-FIFO Bus Configuration Registers (D0FBCFG, D1FBCFG)

D0FBCFG is a register that controls bus access to the DMA0-FIFO and D1FBCFG is a register that controls bus access to the DMA1-FIFO. Note that the setting of this register is invalid when the DMA0-FIFO bus or DMA1-FIFO bus is connected to the local bus.

These registers are initialized by a power-on reset.

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Bit	Bit Name	Initial Value	R/W	Description
15, 14	-	Undefined	R	Reserved The read value is undefined. The write value should always be 0.
13, 12	DFACC[1:0]	00	R/W	DMAx FIFO Access Mode Specifies the access mode of the FIFO port. 00: Cycle steal mode (initial value) 01: 16-byte continuous access mode 10: 32-byte continuous access mode 11: Setting prohibited These bits specify a DMA transfer mode. (a) In cycle steal mode, use the DnFIFO port to access the FIFO buffer. (b) In 16-byte/32-byte continuous access mode, use the DnFIFO continuous transfer port to access the FIFO buffer. The MBW bit in DnFIFOSEL can be set to 10 (32-bit width) only. Be sure to follow the procedure below when setting the DFACC bits for 16- or 32-byte continuous access. (1) Set the DREQE bit in the DnFIFOSEL register to 0. (2) Set the DFACC bits to 01 (16 bytes) or 10 (32 bytes). (3) In the DnFIFOSEL register, set the CURPIPE bits to 0000 (specifying no pipe) and the MBW bits to 10 (32-bit width) at the same time. After that, read the CURPIPE bits to confirm that they have been updated to the written value (0000). (4) Use the CPU to dummy-read the DnFIFO port register (DnFIFO) with 32-bit width (the value read data can be discarded). After that, specify the target pipe by using the CURPIPE bits in the DnFIFOSEL register and read the CURPIPE bits to confirm that they have been updated to written value. (5) Set the DREQE bit in the DnFIFOSEL to 1. Note that the above procedure is not required if these bits are to be set for the cycle-stealing mode (not following the procedure has no effect).
11 to 5	-	Undefined	R	Reserved The read value is undefined. The write value should always be 0.

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