Current Consumption Reduction Solutions

Terms and Definitions

ACMP	Analog Comparator
ADC	Analog-to-digital converter
DCMP	Digital Comparator
IC	Integrated Circuit
MCU	Microcontroller Unit
OSC	Oscillator
WS	Wake/Sleep

Introduction

Today's rapidly evolving technological landscape facilitates the constant demand for faster, more efficient, and smarter electronic devices. Integrated circuits (ICs) lie at the heart of these devices, serving as the building blocks of virtually all modern electronic systems, from smartphones to supercomputers. However, with the proliferation of these devices comes an associated increase in energy consumption and carbon emissions, posing significant challenges to our global sustainability efforts. Figure 1 shows the history of the world's electricity consumption.

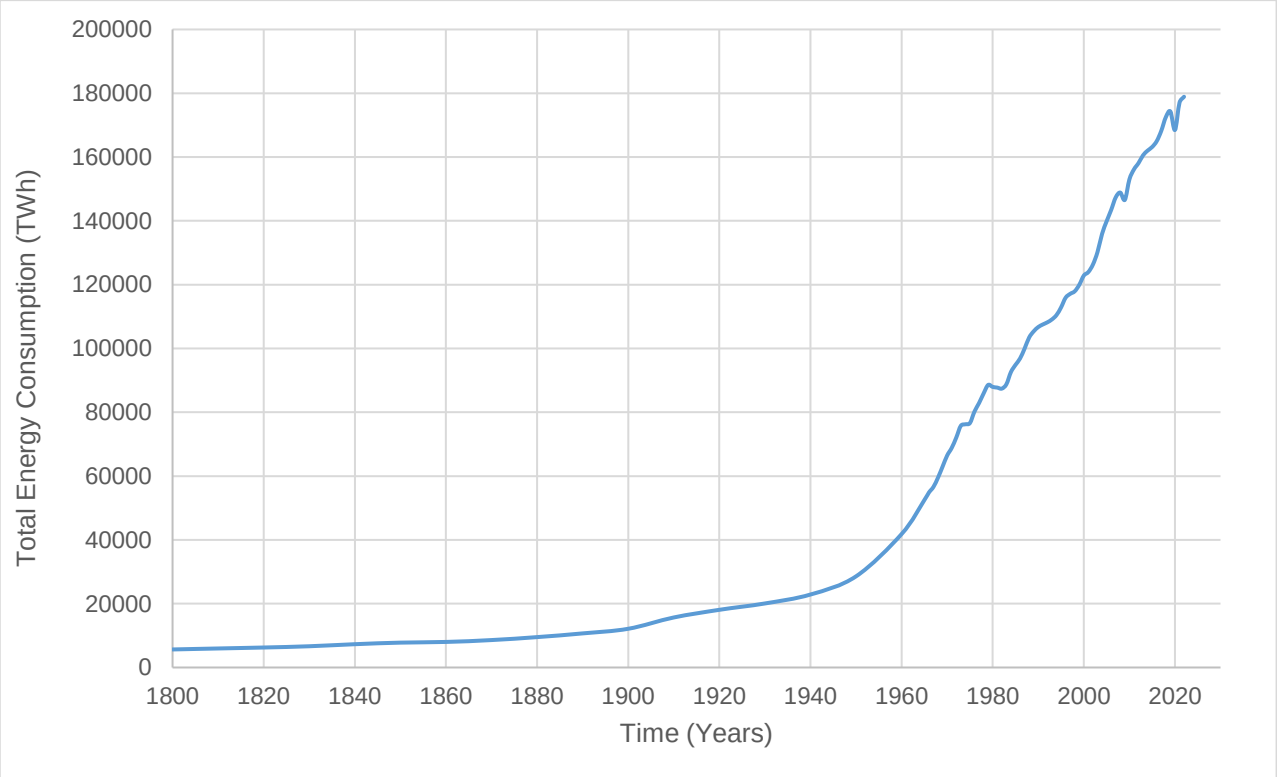

Figure 1. Historical Global Electricity Consumption*

* Source: Energy Institute - Statistical Review of World Energy (2023); Smil (2017)

Reducing the power consumption of ICs is not just a matter of improving device efficiency; it is a critical step towards mitigating the environmental impact of the electronics industry. As the world grapples with the urgent need to reduce carbon footprints and combat climate change, the semiconductor industry finds itself at a crossroads. While advancements in IC design and fabrication have led to remarkable improvements in performance and functionality, achieving substantial reductions in power consumption remains a formidable challenge.

1. CMOS Power Consumption

The power consumption for CMOS (complementary metal–oxide–semiconductor) technology, which dominates the market, is featured by extremely low power consumption.

The power consumption in CMOS technology consists of two main types: dynamic power and static power, often referred to as leakage power. In geometries smaller than 100 nm, leakage power becomes the primary consumer of energy, while in larger geometries, dynamic power plays a more significant role. Dynamic power is the combined effect of switching power and short-circuit power. The total power is the sum of dynamic and static power:

$$\text{Total Power} = P_{switching} + P_{short\text{-}circuit} + P_{leakage}$$

1.1 Dynamic Power Consumption

Switching power is dissipated when charging or discharging load capacitance.

$$P_{switching} = AF\ f\ C_L\ V_{DD}^2$$

Where:

AF – activity factor (the average fraction of time the signal is high or switching)

f – switching frequency

C_L – load capacitance

V_{DD} – supply voltage

Figure 2 shows a CMOS inverter, which has dynamic power consumption during switching due to the need to charge and discharge the load capacitance.

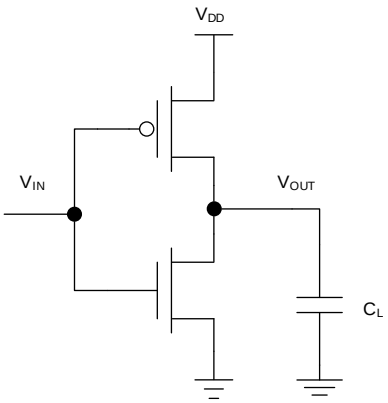

Figure 2. CMOS Inverter

Short-circuit power refers to the power dissipated when there is an instantaneous short-circuit connection between the supply voltage and the ground during the gate's state transition.

$$P_{short\text{-}circuit} = I_{sc}\ V_{DD}\ f$$

where:

I_{sc} – the short-circuit current during switching

V_{DD} – supply voltage

f – switching frequency

As shown from the equations above, reducing the dynamic power consumption will require a decrease in the switching frequency and/or power supply voltage.

1.2 Static Power Consumption

The primary cause of P_{static} is the leakage current, which mainly arises due to short-channel effects. Generally, static power can be calculated as:

$$P_{static} = V_{DD}\ I_{leakage}$$

However, the leakage current consists of the following components:

- reverse bias p-n junction current
- subthreshold current
- gate oxide leakage
- leakage current due to hot carrier injection from the substrate to gate oxide
- gate-induced drain leakage

Analysis of all these components in the leakage current reveals that it depends on the switching threshold voltage V_{th} and the transistor size. The mathematical representation can be presented as follows:

$$P_{leakage} = f\ (V_{DD},\ V_{th},\ W/L)$$

where:

V_{DD} – supply voltage
V_{th} – threshold voltage
W – transistor width
L – transistor length

In general, the leakage current increases with the reduction of V_{TH} and transistor size.

2. Common Techniques to Reduce Power Consumption

GreenPAK, offered by Renesas, is a broad family of cost-effective configurable mixed-signal chips which feature extremely low current consumption.

Since GreenPAK technology mostly performs tasks that rely on microcontrollers (MCUs), it is appropriate to analyze the power-saving techniques of microcontrollers. Methods to reduce the current consumption in MCUs include:

- Standby mode
- Operating clock selection
- Power supply selection
- Controlling peripheral operation

2.1 Standby Mode

Although almost all MCUs have a sleep mode, they must wait until the chip switches from power-saving mode to normal operating mode. This delay causes a lag in response and, most importantly, increases the power consumption upon wake-up. In contrast, GreenPAK devices remain powered on while in its standby mode, with all digital components active and ready to respond. All inputs are ready for any input changes with low latency, and most importantly, there are no switching losses. Additionally, the quiescent current consumption of the GreenPAK is very low, averaging 100 nA across the GreenPAK family, although some ICs in the family are even lower. This is attributed to the use of a technology node above 100 nm, resulting in low leakage currents.

2.2 Operating Clock Selection

In any MCU, the system clock can be reduced using pre-dividers to lower the operating current. During periods when the system does not need to perform any main processing, many MCUs use low-speed clocks such as 32 kHz. The GreenPAK oscillators (OSCs) have pre-dividers that allow for reduced current consumption (see Figure 3 for the GreenPAK SLG47105 high-speed OSC1). For tasks that do not require high performance, the GreenPAK ICs have a built-in low-power oscillator typically with a frequency of 2.048 kHz, which consumes only a few microamps of power (or even less). This current consumption is significantly lower than that of low-speed OSCs in MCUs.

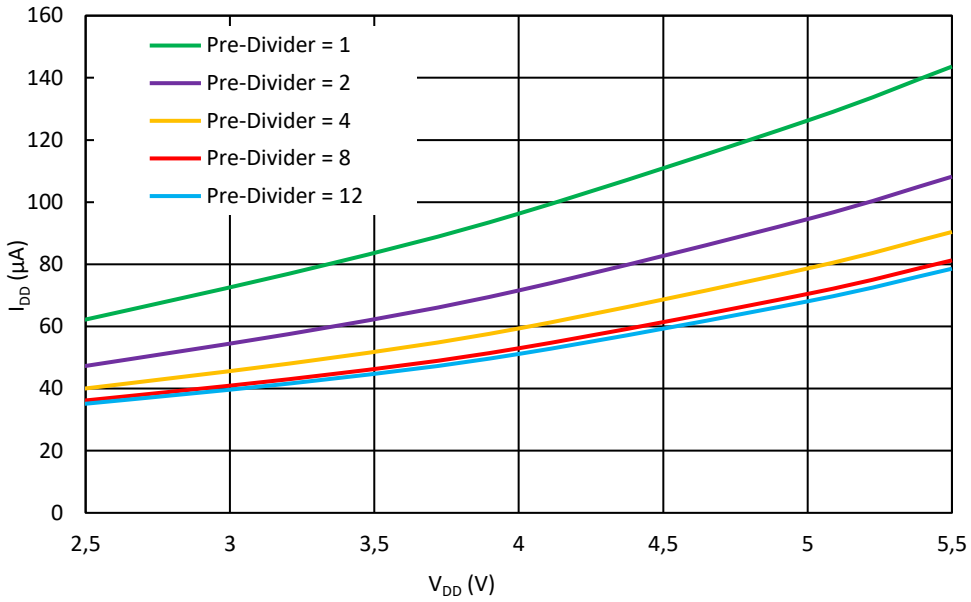

Figure 3. SLG47105 OSC1 Current Consumption vs. V_{DD} for Different Pre-dividers

2.3 Power Supply Selection

Recent trends focus on lowering the operating voltage of ICs, which, as can be seen from the equations for the power consumption, leads to a significant reduction in the current consumption. Many GreenPAK ICs can operate with as little as 1.71 V. Additionally, several low-voltage PAKs can operate from as low as 1 V. Figure 4 shows the current consumption vs. V_{DD} for the SLG47105 oscillator.

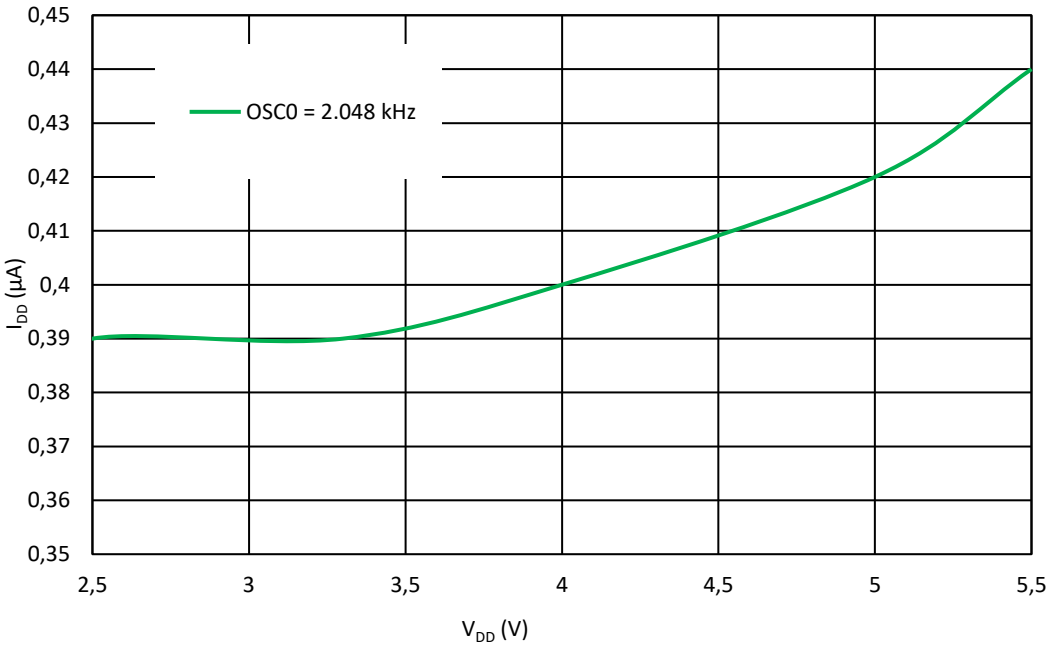

Figure 4. SLG47105 OSC0 Current Consumption vs. V_{DD}

2.4 Control Peripheral Operation

Analog blocks typically consume more power than most digital blocks due to their static power drains, such as resistors and references, which are independent of the clock rate. To save power, it is essential to deactivate any unused peripherals. In many microcontrollers, this requires enabling the clock for the specific peripheral before using it. However, certain advanced peripherals, like USB, may need a separate clock that remains active even during standby modes.

Additionally, most MCU's have a built-in watchdog timer and clock to detect if the system has frozen or stalled and then restart it if necessary. This cannot be turned off and consumes additional power.

GreenPAK ICs are not program-driven and therefore, do not freeze and do not require a watchdog. The GreenPAK offers many built-in methods to reduce the power consumption in analog blocks such as the following:

- Auto Power-On
- Low Power Blocks
- Power-Up Inputs
- Wake and Sleep Methods

2.4.1. Auto Power-On

There are "Auto Power-On" and "Force Power-On" configurations for different oscillators. An oscillator in "Auto Power-On" mode does not consume current when dedicated blocks are not active. The "Auto Power-On" configuration allows the oscillator to start with Delay blocks, Counter blocks, ADC, DCMP, and others. Figure 5 shows an example of the power savings from "OSC Auto Power-On" in the SLG46721.

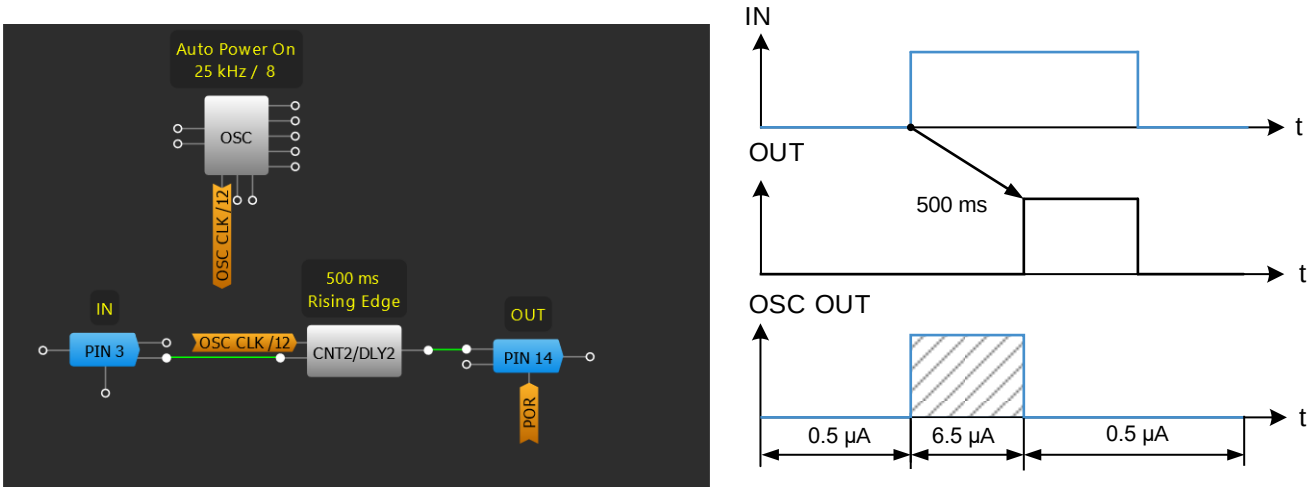

Figure 5. Example of Auto Power-On Function

2.4.2. Low Power Blocks

The most common analog blocks have a high-speed version for tasks that require high performance and a special low-power version for tasks that require reduced consumption. These low-power oscillators and analog comparators (ACMP) consume a few microamps or less of power. Figure 6 shows the current consumption for the OSC0 (low-frequency) and OSC1 (high-frequency) in GreenPAK.

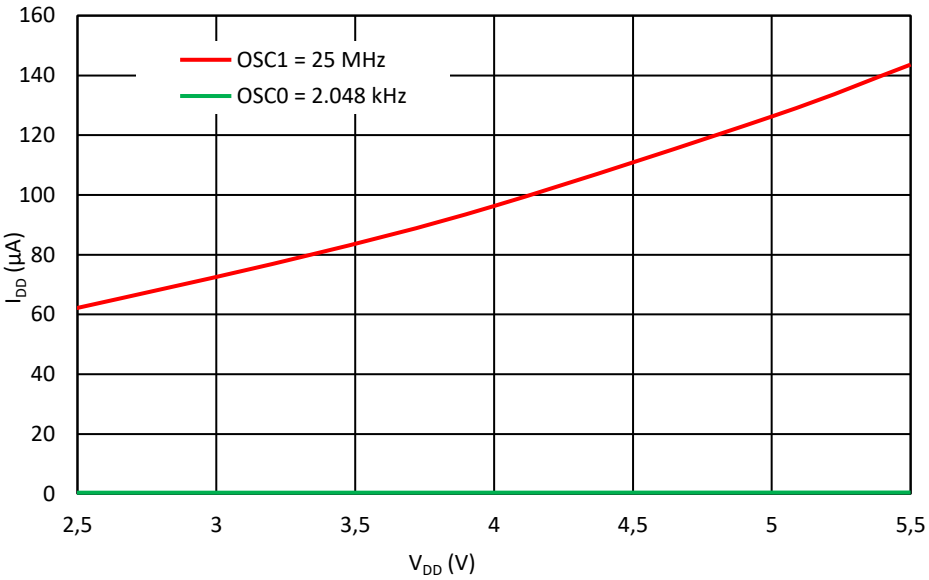

Figure 6. OSCs Current Consumption vs. VDD

2.4.3. Power-Up Inputs

Furthermore, each block can be dynamically powered on or off based on the user's needs. It is common practice to only activate the blocks when they are used within the GreenPAK. Let's use an analog comparator as an illustration of this functionality. Analog comparators, along with other analog blocks, feature a Power-Up input that enables complete deactivation of the block. When the signal is set to HIGH, the ACMP is activated. Utilizing logic, counters, or other macrocells to deactivate the ACMP can significantly reduce power consumption. For instance, if there's a need for two different voltage thresholds, the ACMP with the higher threshold can remain dormant until the lower threshold is reached. Furthermore, it's possible to deactivate the comparators using an external signal.

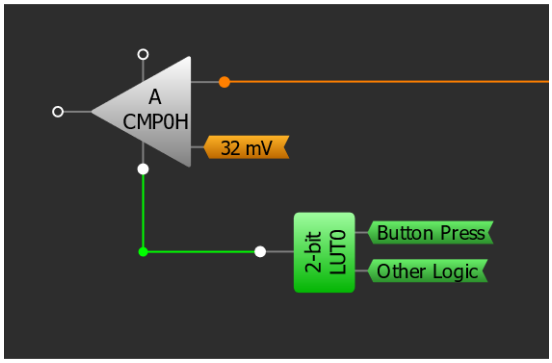

Figure 7. Power-Up Configuration Controlled by Logic

2.4.4. Wake-and-Sleep Method

Another mechanism for reducing analog comparator consumption is the wake-and-sleep method. The wake/sleep method involves periodically switching analog macrocells on and off. For some GreenPAK ICs, this function can be implemented using the WS Control block. For those that do not have this block, it can be implemented using two counters (or a single counter if there is no need to change the wake time), a D flip-flop, and an inverter. Figure 7 displays examples using these respective methods.

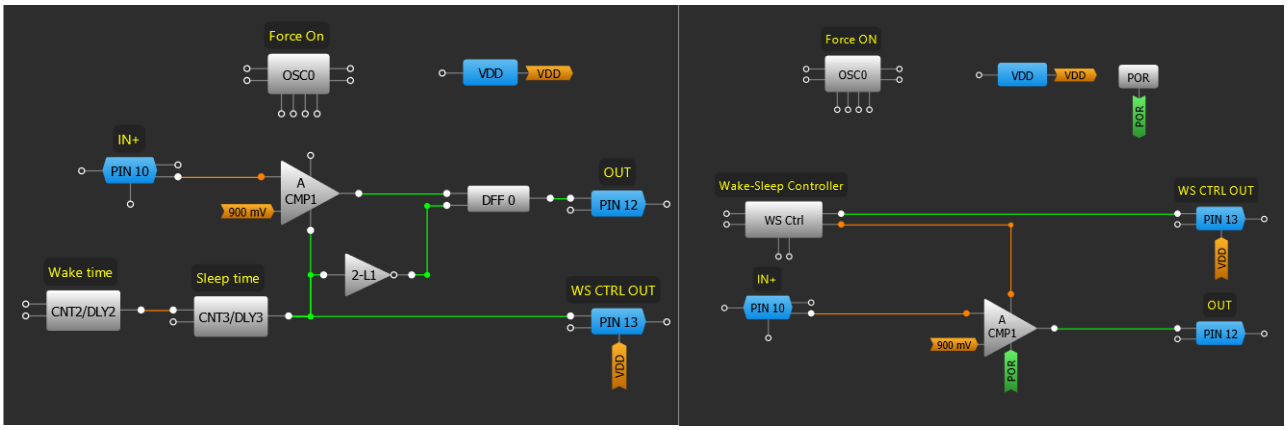

Figure 8. Wake/Sleep Control Method using Counters (left) or WS Control Block (right)

Without wake/sleep implemented, the total current consumption consists of quiescent current and analog comparator current. With wake/sleep implemented, the quiescent current can be approximated with the following equation:

$$I_{WS} = \frac{\text{System Wake}}{\text{System Wake + System Sleep}} I_{\text{without WS}} = \frac{\text{System Wake}}{\text{WS Period}} I_{\text{without WS}}$$

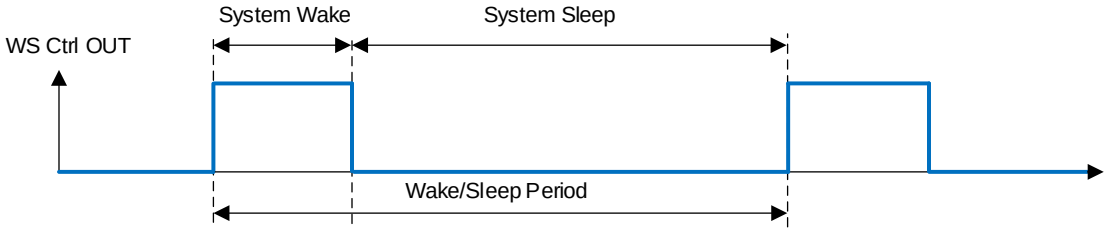

Figure 9. Behavior of Wake/Sleep

The total current with wake/sleep implemented is:

$$\text{Total Current} = I_{\text{quiescent}} + I_{OSC} + I_{\text{Wake Sleep}}$$

Conclusions

To summarize, the GreenPAK family of integrated circuits is perfectly optimized for power consumption and fits well into portable devices where power consumption is critical. GreenPAK ICs provide a compelling solution for electronic systems through their versatility, low power consumption, integrated features, cost-effectiveness, PCB space efficiency, and positive environmental impact. As the demand for energy-efficient devices continues to grow, the integration of chips like GreenPAK is expected to play a significant role in shaping the future of electronics design and contributing to a more sustainable world.

View our **GreenPAK™** page on the Renesas website to get more information.

Revision History

Revision	Date	Description
1.00	August 19, 2024	Initial release

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