Data Converters & Custom ASICs for Ubiquitous Broadband Communications

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Abstract

Our insatiable desire for on-demand data and information, wherever and whenever, continues to challenge system requirements. Developments in 5G are happening quickly and the complexity in the development of these RF systems continues to increase. Despite new demands on these measurement systems, at a top level, such systems have not changed too much. However, the performance of the data converters being used in these systems is being pushed. In this whitepaper, we examine some of the developments in converter technology to meet these broadband communication demands.

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Introduction

The growth in wireless systems infrastructure and the number of wireless devices deployed continues to grow year-on-year. Our insatiable desire for on-demand data and information – wherever and whenever – continues to challenge system requirements. Developments in 5G are happening quickly, as are increases in the number of satellites planned to enable all of this.

The complexity in the development of these RF systems continues to increase to provide end users with quicker access, guaranteed connectivity, and batteries with longer lifetimes. All this feeds back into the development of better RF communication systems.

Despite new demands on these communication systems, at a top level, such systems have not changed too much. There is an antenna to connect the radio waves with the transceiver RF chip. In the receive path, the signal is filtered and amplified to separate the desired RF signal from the other signals picked up by the antenna, and the signal is then down converted to the baseband frequencies. In the transmitter path, the signal, after being up converted, is also filtered, and amplified to drive the antenna. Typically, the data converters in the baseband chip act as the interface between the analog signals at the RF chip and the digital data processing.

The large bandwidth communication channels are required for the broadband communication between the multiple devices (edge) and the central system, either a cloud or a server. The new 5G wireless protocol is helping enable this communication. New advancements in AI (Artificial Intelligence) and Big Data provide the tools to process the data.

The decision intelligence at the device level, also called processing at the edge or edge computing, is important in an industrial environment, when fast decisions are required, and delays related to the communication latency with the central system are not acceptable.

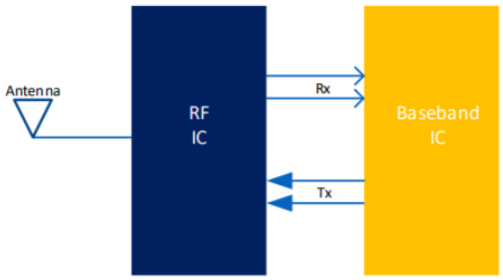


Figure 1. RF Communications Transceiver

Renesas, formerly Dialog has over 30 years' experience in developing ASIC solutions for the RF communications market. In recent white papers, we discussed Renesas, formerly Dialog's portfolio of precision and high-speed analog-to-digital converter (ADC) IP offerings. Together with Renesas, formerly Dialog's digital-to-analog converters (DACs), phase locked loops (PLLs), low dropout regulators (LDOs), references and temperature Sensors, we have the constituent building blocks for broadband communications. In this paper, we will discuss data converter design considerations for broadband communications and some example ASIC applications

ADC Architecture for Broadband Communications

When the signal bandwidth is in the order of hundreds of MHz, the data conversion is designed with sampling rates of Giga samples per second (GSps). IoT, 5G and satellite communications are some of the markets pushing for the deployment of such solutions. While the current-steering DAC architecture is still adequate to operate at such rates, the successive approximation register (SAR) ADC and the SAR-assisted pipeline ADC – which we've discussed in recent papers – typically cannot achieve these rates. A different architecture is required to meet such rates while maintaining high energy efficiency. For this application, the time-interleaved ADC is the best solution. By combining the SAR-assisted pipeline ADC core with the time-interleaved architecture, Renesas, formerly Dialog's ADC IP can extend its sampling rate to GSps with a robust, low-power and highly efficient solution. This architecture was designed to be used in broadband communication custom ASICs, as well as licensed as standalone IP for Renesas, formerly Dialog's customers to integrate into their own SoCs.

Figure 2: Satellite Communications

Inside the Time-Interleaved ADC

A time-interleaved ADC sampling at Fs (Frequency Sampling) rate is implemented with M sub-ADC cores, each one sampling sequentially at Fs/M rate. Each sub-ADC operates at M-times lower frequency, which significantly relaxes the design requirements. An accurate conversion requires each one of the sub-ADCs to be exact replicas, and the sample timing of each sub-ADC to be extremely accurate. Any mismatch or delays in the sampling time will degrade the converter performance. It is obviously impossible to guarantee mismatch-free sub-ADCs during the fabrication, so the solution to avoid the ADC performance loss is to use calibration.

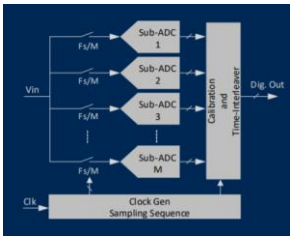
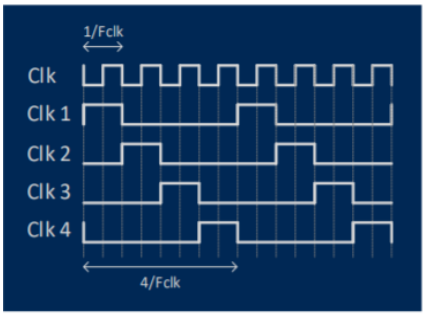


Fig.3: Time-Interleaved ADC

Using, as an example, a time-interleaved ADC implemented with 4 cores, the sample timing for each sub-ADC must follow a sequence as described in Fig.4 (on the right), where “CLK n” represents the sampling clock for the “sub-ADC n”.



In addition to the exact sequence and timing of each clock, non-overlapping on the clock phases is essential to avoid leakage, crosstalk between sub-ADCs, and performance loss. In addition to the clock skew, there are other error sources that contribute to the performance degradation of time-interleaved ADCs.

One contributor to performance degradation is offset mismatch or gain mismatch between sub-ADCs. A mismatch on these parameters creates spurs in the output spectrum which may fall within the signal bandwidth, degrading the dynamic performance.

Another source of possible performance degradation on time-interleaved ADCs is input network bandwidth mismatch between sub-ADCs. In a switched-capacitor implementation, the sampling network is typically a switch (implemented with a MOSFET) and a capacitor. The switch series resistance RON and the sampling capacitor CSAMP behave as a low-pass filter with a cut-off frequency of

$$f_C = \frac{1}{2.\pi.R_{ON}.C_{SAMP}}$$

Any mismatch in the resistance or capacitance between sub-ADCs (which is inherent to any silicon process fabrication) will also create spurs that can contribute to ADC performance loss. Each of these error sources can be considered separately using a model of the sub-ADC, as the one shown in Fig.4.

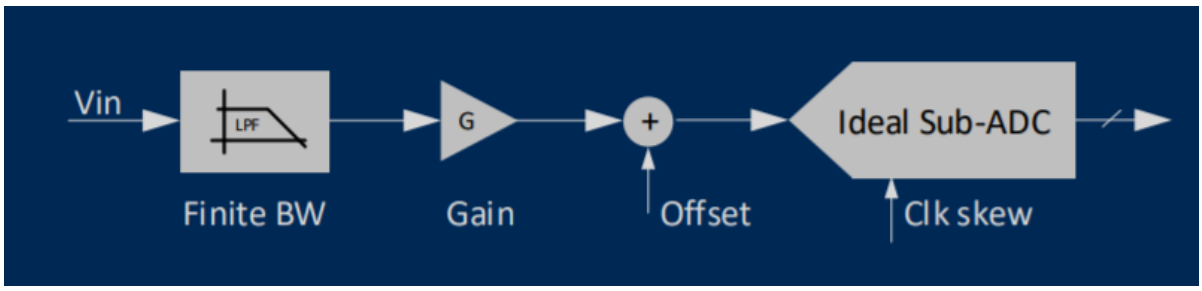


Figure 5: Time-interleaved sub-ADC model including non-idealities

The power and frequency location of the spurs generated from all these effects depend on several parameters including the level of mismatches between the sub-ADCs and the number of cores. A time-interleaved ADC with M sub-ADC cores and input clock frequency f_{CLK}, has each sub-ADC sampling at f_{CLK}/M rate. When the input signal is a sinewave with frequency f_{IN},

- an offset mismatch between the sub-ADCs creates spurs at

$$\frac{f_{CLK}}{M}.k; \qquad k: 1; 2; \dots; M\ 1\ (integer)$$

- a gain mismatch, bandwidth mismatch or clock skew create spurs at

$$\frac{f_{CLK}}{M}.k \pm f_{IN}; \qquad k: 1; 2; \dots; M\ 1\ (integer)$$

Fig.6 shows an example of a time-interleaved ADC's digital output spectrum with (top) and without (bottom) sub-ADC offset and gain mismatch related spurs. In this example, the input signal is a sinewave of 180MHz and the ADC, sampling at 424MSps, is implemented with 3 cores; each sub-ADC has a sampling rate of 424MSps/3 = 141.3MSps.

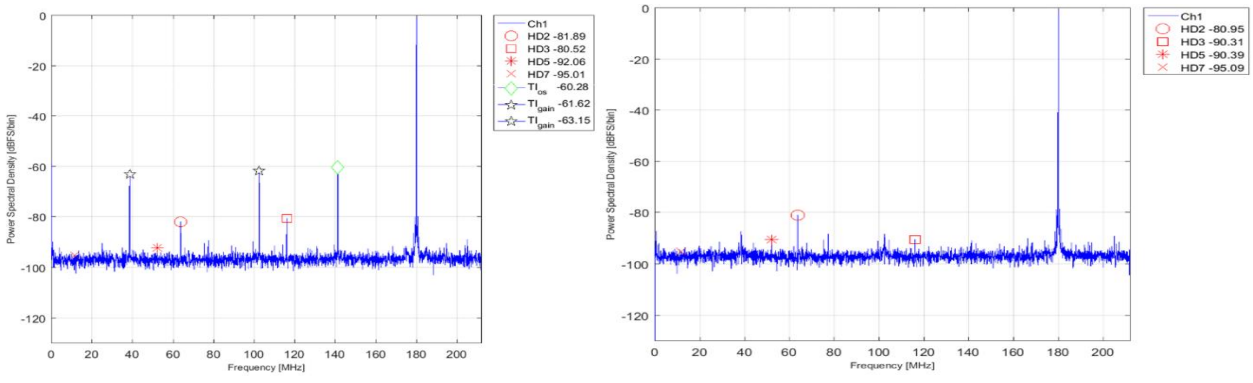


Fig.6: ADC Digital Output Spectrum of Sinewave with (left) and without (right) time-interleaved sub-ADC offset and gain mismatches

(Note: the left and right spectrums are from different samples.)

The offset mismatch between the sub-ADCs creates spurs at 424MHz/3 = 141.3MHz and 424MHz/3*2 = 282.6MHz (which folds back to 141.3MHz in the spectrum).

The gain mismatch between the sub-ADCs creates spurs at 424MHz/3 ± 180MHz and 424MHz/3*2 ± 180MHz. In these plots, two of these are located at 38.7MHz and two at 102.7MHz.

When these mismatches are not calibrated, the performance of the converted sinewave in this single-tone test is clearly degraded. The spurious-free dynamic range (SFDR) in the top spectrum is limited by the time-interleaved related spurs to about 60dB, while the SFDR in the bottom spectrum, where there are no such spurs, is better than 80dB.

When converting broadband signals with time-interleaved ADCs, an accurate and efficient conversion is only possible with an optimized and robust calibration. Performance, cost, and power all depend on how good this calibration is. Fig.7 shows the high-level block diagram of Renesas, formerly Dialog's time-interleaved ADC.

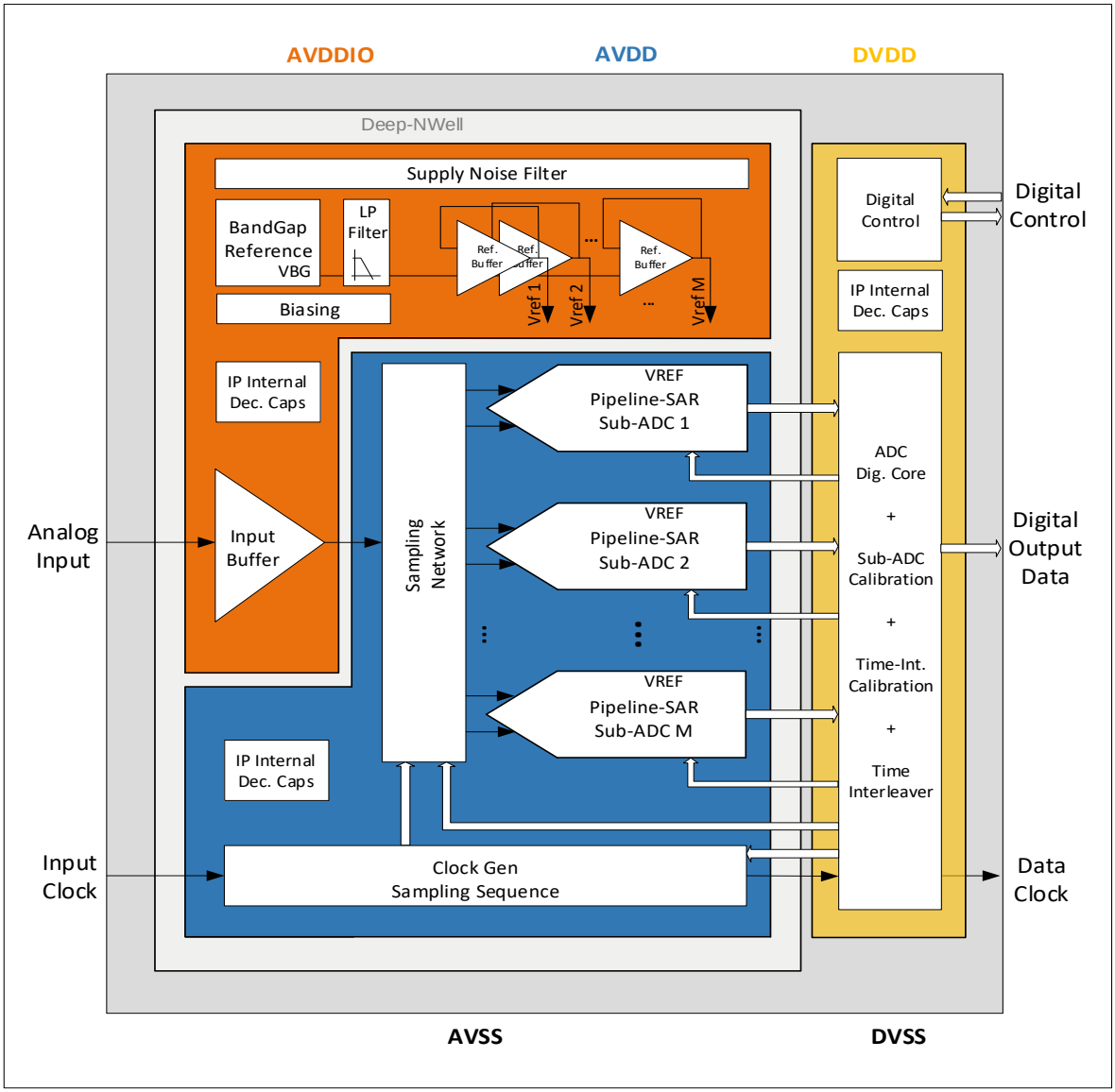


Fig.7: Time-interleaved ADC block diagram

The sub-ADCs are designed with a SAR-assisted pipeline ADC, the architecture discussed in a recent paper and shown in Fig.8. The power domain's floorplan, noise isolation, analog-digital breakdown, etc. are all designed with a similar approach as for the SAR-assisted pipeline ADC itself. The time-interleaved calibration is an additional calibration layer which is implemented both on the digital and analog domains, with a digital algorithm measuring and correcting the sub-ADC mismatches and feeding information back to the analog domain at the input sampling network for timing skew equalization for each sub-ADC. The calibration algorithm, operating in the background, works with any broadband signal and does not require any pilot signals or calibration vectors.

An additional block included in this broadband ADC is the input buffer. In the block diagram in Fig.7, the input buffer is supplied with AVDDIO to interface with RF chips with output common-mode voltage at AVDDIO/2, but other options are also possible.

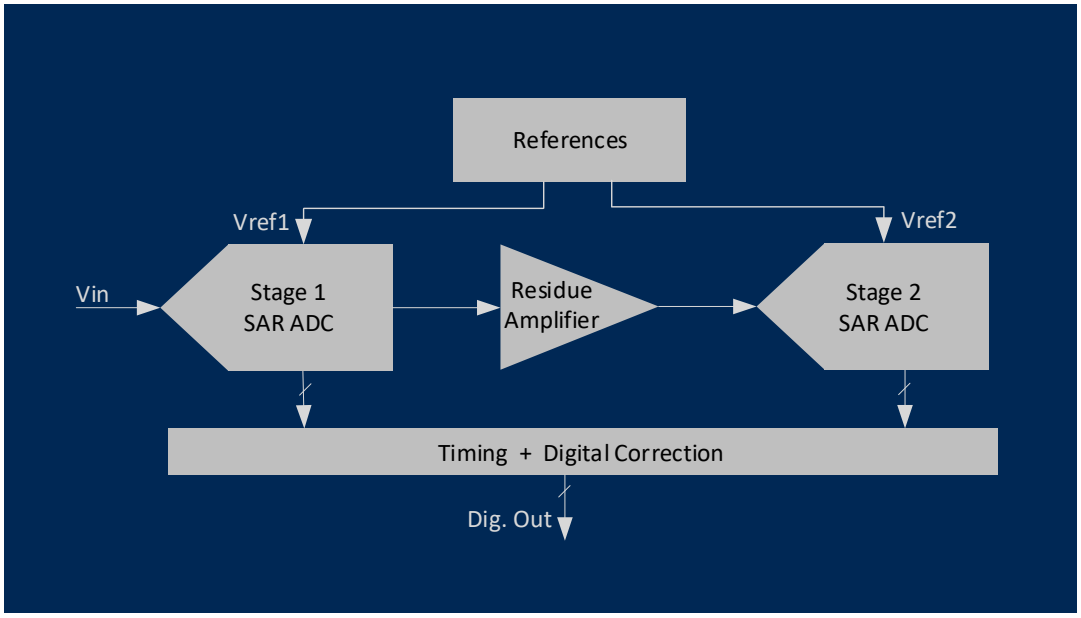
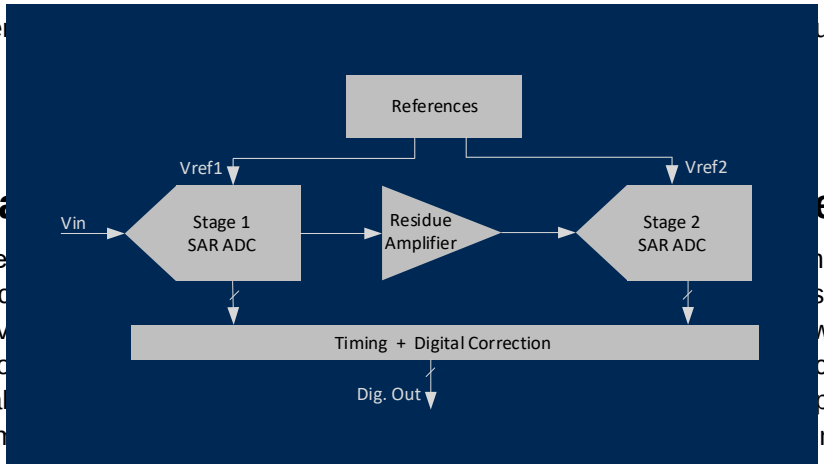


Fig.8: Sub-ADC implemented with SAR-assisted pipeline architecture

When the filte ut buffer may be skipped, and the last stage



Performa ers

Data converte nput sinewave. A sinewave is simple to spec s easy to generate both in the simulation env with such stimulus like Signal-to-Noise Ratio c Range (SFDR). In a typical test, a full-scal present at the converter input, and the dynam metrics above.

However, for broadband signals, this test is less suitable to determine if the converter has adequate performance for the system requirements. While a single tone has all its power in a single frequency, in a broadband signal the power is spread over a large bandwidth. Therefore, to avoid saturation in the signal path channel, the signal spectral density must be lower than the one with a single tone. This change in the signal spectrum corresponds to a change in the converter requirements which must be considered when designing an optimized ADC or DAC (power and area) while still meeting the performance required for the overall solution.

Clock jitter is an example of a parameter which can be incorrectly specified if the right test methodology is not used. ADC clock jitter increases the system noise and contributes to the loss of performance. The theoretical SNR of an ADC when limited by jitter only is given by

$$SNR_{dB} = -20.LOG_{10}(2.\pi.f_{IN}.t_J)$$

where f_{IN} is the input sinewave frequency and t_J is the clock jitter.

Fig.9 shows the SNR_{dB} vs f_{IN} curves for several jitter levels.

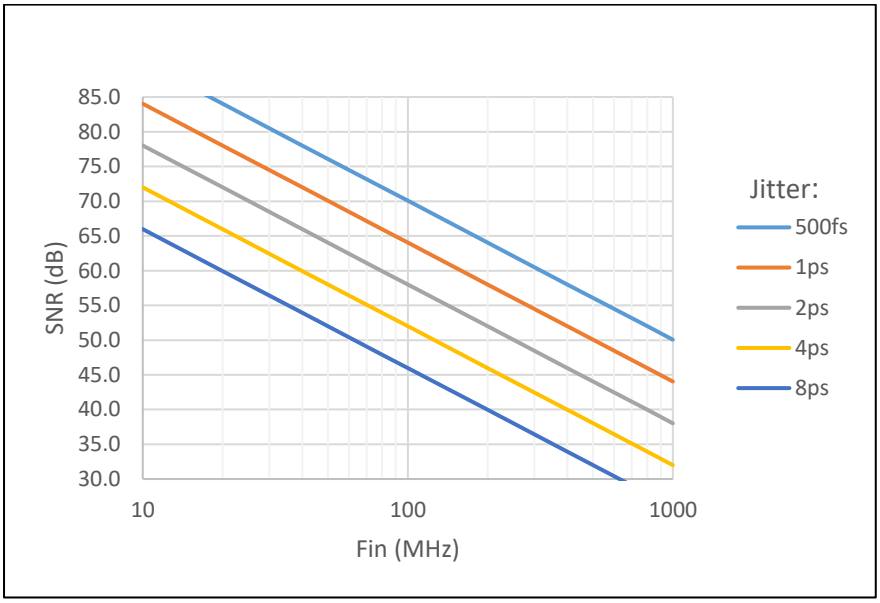


Fig.9: ADC SNR_{dB} vs f_{IN} for different clock jitter levels

Considering, for example, a 1psrms clock jitter and a sinewave with frequency at or higher than 300MHz, the performance is always below 55dB SNR even without any other error or noise sources. For high-performance systems, this would require highly challenging and expensive clock references. The power of a broadband signal is spread over a large bandwidth with a spectral density quite different from a spectral density of a single tone. This can significantly relax the clock reference jitter requirements and result in a lower power and more efficient solution.

For some communications systems, other data converter parameters can also be relaxed when we consider a test stimulus closer to a real communications signal. This means a less expensive and lower-power solution without any performance loss for the overall solution.

Multi-tone power ratio (MTPR) or noise-power ratio (NPR) tests can be used to measure the performance of data converters using a broadband input signal. These parameters are measured by removing the signal power in a few frequency bins within the signal bandwidth and measuring the power ratio between non-empty and empty bins. In addition to noise, the empty bins at the converter output will also have some intermodulation components resulting from the converter nonlinearity.

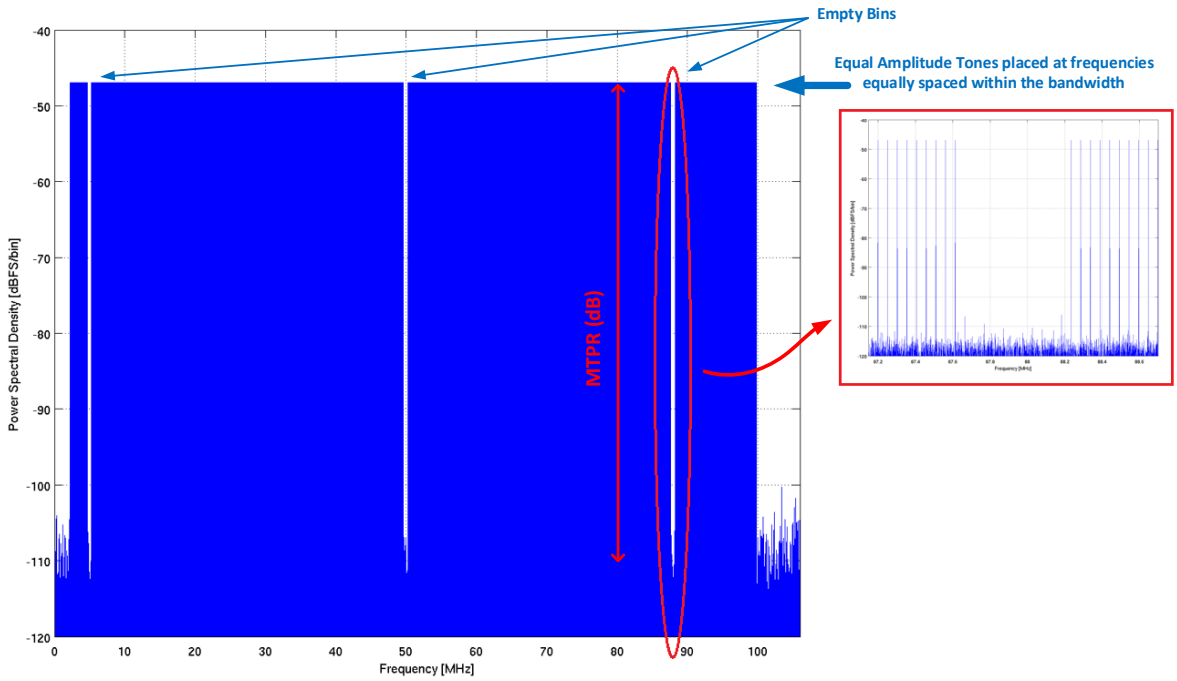


Fig.10: MTPR measurement

Fixed Wireless Access

Fixed wireless access (FWA) provides broadband data communication, performed between fixed locations. For example, in the “curb-to-the-home” scenario, it replaces the need for new fibre-line and copper installation costs, by providing a radio link as the connection method. Fixed wireless access is seen as a cheaper and more practical solution in the roll-out of broadband to the many locations, providing better coverage at lower cost, when compared to new fibre or copper rollout. The equipment is usually located high up, on the roofs of building etc., to ensure there is no obstruction in the transmission.

Renesas, formerly Dialog recently worked on the development of a custom ASIC for a fixed wireless access application. The custom chip was the interface between the RF transceiver and the baseband processor, in an implementation where three chips were used for the complete signal path.

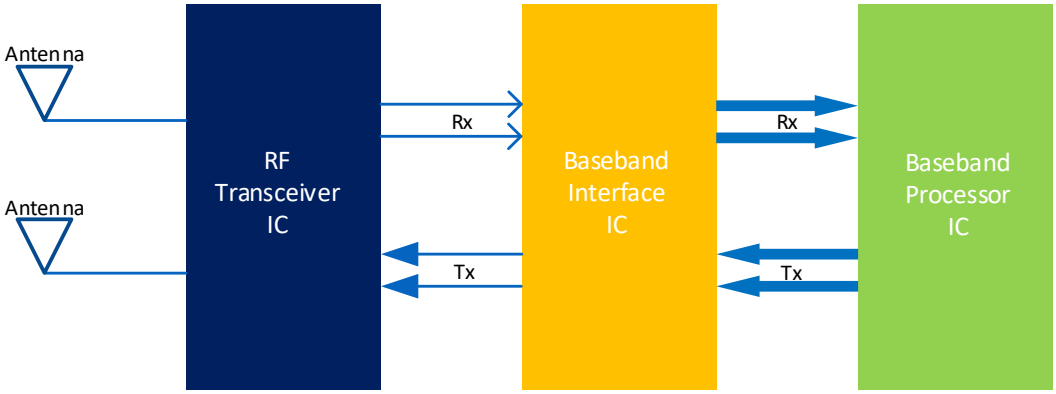


Fig.11: Fixed wireless access system

The baseband interface chip incorporated silicon proven ADC and DAC IP along with additional externally licensed JESD204B/C IP. The complex integration of all these functions was implemented using standard CMOS technology.

The data converters used in the data path interface were implemented with a quadrature current-steering DAC sampling at 360MSps (Tx-Path) and a quadrature SAR-assisted pipeline ADC sampling at 160MSps (Rx-Path). The SAR-assisted pipeline ADC technology, which was discussed in detail in a recent paper, fits perfectly this architecture, minimizing the complexity and costs of the complete solution.

The successful design leveraged a multi-disciplinary team with many combined years of FWA communications systems knowledge.

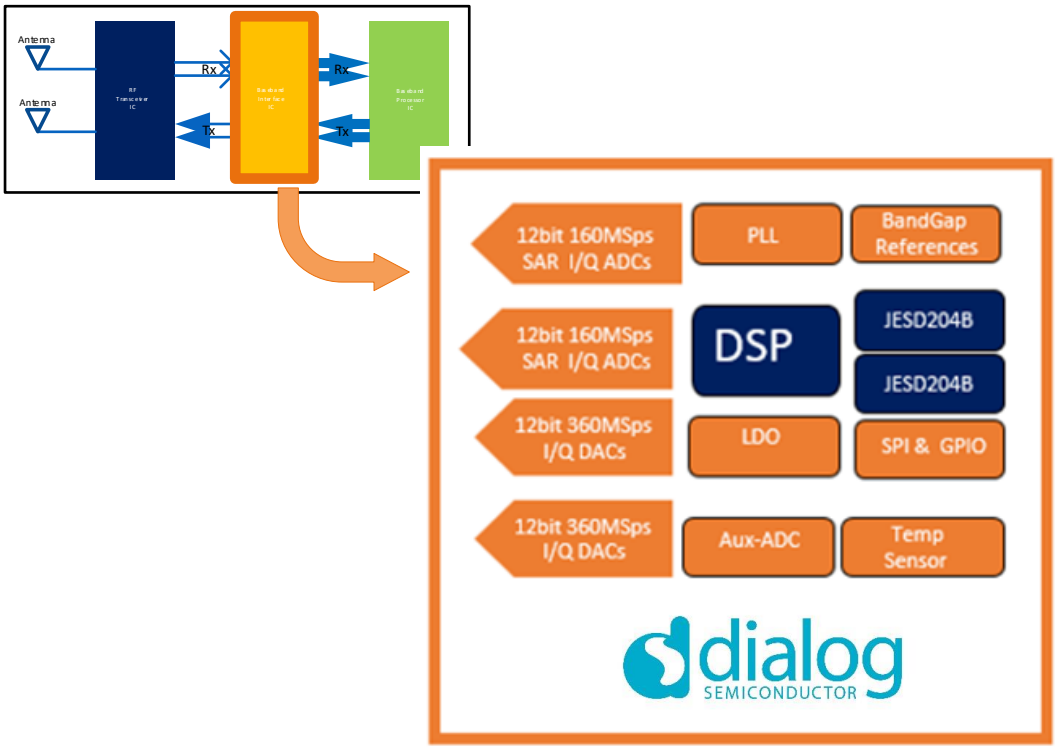


Fig.12: Baseband interface ASIC for fixed wireless access system

Not just RF - Ultra-Fast Broadband over Copper Lines with G.Fast

G.Fast is an ultrafast broadband technology that can deliver download speeds of over 100Mb/s. Typically it is used over the existing copper infrastructure that is already likely in place, and therefore can provide upgraded ultrafast broadband t. G.Fast is aimed at local loops shorter than 500m and therefore is an excellent opportunity for bringing high-speed internet to many locations.

Fig.13 shows the block diagram of an Analog Front End (AFE) designed by Renesas, formerly Dialog for a G.Fast modem.

The data converters sample the signal at 424MSps; the ADC is implemented with a time-interleaved architecture and the DAC is a current-steering architecture. With a broadband signal of 212MHz, the converters' performance is around 52dB MTPR.

The receive path also includes a power gain amplifier (PGA) with a wide range programmable gain and a low-pass filter. The transmit path includes an amplifier to drive the line. The complete AFE includes voltage generation and regulation and

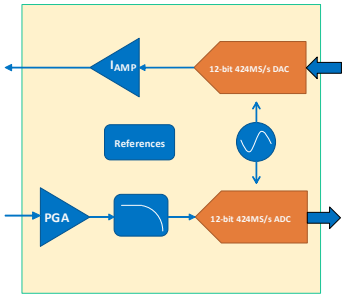


Fig.13: AFE for G.Fast technology

timing and clock generation, in addition to several other auxiliary blocks.

Conclusions

Regardless of whether the transport mechanism to deliver broadband is wireless or wireline, the common need is for increased coverage and capacity. This translates to higher-sample rate data-converters. Time interleaved ADCs and SAR-assisted pipeline ADCs are providing the data rates necessary to service these requirements. With the future demand for 5G radios wireless communication, data rates will be faster than 1Gb/s. mmWave bands, MIMO (multiple-input, multiple-output) antenna technology and ultra-fast silicon technologies are making this a reality.

Once again, data converter technology will be under pressure to extend its maximum bandwidth without losing performance or energy efficiency. Regardless of these demands, Renesas will be at the forefront of meeting these requirements, developing the ADC and DAC IP to support your next design or for use in a custom ASIC to meet these market conditions.

Revision History

Revision	Date	Description
1.0	Apr 03, 2020	Initial release.
1.1	Dec 22, 2021	Rebrand