

Image Processing for Vision AI

Takaaki Suezawa, Enterprise Infrastructure Solutions Business Division, IoT and Infrastructure Business Unit, Renesas Electronics Corporation

Overview

Recent years have seen an increasing need for Vision AI applications using AI to enable real-time image recognition. Vision AI, which substitutes AI for human visual recognition, requires optimal image processing.

Renesas has released RZ/V2M as mid-class, and RZ/V2L as an entry class, Vision AI microprocessors (MPUs). Both products are equipped with DRP-AI which is Dynamically Reconfigurable Processor for AI inference. DRP-AI is an AI accelerator highly rated for its superior power efficiency, providing optimal image processing for Vision AI. RZ/V2M is equipped with a dedicated hardware ISP (Image Signal Processor) which is tuned to match the unique characteristics of the Renesas-selected CMOS sensor. Optimal image quality is realized using easy to use API without requiring CMOS sensor tuning by the end user. With RZ/V2L, DRP-AI can be used for AI inference processing as well as a broad range of image processing, taking advantage of its characteristic DRP flexibility. We illustrate this with a description of Simple ISP function.

DRP: Dynamically Reconfigurable Processor – Renesas proprietary hardware that executes applications while dynamically switching connections between arithmetic units.

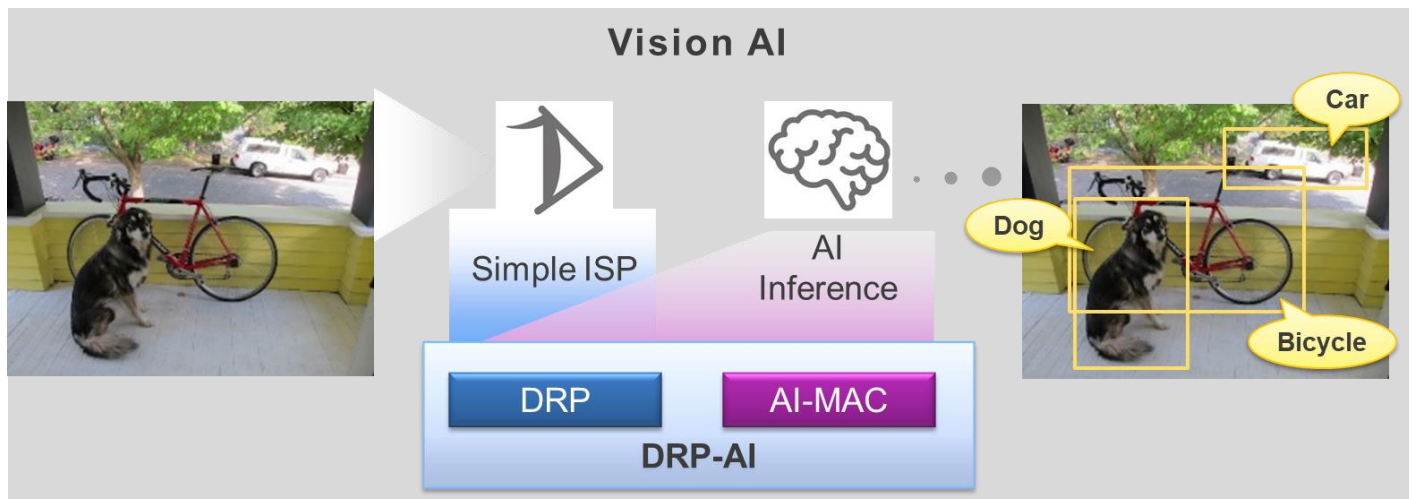


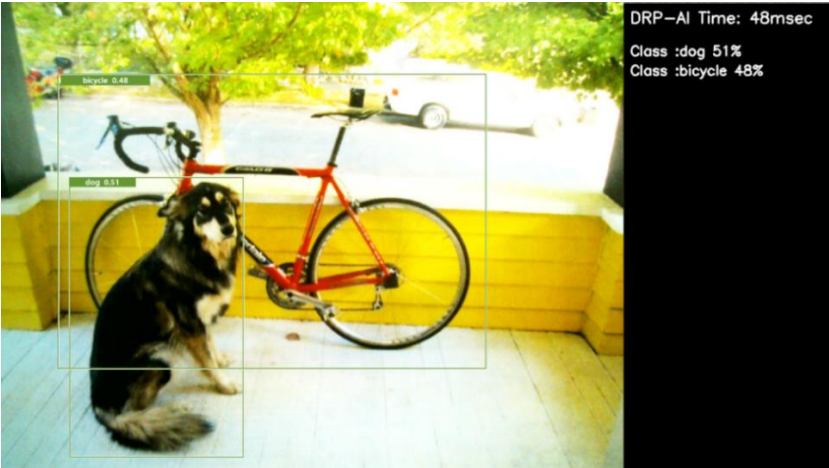

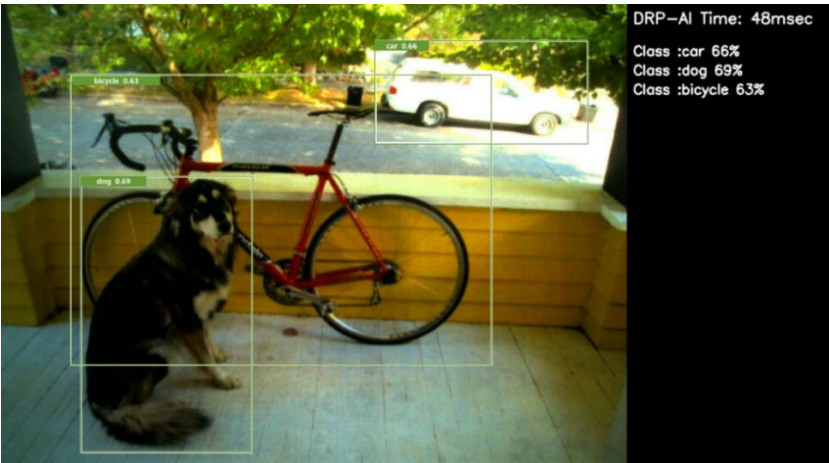
Figure 1: Vision AI realized with DRP-AI

Introduction

This white paper introduces Simple ISP, its features, and the software and image quality adjustment procedures provided by Renesas.

Image preprocessing and AI inference:

Simple ISP curbs the environmental impact of the target image while enabling a stable AI inference outcome. The following image is an AI inference execution resulting from implementation of TinyYOLOv2. Simple ISP exposure control (feedback control to the camera) results in subdued brightness of the overall image. Although objects remain undetected prior to brightness correction (Figure 2), they are clearly identified (car) following brightness correction (Figure 3).

<p>Before brightness correction: High brightness inhibits recognition of outdoor objects</p>  <p style="text-align: center;">Figure 2: AI Inference in Image Before Brightness Correction</p>	<p>AI inference results</p> <p>Dog: 51%</p> <p>Bicycle: 48%</p>
<p>After brightness correction: </p> <p>Brightness correction enables recognition of outdoor objects (car)</p>  <p style="text-align: center;">Figure 3: AI Inference in Image After Brightness Correction</p>	<p>AI inference results</p> <p>Car: 66%</p> <p>Dog: 69%</p> <p>Bicycle: 63%</p>

Cost Optimization: Realizing Image Processing for Vision AI Without an External ISP

Simple ISP incorporates all basic functions required of ISP, while allowing inexpensive CMOS sensors without dedicated ISP hardware, significantly reducing system costs. Simple ISP supports Bayer RGB RAW (RAW8/RAW10/RAW12) as the input image format, enabling connection with most CMOS sensors on the market.

Simple ISP functions:

- Input image format Bayer RGB RAW(RGGB) RAW8/RAW10/RAW12
- Input resolution 5MP (2592*1944) max
- Output image format YUYV/UYYV/RGB888/ARGB8888
- Input signal level correction Black level, digital gain
- Demosaicing APCI Method version
- Color correction 3x3 color matrix color correction
- 2D noise reduction Median filter for 2D noise removal
- 3D noise reduction Noise removal between frames
- Edge enhancement Laplacian filter to highlight edges
- Gamma correction Gamma correction by user-specified LUT
- Exposure control Automatic/manual
- White balance control Automatic*/manual
- Performance (frame rate) 30fps @HD (1280x720)

*Under development

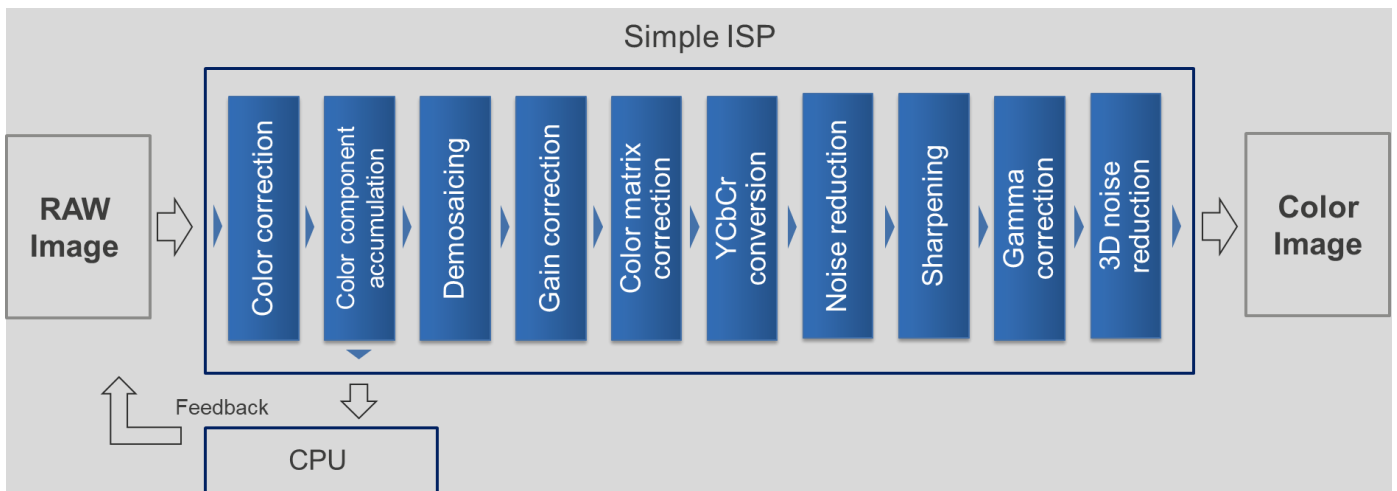


Figure 4: Simple ISP Function Block

Ease of Use: V4L2 Interface Compatibility Simplifies OSS and Design Asset Diversion

The RZ/V series offers Linux BSP as a software development environment, and the Linux system’s V4L2 (Video for Linux version 2) supports Simple ISP. This makes it easy for users to divert various OSS (Open Source Software) that use the V4L2 interface as well as existing user applications.

V4L2 API:

V4L2 interface allows the user to determine settings and controls for Simple ISP. Defining “VIDIOC_S_EXT_CTRL” as the extended API and setting Simple ISP parameters enables image quality adjustments according to the application.

System call	Summary
open	Open a V4L2 device file.
close	Close a V4L2 device file.
ioctl	Issue V4L2 API for the opened device file.
select	Check if DQBUF can be executed.
mmap	Map a buffer in user space.
munmap	Unmap a buffer in user space.
ioctl(VIDIOC_S_FMT)	Specify the data format.
ioctl(VIDIOC_REQBUFS)	Request a buffer area.
ioctl(VIDIOC_QUERYBUF)	Query the status of a buffer.
ioctl(VIDIOC_QBUF)	Register a buffer.
ioctl(VIDIOC_DQBUF)	Release a buffer.
ioctl(VIDIOC_STREAMON)	Start streaming.
ioctl(VIDIOC_STREAMOFF)	Stop streaming.
ioctl(VIDIOC_S_EXT_CTRL)	Setting value of extended control

Table 1: V4L2 APIs

Simple ISP parameter settings:

Table 2 lists Simple ISP parameter settings.

White level (No. 2) and **Setting of color matrix** (No. 4) define typical setting values as the preset values. Moreover, **Setting of all parameters** (No. 0) allows for even more minute adjustments. For further details concerning **Setting of all parameters** (No. 0), refer to [Simple ISP User’s Manual](#) on the Renesas website.

No.	Specification	Range of values	Parameter of function argument	
			Control ID	Control class
0	Setting of all parameters	-	V4L2_CID_RZ_ISP_ALL	See. User's Manual
1	Adjustment value of black level	0 through +127 Default:0	V4L2_CID_RZ_ISP_BL	0 through 127 Default:0
2	Adjustment value of white level	0: Day light 1: Neutral light 2: Interior light 3: Lamp light Default:1	V4L2_CID_RZ_ISP_WB	V4L2_RZ_ISP_WB_DAYLIGHT V4L2_RZ_ISP_WB_HORIZON V4L2_RZ_ISP_WB_WHITE V4L2_RZ_ISP_WB_STUDIO_LAMP
3	Setting of gamma value	1 through 9999 Default:100(mean 1.00)	V4L2_CID_RZ_ISP_GAMMA	1 through 9999
4	Setting of color matrix	0: Original 1: Standard correction 2: Vivid correction 3: Sepia correction Default:1	V4L2_CID_RZ_ISP_CMX	V4L2_RZ_ISP_CMX_NONE V4L2_RZ_ISP_CMX_NORMAL V4L2_RZ_ISP_CMX_VIVID V4L2_RZ_ISP_CMX_SEPIA
5	2D noise reduction	0 through 100 Default:100	V4L2_CID_RZ_ISP_2DNR	0 through 100
6	3D noise reduction	0: OFF 1: ON Default:1	V4L2_CID_RZ_ISP_3DNR	0 or 1
7	Unsharp Mask	0: OFF 1: WEAK 2: NORMAL 3: STRONG Default:0	V4L2_CID_RZ_ISP_EMP	V4L2_RZ_ISP_EMP_NONE V4L2_RZ_ISP_EMP_WEAK V4L2_RZ_ISP_EMP_NORMAL V4L2_RZ_ISP_EMP_STRONG
8	AE ON/OFF	0: OFF 1: ON Default:0	V4L2_CID_RZ_ISP_AE	0 or 1
9	Expose level	-40 through 40(dB) Default: 0dB	V4L2_CID_RZ_ISP_EXPOSE_LV	-40 through 40
10	Target brightness (8-bit range)	1 through 254 Default: 128	V4L2_CID_RZ_ISP_T_BL	1 through 254
11	Brightness threshold	1 through 64 Default: 10	V4L2_CID_RZ_ISP_THRESHOLD	1 through 64

Table 2: Setting Parameters Definitions for all Functions

Flexibility: Source Codes Provided for all Software Including Simple ISP Control Software

All software has been made available through source codes. Users can adjust the camera control to suit their application and make necessary software changes when changing CMOS sensors. The Simple ISP parameter adjustment environment is also included as sample application software. This environment allows users to extract appropriate Simple ISP parameters to tune images based on the characteristics of the CMOS sensor.

Software configuration:

- Renesas software packages are configured with device drivers for peripheral functions, middleware (OSS such as V4L2, Wayland, etc.), and a sample application that conducts image capture using Simple ISP. As all software is provided in source code, users can make additional modifications such as changes to the camera drive and changes/additions to camera feedback control (discussed below) when selecting and assessing the CMOS sensor. For detailed information concerning RZ/V2L hardware, refer to the RZ/V2L Hardware User’s Manual.

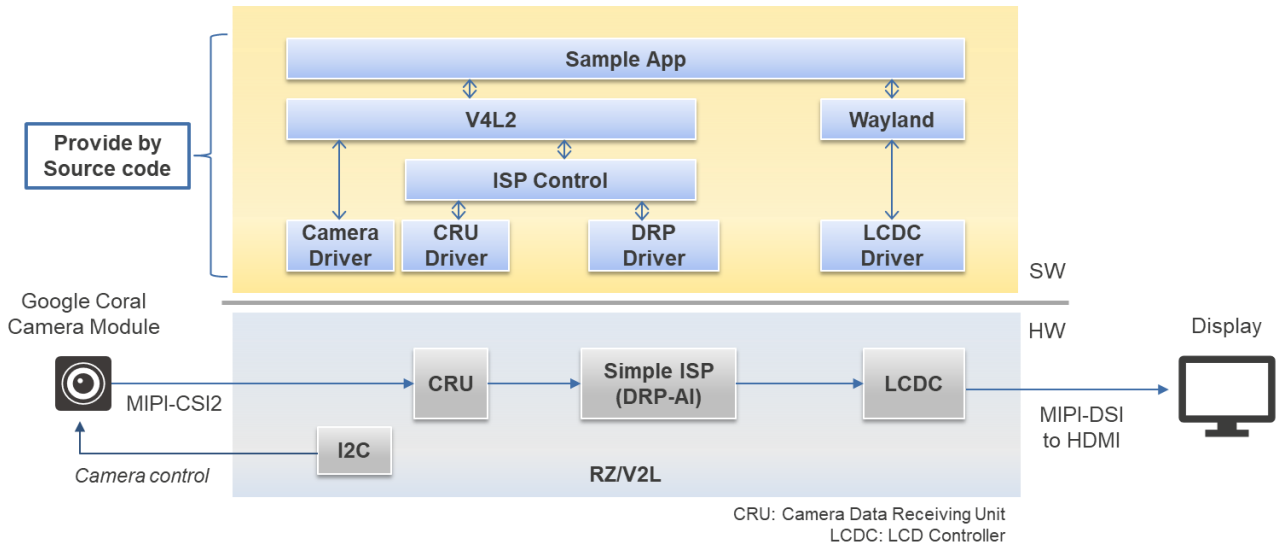


Figure 5: System Configuration

Camera feedback controls are based on the integrated luminance value of the input image extracted by Simple ISP, allowing camera brightness to be controlled by adjusting gain and shutter speed. This processing is implemented within the ISP Control. The range of gain and shutter speed settings, as well as resolution, will differ for each camera.

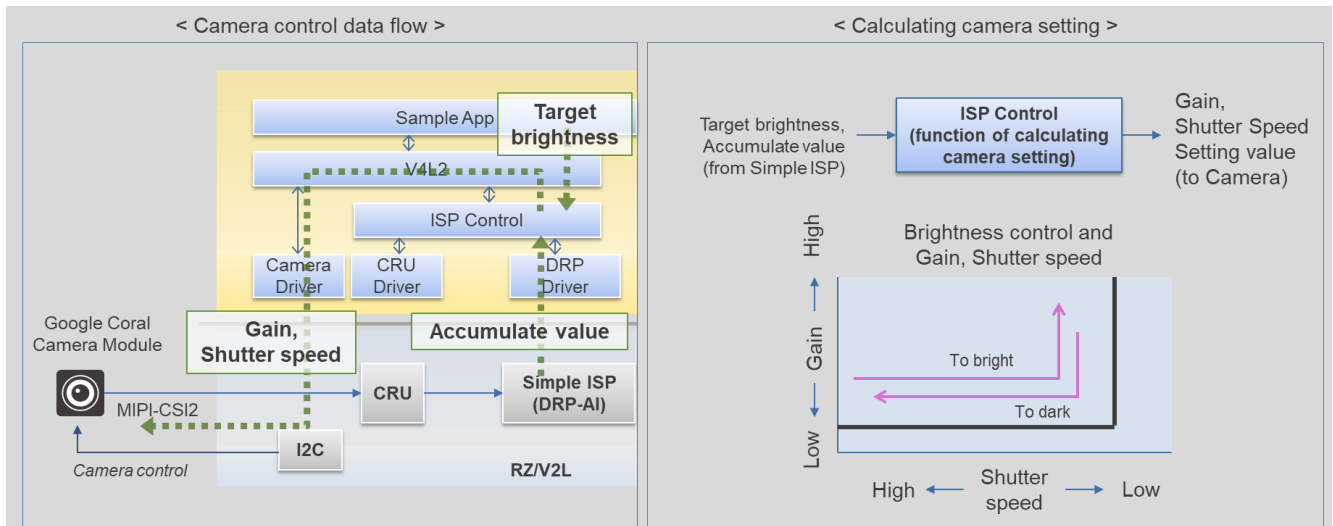


Figure 6: Camera Controls

Environment for adjusting image quality:

The following explains the steps required to set white balance and gamma correction, two of Simple ISP's image adjustment parameters. The description assumes usage of sample application software packaged with ISP Software Package V1.00.

Implement the following steps to change the image quality adjustment parameters of Simple ISP and adjust quality while viewing the image displayed on your screen.

1. Execute sample application "sample_app_cam."
2. Edit the Simple ISP parameter setting file (text) to change the setting value.
Reference: Default setting and sample setting (color inversion) text are included in the ISP Support Package.
3. Send the file edited in Step 2 (above) from the terminal software to the board.

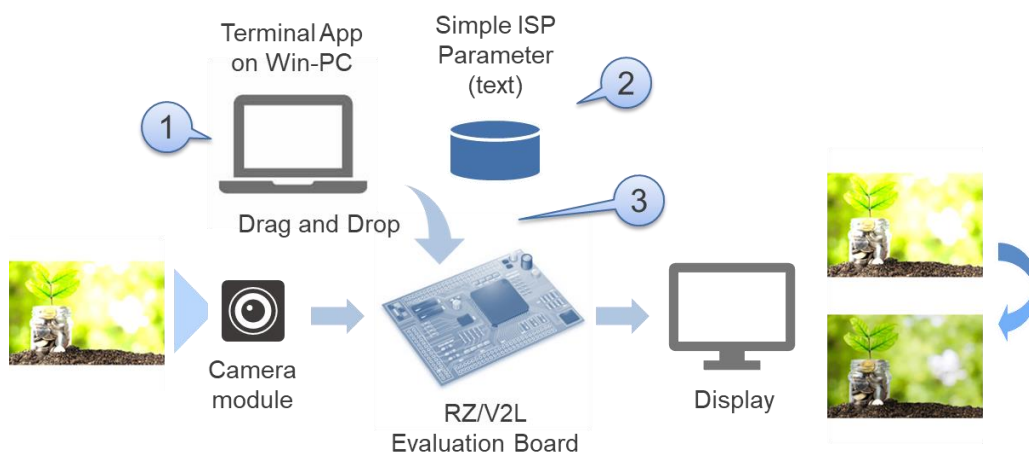
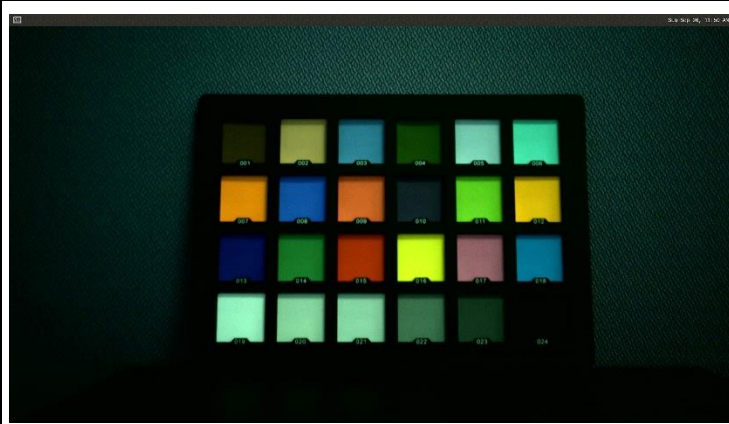


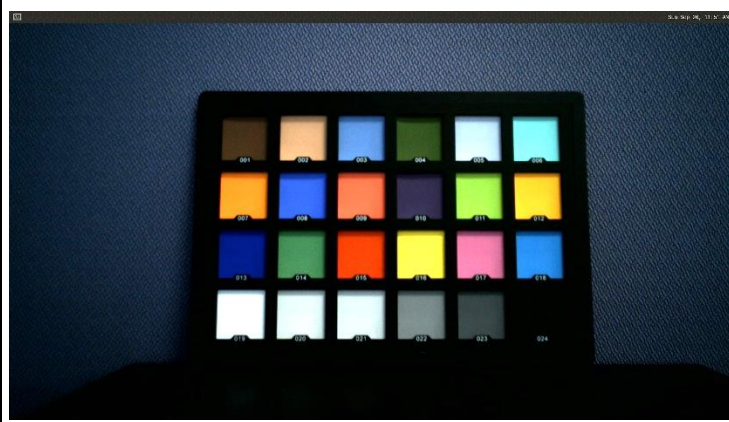
Figure 7: Image Quality Adjustment Procedure

Below, note the sample setting changes for two Simple ISP parameter settings – **Color matrix correction** (Table 2 No.4) and **Gamma correction** (Table 2 No.3).

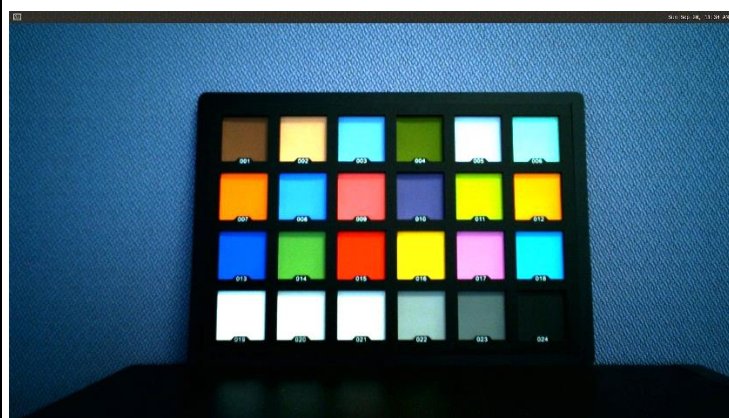
Table 3: Color matrix correction



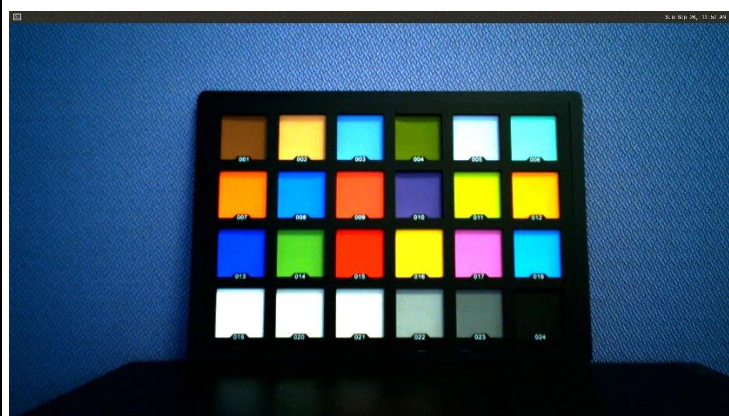
Color matrix setting: no correction
(no input gain correction)



Color matrix setting
0: Original (no correction)



Color matrix setting
1. Standard correction
(standard setting)



Color matrix setting
2: Vivid correction
(vivid)

Table 3: Color matrix correction

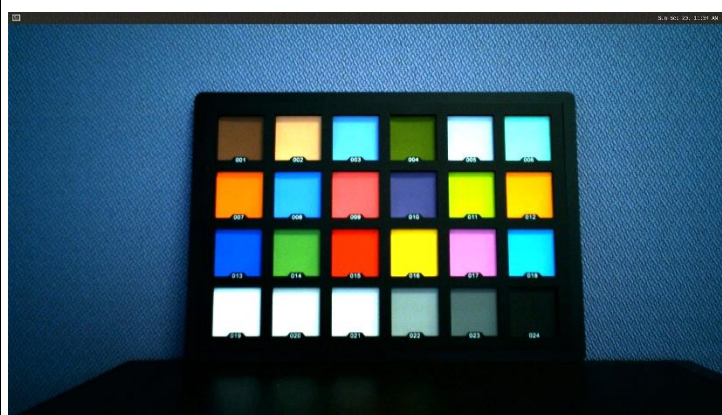
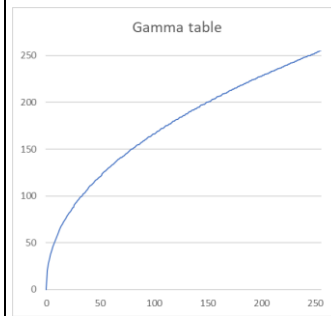


Color matrix setting
3: Sepia correction
(sepia)

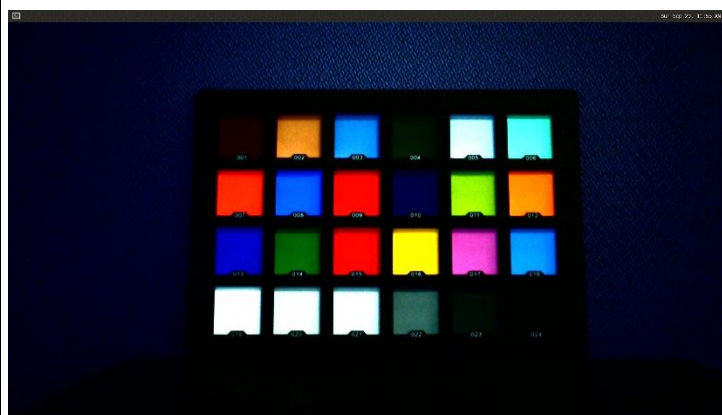
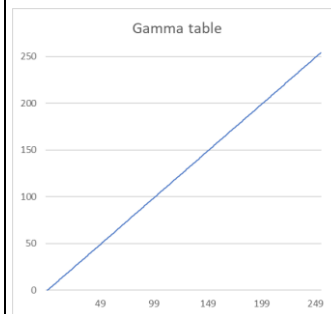
Table 4: Gamma correction



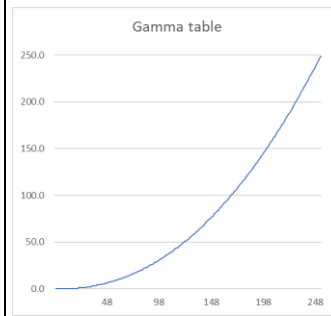
Gamma:1/2.2



Gamma:1



Gamma:2.2



Easy to Start: Complimentary BSP and Sample Application Software Available on the Web

Renesas provides the RZ/V2L Evaluation Kit with the camera module as well as free software to enable users to begin development immediately. Documents and sample software can be downloaded easily from the [RZ/V2L Website](#).

- Various manuals
- Application notes
- Software (Linux Package, DRP-AI Support Package, ISP Support Package)

HW	Evaluation board Kit for RZ/V2L MPU <ul style="list-style-type: none"> - SMARC Module Board - SMARC Carrier Board - MIPI-Camera Module
SW	RZ/V Verified Linux Package <ul style="list-style-type: none"> - Linux Kernel - Device Driver
	RZ/V2L ISP Support Package <ul style="list-style-type: none"> - Simple ISP Sample Application - Simple ISP User's Manual
	RZ/V2L DRP-AI Support Package <ul style="list-style-type: none"> - DRP-AI Sample Application - AI Evaluation Software - AI Implementation Guide
	RZ MPU Graphics Library Evaluation Version for RZ/G2L and RZ/G2LC
	RZ MPU Video Codec Library Evaluation Version for RZ/G2L
Tool	DRP-AI Translator

Table 5: RZ/V2L Development Environment

Summary

The Renesas RZ/V2L offers not only DRP-AI for AI inference execution, but also optimal imaging for Vision AI. The key points are summarized below.

- Stable AI inference obtained by suppressing the environmental effects on the target image
- Eliminates need for external ISPs, resulting in reduced costs
- V4L2 API support helps shorten software development period
- CMOS sensor selectable
- Free BSP and sample application software enables immediate prototype development
- DRP flexibility enables future expansion of functionality

Related Information

- [AI Accelerator \(DRP-AI\)](#) — AI Accelerator (DRP-AI) White Paper
- [RZ/V2M](#) — Renesas' AI-only Accelerator (DRP-AI) and 4K-compatible Image Signal Processor (ISP), and Vision-AI ASSP for Real-time Human and Object Recognition using embedded devices
- [RZ/V2L](#) — General-Purpose Microprocessor Equipped With Renesas' Original AI-Dedicated Accelerator (DRP-AI), 1.2GH Arm® Cortex®-A55 CPU, 3D Graphics, and Video Code Engine
- [RZ/G2L](#) — General-purpose Microprocessors with Dual-core Arm® Cortex®-A55 (1.2 GHz) CPUs, with 3D Graphics and Video CODEC Engine

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
<https://www.renesas.com>

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
<https://www.renesas.com/contact-us>

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

