Custom Instrumentation Amplifier Design

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Abstract

This application note describes some of the fine points of designing an instrumentation amplifier with op-amps. We will cover how to maintain good common-mode rejection and output signal linearity. In addition, we will explain various filters that can be integrated in the design to provide additional performance improvements. For our example, we use Dialog's SLG88102V ultra-low power, quad op-amp integrated circuit.

Basic Theory

Difference amplifiers amplify the difference between two input voltage signals. A typical circuit topology, shown in Figure 1, takes the difference between V1 and V2, amplifies it by a factor of R2/R1, and outputs the amplified difference to VO. In addition to amplifying the difference between the input signals, this circuit rejects common-mode signals that are present on both input terminals. For single supply amplifiers, this common-mode rejection is especially important as the common-mode voltage of the input pins isn't amplified despite its input biasing centered off the well-behaved GND plane.

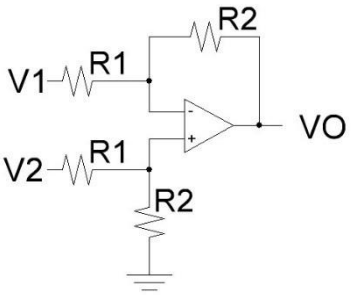

Figure 1. Difference Amplifier

This basic difference amplifier topology, however, is often inadequate by itself to interface sensors due to its low resistive input impedance: V1 and V2 have impedances of R1 and R1+R2 respectively. The loading on a high impedance sensor due to the amplifier input impedance can result in significant measurement error. To avoid this problem, engineers use the instrumentation amplifier.

The instrumentation amplifier typically uses the three op-amp circuit topology shown in Figure 2. By using the additional buffering op-amps, the designer can take advantage of the input terminal's high input impedance to avoid loading the circuit he or she is trying to amplify. This circuit also provides multistage gain that is easily adjustable with the use of the various resistors in accordance with Equation 1.

$$\frac{V_O}{V_1 - V_2} = \left(1 + \frac{2R_3}{R_G}\right)\frac{R_2}{R_1}$$

Equation 1. Instrumentation Amplifier Gain

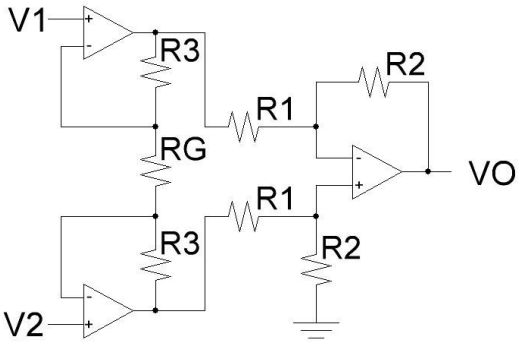

Figure 2. Instrumentation Amplifier

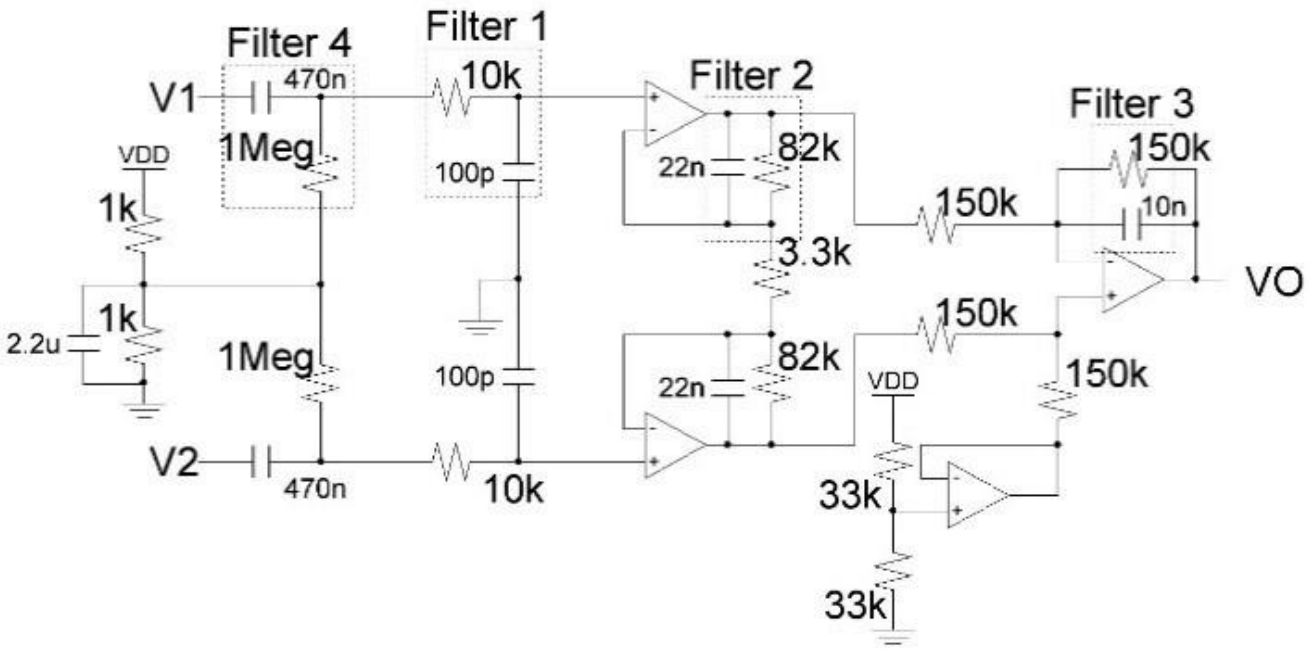

Figure 3. Instrumentation Amplifier Example Schematic

Numerous off-the-shelf instrumentation amplifier ICs are available with various open-loop gain values, noise performance characteristics, common-mode rejection ratios (CMRR), power supply rejection ratios (PSRR), and other amplifier specifications. These integrated chips typically allow for some limited adjustments such as basic gain programming using an external gain resistor (R_G). If more flexibility is desired, such as noise filtering and frequency response adjustment, a custom implementation can provide an effective solution.

Instrumentation Amplifier Example Design

Figure 3 shows an example instrumentation amplifier schematic with additional filtering and biasing circuitry from our previous schematic shown in Figure 2.

By using Equation 1, we can calculate a differential input voltage gain of approximately 50 for this circuit. The capacitors added to this circuit provide RC signal filtering at various points in the circuit. Although most of the filters are low-pass in nature, the 470nF capacitors and 1MegΩ resistors are used as high pass filters to AC couple the input signals into the instrumentation amplifier. The 1kΩ resistors DC bias this input voltage at mid-supply. Similarly, the 33 kΩ resistors and the voltage follower op-amp bias the output voltage at mid-supply. Other sections of this application note will discuss these topics in more detail.

Signal Filtering Techniques

In many circuits, filtering allows the designer to extract a desired signal frequency from unclean signals in a noisy environment.

In a similar way, it is often necessary to remove unwanted frequencies from the instrumentation amplifiers. By creating a custom instrumentation amplifier, the designer opens up many ways to filter an input signal.

	Type	Resistor (Ω)	Capacitor (F)	Cutoff Frequency (Hz)	Number of Poles
1	Low Pass	10k	100p	159.2k	2
2	Low Pass	82k	22n	88.22	2
3	Low Pass	150k	10n	106.1	1
4	High Pass	1Meg	470n	338.6m	2

Table 1. Filter Frequencies

$$f_{3dB} = \frac{1}{2 * pi * R * C}$$

Equation 2. RC Filter Equation

Table 1 lists the various filters that we have included in our design. Equation 2 shows the frequency calculation for a simple RC filter. By looking at the AC analysis of the instrumentation amplifier as shown in Figure 4, we can see that these filters cause low and high frequency roll off of the amplifier's gain. To receive the full differential gain of 50, the input signal needs to be between 1 Hz and 20 Hz. By changing the internal filtering, the AC characteristics can be altered to the desired frequency ranges.

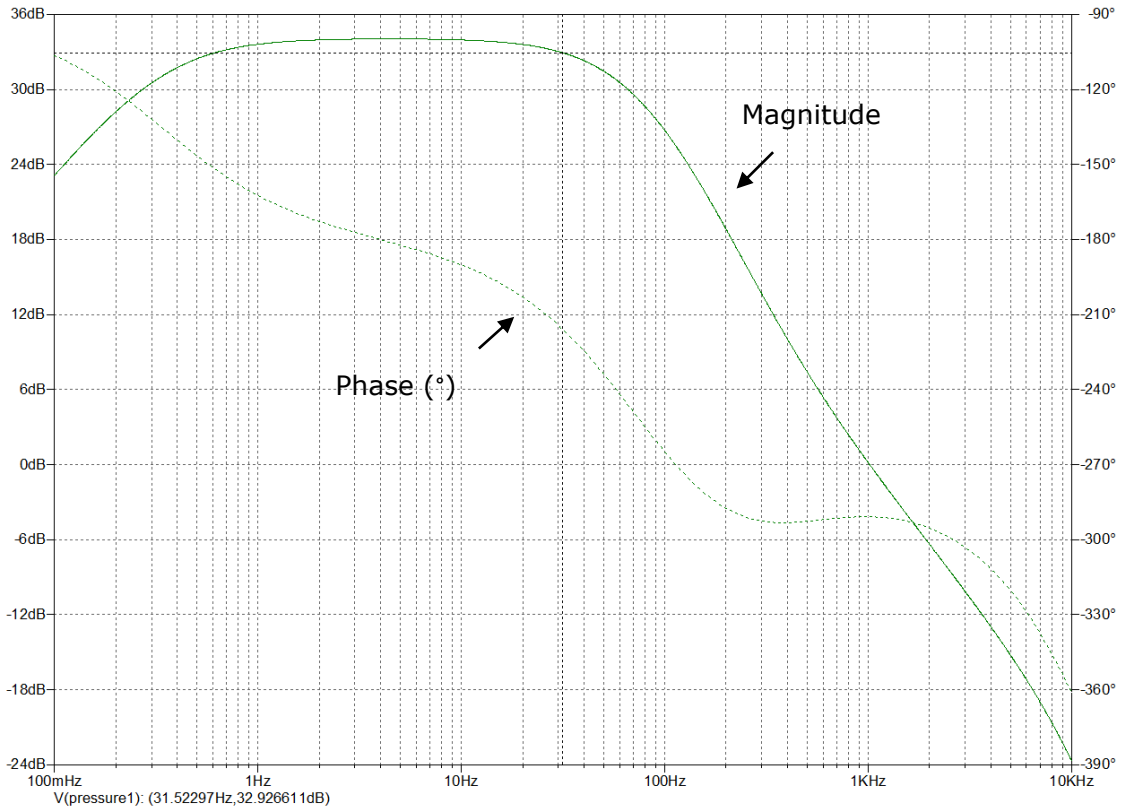

Figure 4. AC Analysis of Instrumentation Amplifier Output

For this instrumentation amplifier example, the filter poles were chosen to provide a gain-bandwidth (GBW) of approximately 1 kHz. The low-frequency attenuation exists because of filter 4 in Table 1. In order to DC bias the input signal at mid-supply, this filter needs to be included to block the DC signals from passing through the 470nF capacitors into the differential sources.

Achieving Common-Mode Rejection

As previously noted, ideal instrumentation amplifiers can reject all common-mode signals present on both input terminals. In reality though, the strength at which an instrumentation amplifier rejects these signals is finite and is characterized in terms of its common-mode rejection ratio (CMRR). CMRR is defined as the ratio of the differential-mode gain to the common-mode gain of a circuit. The CMRR of an instrumentation amplifier is frequency dependent and rolls off at high frequency. A non-ideal CMRR results from two different sources inside the instrumentation amplifier: 1) the individual op-amps themselves and 2) the mismatch in the gain resistor values.

Inside the op-amp, two different effects impact the CMRR of our instrumentation amplifier. The first effect comes from component mismatch in the op-amp fabrication process. For example, an op-amp might have an input stage similar to the differential pair shown in Figure 5. This input differential pair takes two signals and turns them into a single-ended signal that appears at VO.

Mismatched drain resistance, transistor areas, channel lengths, gate capacitances and many other aspects in just this differential pair can cause unwanted differential output voltages at VO even with the inputs V1 and V2 shorted together. The second effect that impacts CMRR can be seen when looking at frequency dependent common-mode signals. As the frequency of the common-mode signal increases, op-amp capacitive coupling also increases. As the frequency increases, the capacitances inside the circuit start to look like short circuits and common-mode signals can feed into sensitive nodes within the op-amp. The magnitude of these common-mode effects are generally documented in op-amp datasheets as CMRR specifications. SLG88102V, for example, features a CMRR of 82dB.

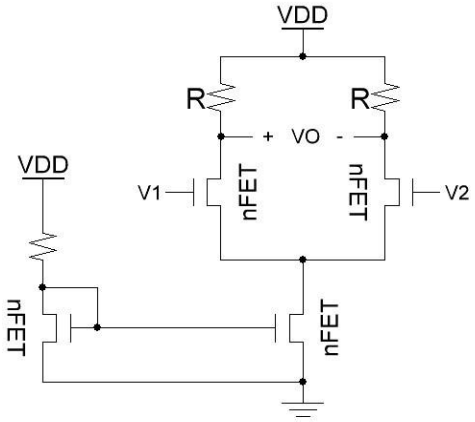

Figure 5. Differential Pair Schematic

The second source of CMRR degradation in an instrumentation amplifier comes from the circuit component mismatches.

With the instrumentation amplifier topology, systematic CMRR is a function of the gain ratio mismatch. This mismatch is determined by the difference stage's gain resistors (R1 and R2 of Figure 2) in the inverting and non-inverting paths. This CMRR effect is given by the expression shown in Equation 3. In this equation, ΔR represents the difference between the feedback resistor ratios on the positive and negative side of the differential op-amp. In the ideal case, ΔR goes to zero and CMRR approaches infinity. It is easy to see that any difference between the resistor ratios will reduce this value to a finite number.

$$CMRR = \frac{\left(\frac{1}{2}\right)(G+1)}{\left(\frac{1}{2}\right)\left(\frac{R_{2-}}{R_{1-}}\right)(\Delta R)} \quad where\ \Delta R = \left(\frac{R_{1-}}{R_{2-}} - \frac{R_{1+}}{R_{2+}}\right)$$

Equation 3. CMRR of a Difference Amplifier

With this information in mind, how can one design an instrumentation amplifier to maintain high CMRR? This can be achieved through careful attention to resistor matching. For starters, use high precision (<1%) resistors in your circuit. Similarly, one should reduce additional trace and wire resistance impacts by keeping connections short and symmetrical on both inputs of the difference amplifier stage.

Proper Signal Biasing

When following the differential signal path through the instrumentation amplifier, it is important to check that all of the internal and external signals are biased away from the power supply and ground rails.

The reason for this lies in the open loop gain characteristics of an op-amp.

In control theory, the closed loop gain of an op-amp is described by Equation 4, where A_{OL} is the open loop gain and B is the resistive feedback of the circuit.

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL} * B}$$

Equation 4. Closed Loop Gain Equation

In an ideal scenario, the open loop gain of an op-amp is infinite and the equation can be reduced to 1/B. In reality though, an op-amp has finite open loop gain which degrades when it operates close to the rails (GND and VDD for single supply op-amps). This begins to occur when the supply voltage headroom approaches 0. This behavior is illustrated in Figure 6. Since the open loop gain decreases around the rails of an op-amp, the closed loop gain of the system starts to change with the open loop gain. This introduces error into the system and causes a non-linear output. The graph in Figure 6 represents how the SLG88102V op-amp operates near the rail. The SLG88102V datasheet describes a linear output swing range 100mV inside the positive and negative rails.

Figure 7. AOL vs VOUT Characteristics for SLG88102V

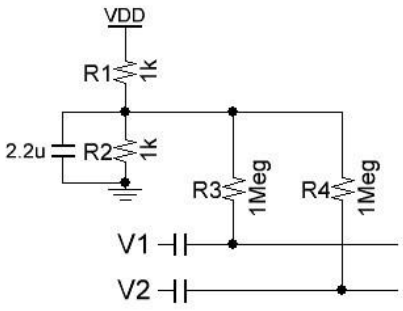

Figure 6. Input Mid-supply Biasing

In order to minimize the non-linearity of the output signal, the op-amp needs to be biased within this linear range. By biasing the input and output signals at mid-supply, the maximum open loop gain of the amplifier kicks in and helps reduce the closed loop gain error.

To DC bias the input signals, we can use a simple voltage divider with the input signals AC coupled onto the DC biased terminals. This idea is shown in Figure 7. By dividing the voltage in half and using a high impedance resistor to pass the voltage onto the input pins of the instrumentation amplifier, we can provide a mid-supply, DC offset to the AC differential input present across V1 and V2. In addition, this topology reduces the need for two resistive dividers and close resistor matching on each divider. By using one resistive divider and equally matched 1MegΩ resistors, this topology allows for common-mode voltage matching on both of the input terminals.

Similarly, the output of the instrumentation amplifier needs to be biased at mid-supply. By biasing the difference amplifier as shown in Figure 8, the output of the instrumentation amplifier will be centered on a mid-supply voltage. The voltage divider buffer is required to minimize the loading on the difference amplifier. Without this buffer, resistive loading would introduce common-mode amplification to the circuit.

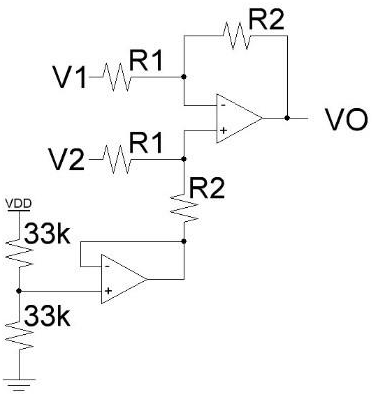

Figure 8. Output Mid-supply Biasing

These design techniques will properly bias an instrumentation amplifier to operate in regions with maximum open loop gain. This maximized open loop gain reduces the non-linearity of the circuit.

PCB Layout Recommendations

When testing a designed amplifier circuit, custom PCBs are often required to minimize the negative effects of a breadboard on the circuit's overall performance. These effects come from the breadboard's passive (resistive, capacitive, and inductive) element additions to the circuit. There are a few proper PCB design techniques that will help minimize the resistive and capacitive effects on the circuit.

First, it is important to place a few decoupling capacitors on the PCB. These capacitors serve two primary purposes: they filter out unwanted high frequency signals from the power supply, and they act as a local power supply for individual ICs in the circuit. These capacitors are generally placed close to the power supply connection of the PCB and the power supply pins for sensitive ICs like the SLG88102V. By placing these capacitors spatially close to an IC, the capacitor can generate a charge and promptly respond to rapid changes in current consumption. Without these capacitors, it would take time for the power supply to react to these changes in current consumption. In addition, high frequency components of the power supply will cause voltage fluctuations on the power rail. By placing these capacitors close to the supply and the IC, these frequencies are shunted to ground.

Another important design technique requires keeping the input and output signals spatially separated on the PCB. Separating these traces helps prevent crosstalk between the input and output traces through AC coupling.

Keeping the input traces close together and symmetric on the PCB is another way to improve performance. When the input traces are close together, both traces pick up common noise from external sources. In the "Achieving Common-Mode Rejection" section of this application note, we discussed the importance of resistive matching in the circuit. Since traces introduce resistance to the circuit, it is important to pay attention to how one lays out the traces in the PCB designer. By keeping the input trace lengths close to each other and symmetric, the residual voltage changes from these traces are able to be rejected by the filter's CMRR. In a similar way, minimizing the trace lengths of an op-amp's feedback loops will help maintain the instrumentation amplifier's CMRR.

Finally, creating a ground plane of copper pour on a PCB layer is useful in reducing ground voltage potential differences across a circuit's various ground nodes. By creating a low resistance square of copper on one layer of the PCB, the effective resistance of the individual ground routing is decreased. As a result, the current through these individual ground routes creates less voltage potential differences between ground nodes.

In Figure 9, the PCB schematic is shown for this instrumentation amplifier design. This schematic was used with the layout in Figure 10 to create our custom instrumentation amplifier PCB.

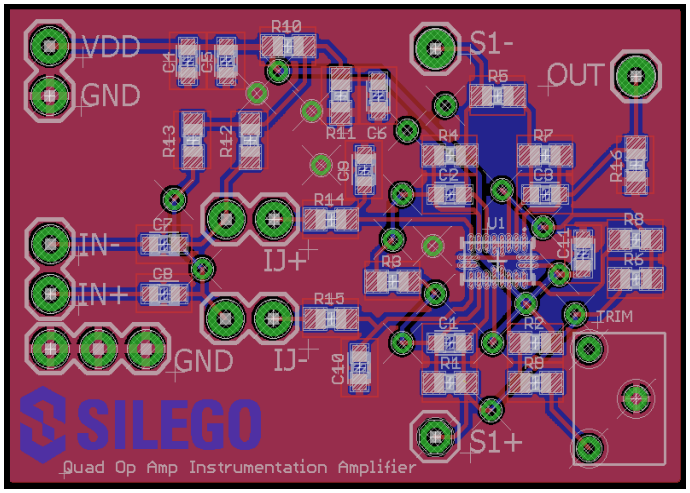

Figure 9. SLG88102V Instrumentation Amplifier Layout

Component	Value	Component	Value
R1	82kΩ	C1	22nF
R2	33kΩ	C2	22nF
R3	3.3kΩ	C3	10nF
R4	82kΩ	C4	100nF
R5	150kΩ	C5	1uF
R6	150kΩ	C6	2.2uF
R7	150kΩ	C7	470nf
R8	150kΩ	C8	470 nF
R9	33kΩ	C9	100pF
R10	1kΩ	C10	100pF
R11	1kΩ	C11	100nF
R12	1MegΩ	U1	SLG88102V
R13	1MegΩ	Trim	5k Trim Resistor
R14	10kΩ		
R15	10kΩ		
R16	10kΩ		

Table 2. SLG88102V Instrumentation Amplifier Components

The specific values used in the design are shown in the schematic view and in Table 2.

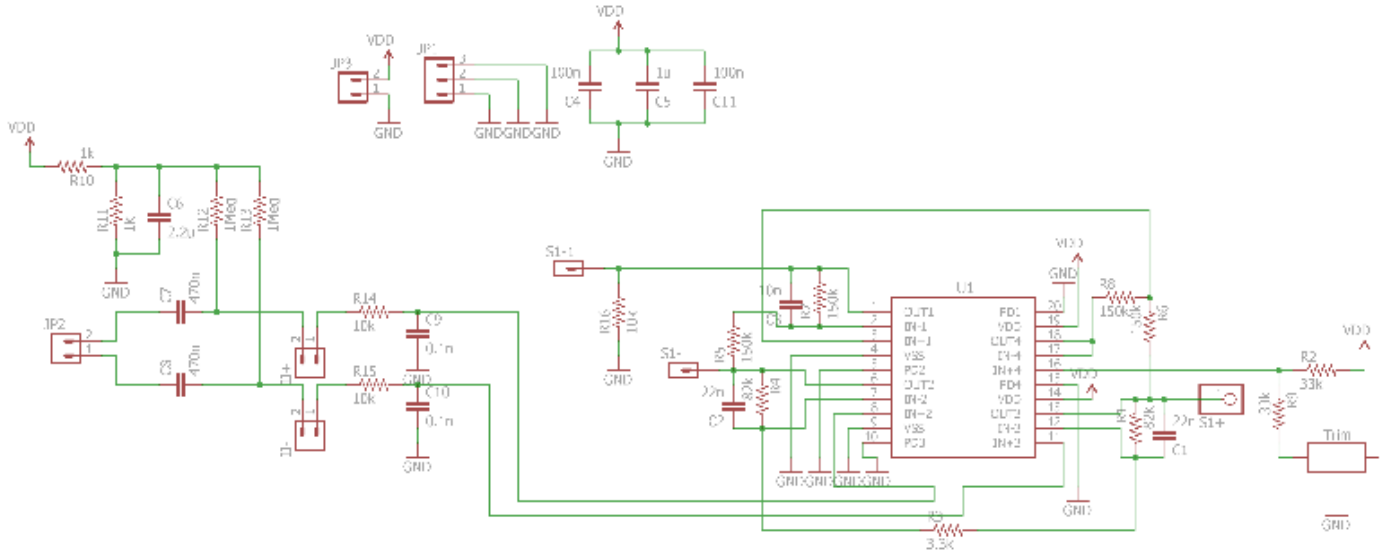

Figure 10. SLG88102V Instrumentation Amplifier Schematic

Measured Results

The fully constructed instrumentation amplifier PCB is shown in Figure 11. In order to test this final design, we are going to compare the experimental and simulated output amplitudes, the closed-loop gains, the GBWs, and the common-mode ranges of the input signal. The measured and simulated values are included in Table 3. For simulation, we used the SLG88101V op-amp model. To test this design, we set VDD to 5 V and grounded IN+. We also placed two jumpers onto the PCB: one across IJ+ and the other across IJ-.

Figure 11. Instrumentation Amplifier PCB

	Simulation	Experimental
A_{CL} (dB)	34.03	33.87
GBW (kHz)	1.014	0.921
Amplitude (V_{PP})	1.00	1.0149
V_{CM-H} (V)	4.74	4.76
V_{CM-L} (V)	0.28	0.25

Table 3. Experimental and Simulated Results

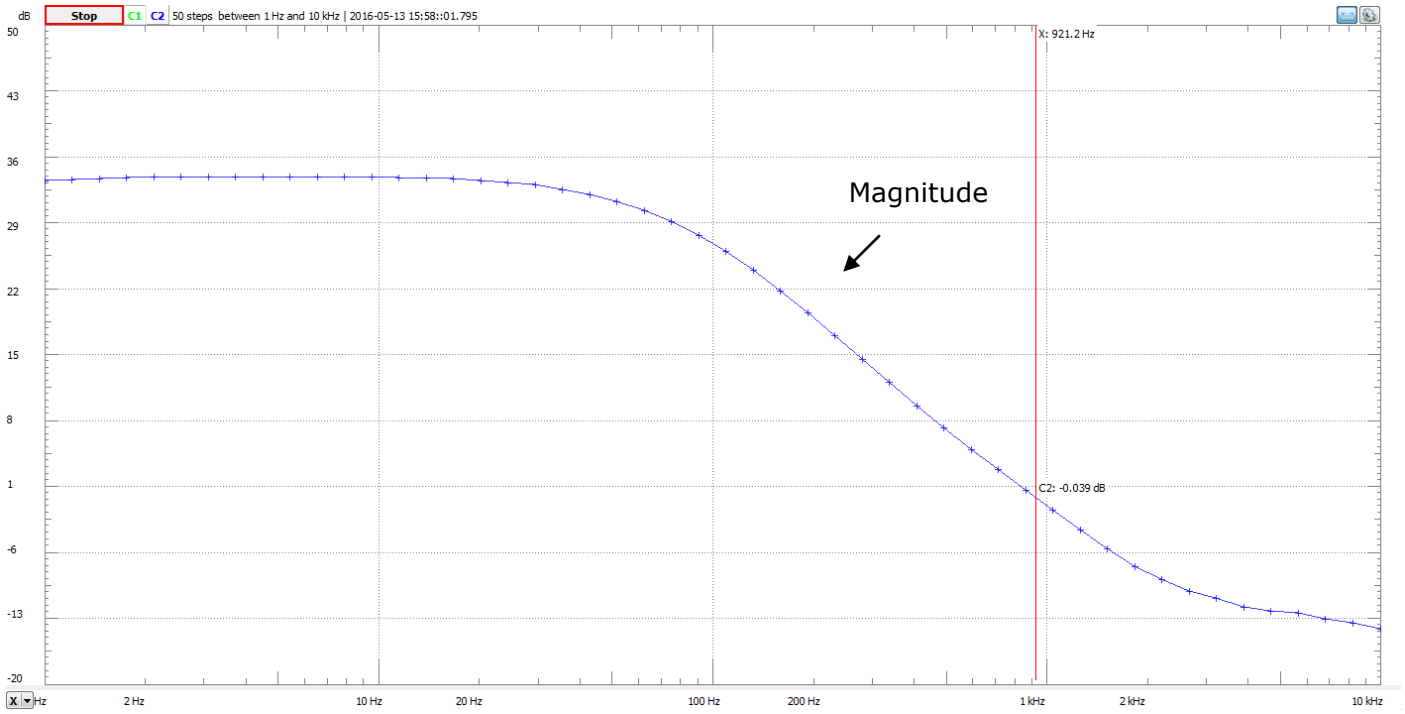

Figure 12. Magnitude plot of the Instrumentation Amplifier

The AC response of this instrumentation amplifier was generated by looking at OUT with respect to IN- with IN+ set to ground. Figure 12 shows the magnitude plot of this circuit. The measured closed loop gain of this circuit is approximately 33.87dB. In simulation, this value was 34.03dB. The experimental gain-bandwidth was 921Hz while the simulated gain-bandwidth was 1.014 kHz.

Figure 13 shows the transient response of this instrumentation amplifier with a 20 mV_{PP}, 0V DC offset on IN-. The magnitude of this signal is 1.0149V_{PP}. In simulation, the magnitude of this signal was approximately 1.00V_{PP}.

The common-mode range of the input signal can be swept by manually pulling the node between R10 and R11 from 0 to VDD.

When the common-mode voltage draws close to the rails, the output signal should clip. Figure 14 and Figure 15 show the experimental voltages at which the output starts to clip. Since this is an inverting amplifier, the lower end of the graph starts to clip as the voltage reaches and exceeds 4.76V. Similarly, as the voltage drops to approximately 0.25V, the top of the transient waveform starts to clip. These values are closer to the rail than the simulated values which are 4.74V and 0.28V respectively.

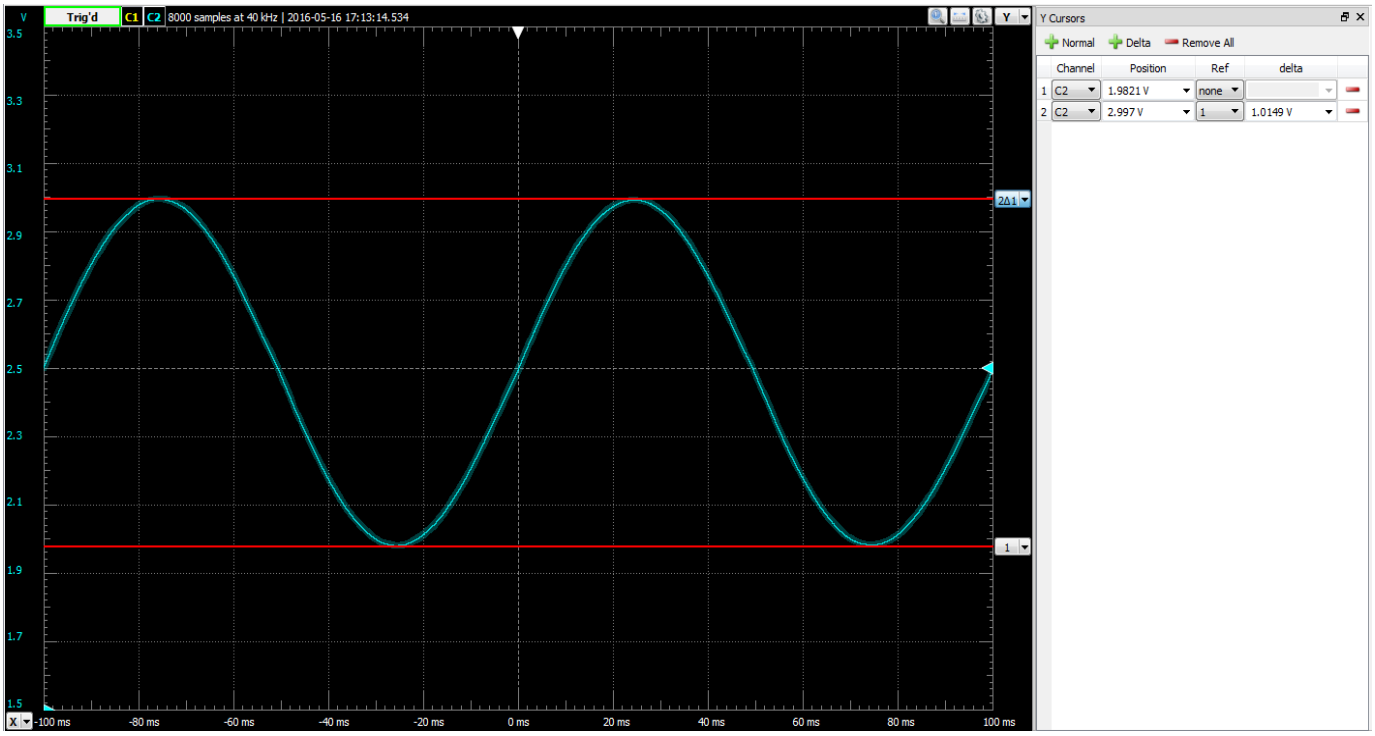

Figure 13. Transient Response with 20mV_{PP} IN- Input

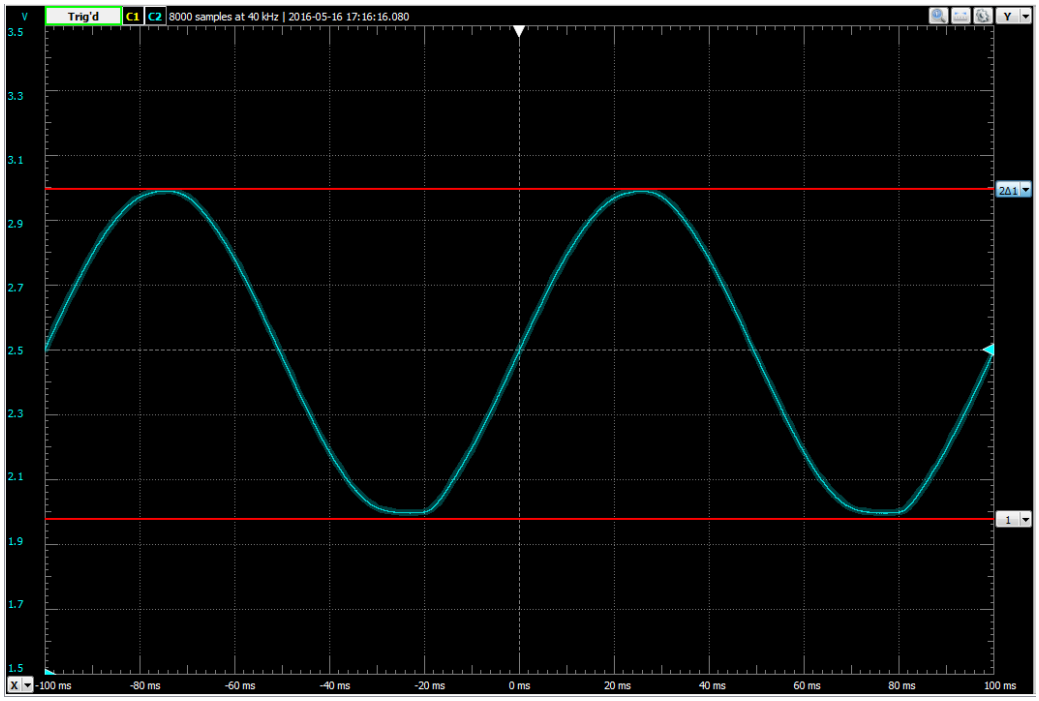

Figure 14. OUT with Common-mode Voltage of 4.76V

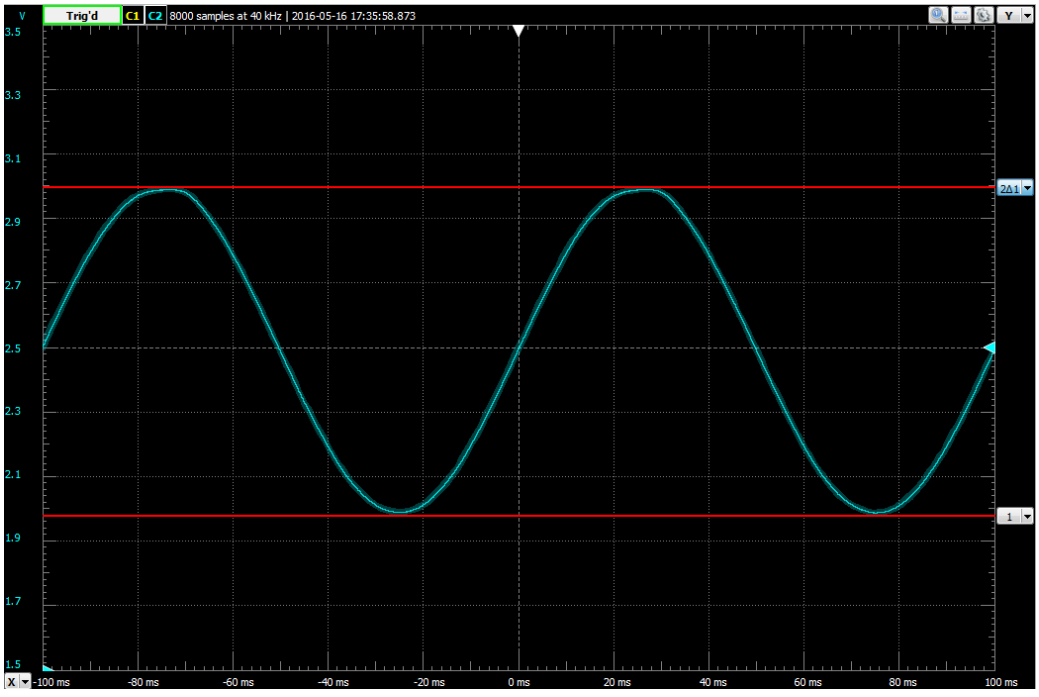

Figure 15. OUT with Common-mode voltage of 0.25V

Conclusion

By using the standard three op-amp instrumentation amplifier topology with some of these described design techniques, a designer can create a linear instrumentation amplifier with high CMRR. By creating the instrumentation amplifier from scratch, the designer opens up the ability to incorporate custom signal filtering into their instrumentation amplifier. All of the op-amps required for this design are available on one SLG88102V quad op-amp package. These op-amps feature rail-to-rail input and output operation with only 400nA of current consumption with each op-amp. The PCB design techniques explained in this application note help guide the designer in creating a high performance, nicely packaged instrumentation amplifier.

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