Operation of the UniSLIC14 & IDT821054 Evaluation Module

Application Note | May 2002 | AN1004.1

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Functional Description

This application note is intended to supplement IDT's Evaluation Board User's Guide. The Users guide describes the Evaluation Board System and use of its software. The system includes one IDT821054 evaluation board, one UniSLIC14 evaluation board and control software IDT821054.exe. For discussion purposes, the IDT821054 evaluation board will be referred to as the Mother Board and the UniSLIC14 evaluation board will be referred to as the Daughter Board.

A good understanding of the material in the Users Guide is a prerequisite to this application note. For a detailed engineering analysis of the reference design using the UniSLIC14 and IDT821054, see application note AN9999.

With this system, the user can configure a channel to channel conversation and perform various tests on the system using a Wandel and Golterman (W&G) PCM4.

The IDT821054 Evaluation Board System can be configured in two modes of operation via JP1, JP2 & JP3 on the mother board.

- **Emulation Mode,** Emulation Mode gets its name from the evaluation board's ability to emulate a far end callee (or caller) telephone conversation as a stand alone unit. In this mode the DC performance of the SLIC (logic state, Tip & Ring voltage levels, on hook & off hook detection) and channel to channel conversation is easily evaluated using the on-board clock circuit of the Mother Board.
  Jumper Configuration:
  JP1 jumper IN (shorting DX/DR)
  JP2 jumper IN (providing power to the on board oscillator)
  JP3 IN (connecting INTERNAL clock to board)
- **Test Mode,** Test Mode gets its name from the evaluation board's ability to test the performance of the system using a PCM4. In this mode the AC performance of the half channel (D/A, A/D, D/D) can be evaluated
  Jumper Configuration:
  JP1 jumper OUT
  JP2 jumper OUT
  JP3 IN (connecting EXTERNAL clock to board)

This application note will first evaluate the DC performance of the system by configuring the Jumpers in the Emulation Mode. Figure 2 shows the required connection between the Evaluation Board, PC, PCM4 tester and Power Supplies. Proper connection should be established before running the software.

If the user prefers to evaluate the AC performance first, then along with the proper connections (Figure 2) and jumpers positioned for the test mode, the user needs to insure the clock of the PCM4 is connected before running the software.

Verifying Basic Operation

The operation of the Mother & Daughter Boards can be verified by performing the following tests:

1. Normal Loop Feed Verification
   Tip & Ring Voltage Forward Active State, On Hook
   Tip & Ring Voltage Forward Active State, Off Hook
   Tip & Ring Voltage Reverse Active State, On Hook
   Tip & Ring Voltage Reverse Active State, Off Hook
2. Loop Supervisory Detection
   On Hook & Off Hook
   Tip Open State, Ground Key Test
   2-wire Loopback
   Operation of the ISL5571A Latch
3. Ringing Verification and operation of the ISL5571A Access Switch.
4. Programming of Coefficients
5. Emulation of Far End Telephone Conversation
6. Gain Verification
   Total System Gain (Digital to Digital)
7. Variable Gain/Frequency
   Receive Gain (Digital to Analog)
   Transmit Gain (Analog to Digital)
8. Total Distortion
   Receive Gain (Digital to Analog)
   Transmit Gain (Analog to Digital)

UniSLIC14 Daughter Board

The HC5514XEVAL2 evaluation board, due to the common pinout of the UniSLIC14 family, is capable of evaluating the performance of the following parts in the UniSLIC14 family (HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150).

The sample provided with this board (HC55142) will meet or exceed the electrical performance for all members of the family listed above.The evaluation board is optimized to match either a 600Ω or a 200Ω + 680Ω||0.1µF line impedances, have a minimum loop current of 20mA, a maximum loop current of 30mA, onhook transmission of $0.775V_{RMS}$, offhook voice transmission of $3.2V_{PEAK}$, and a maximum loop resistance of 1777Ω.

For evaluation of the programmability of the HC5514 family, reference the data sheet for calculation of external components. An Excel spread sheet can be downloaded from the web for easy calculation of external components (www.intersil.com/telecom/unislic14.xls).

The daughter board is a dual channel board that enables testing between adjacent channels (CH1 to CH2, CH3 to CH4, CH5 to CH6, and CH7 to CH8). An additional daughter board can be obtained to enable testing between all channels.

Reference the application note AN9999 for calculation of external components and programming coefficients.

Programming of the logic state of the SLIC, loop supervisory detection, time slot allocation, coefficients, tone/ teletax signals are all controlled via software using the MPI screen (Figure 3).

IDT821054 Mother Board

The IDT821054 Mother Board provides a way to evaluate the operation of IDT's IDT821054 and Intersil's UniSLIC14 family of SLICs. The programming interface illustrated in this application note is the Microprocessor Interface (MPI). Figure 1 shows the IDT821054 mother board component locations. The location of jumpers JP1, JP2, and JP3 are highlighted with arrows. JP1 is used to short the DX and DR signals from the PCM4 to prevent interference when Emulation Mode testing is performed. JP2 connects power to the on-board clock. This enables setup of the software without having to use the clock from the PCM4. JP3 connects either the on-board clock or the clock from the PCM4. Proper operation of the software requires this clock signal.

Getting Started

The following steps will configure the Mother Board for testing in either the Emulation Mode or the Test Mode.

1. Connect IDT821054, UniSLIC14 and PCM4 as shown in Figure 2. Note: The Daughter Board gets its power from the Mother Board.
2. Set the General Parameters of the PCM4 as shown in Table 3 (see Test #6).
3. Once power is applied and the appropriate clock is supplied to the Mother Board (i.e internal clock for Emulation Mode, or PCM4 clock for Test Mode), PRESS the reset button. The LED will flash and then remain on. This will synchronize the clock and enable software control from the PC.
4. Initialize the software by clicking on IDT821054.exe and select the desired Operating Mode (MPI), COM Port and SLIC from the Mode and Port selection screen then click OK.
5. The MPI Mode screen will then appear (Figure 3). All programming of the channels and monitoring of SLIC status are performed using this screen.
6. From MPI Software screen, select Channel 1 in the left shaded area.
7. From MPI Software screen, select Global operation in the left shaded area. Accept defaults or set to your preferences and click the Write button.
8. From MPI Software screen, click on the Auto Detect Enable box. This will enable the CODEC to detect the status of the SLIC. Detection will be in the form of the receiver next to the channel indicator, left shaded area, being one of the 4 indicators located at the bottom of the shaded area in the Legend (Active, Ring, In Use, Power Off). The Auto Detect Enable box will also activate the I/O Pin Status of the SLICs $\overline{SHD}$ pin via SI1 and $\overline{GKD}$ pin via SI2. A red color signifies a logic one and green color a logic zero.
9. From MPI Software screen, clicking on the Broadcast Mode will enable the user to configure multi-channels at the same time.
10. From MPI Software screen, Select: Active F, Power On and click the Write button. **The SLIC is now ready to be tested.**

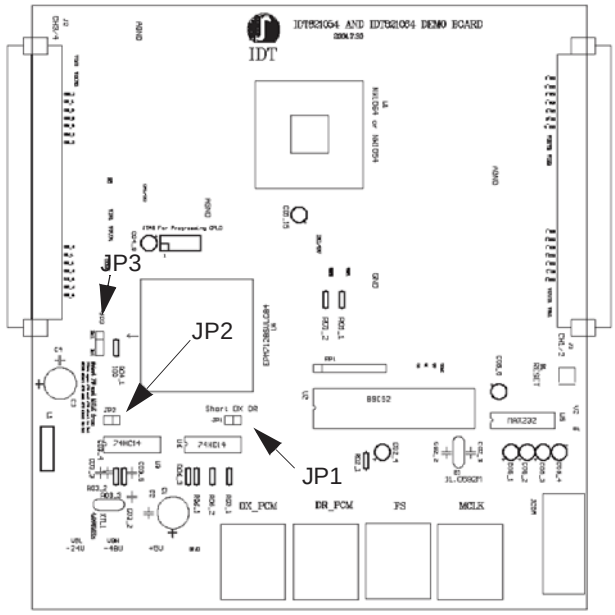


FIGURE 1. IDT821054 MOTHER BOARD COMPONENT LOCATION

Test # 1 Normal Loop Feed Verification

This test verifies the correct tip and ring voltages in both onhook and offhook forward active and reverse active states. Loop current and ground key detect are also verified via the software MPI screen.

Discussion

The HC55142 is designed to have its most positive 2-wire terminal (tip in the forward active state and ring in the reverse active state) fixed at a set voltage. This set voltage depends upon the required overheads for the application. The most negative 2-wire terminals voltage is dependent upon the load across tip and ring and the programmable current limit.

The tip and ring voltages for various loop resistances are shown in Figure 4. The tip voltage remains relatively constant as the ring voltage moves to limit the loop current for short loops.

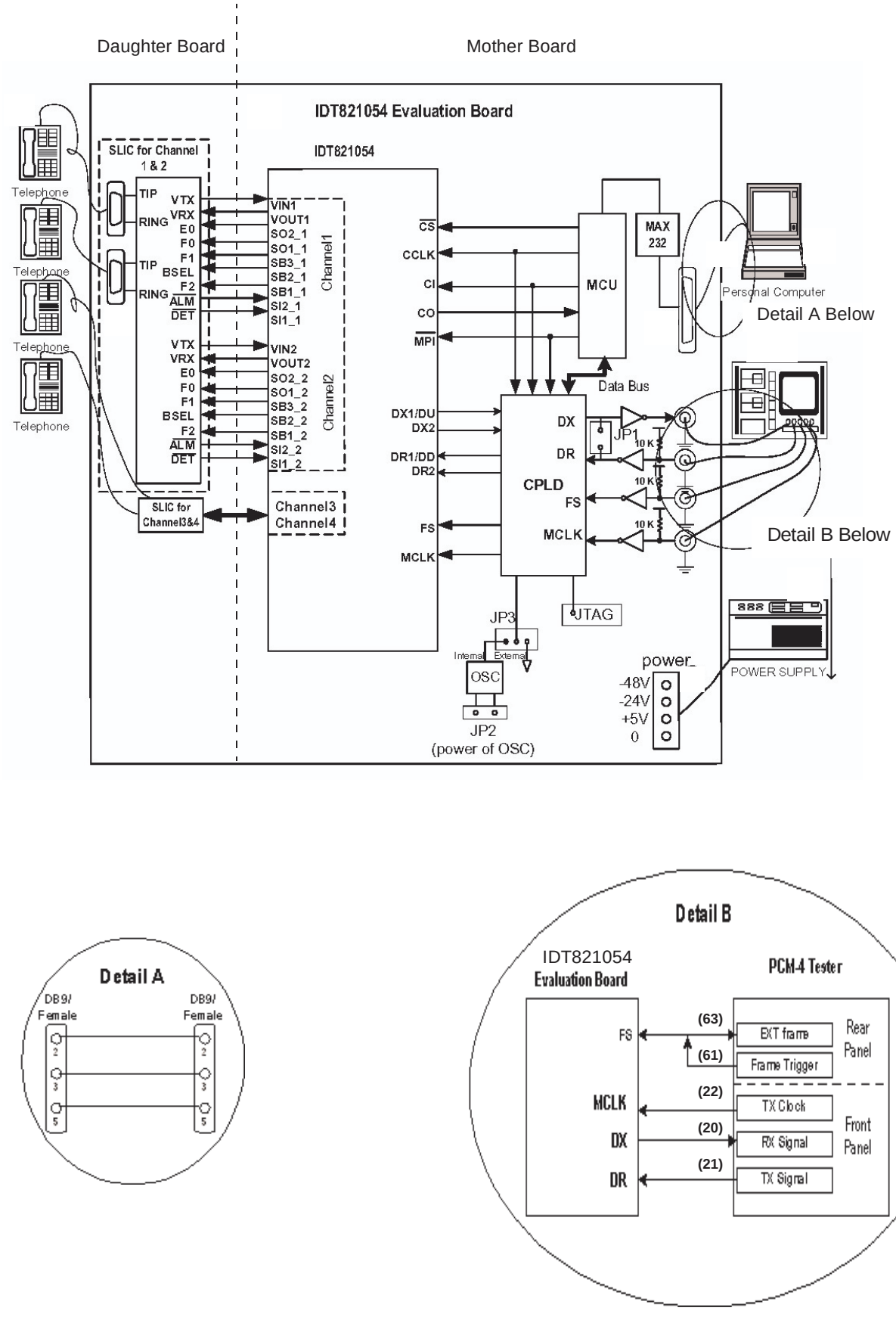


FIGURE 2. IDT821054 MOTHER BOARD CONNECTIONS

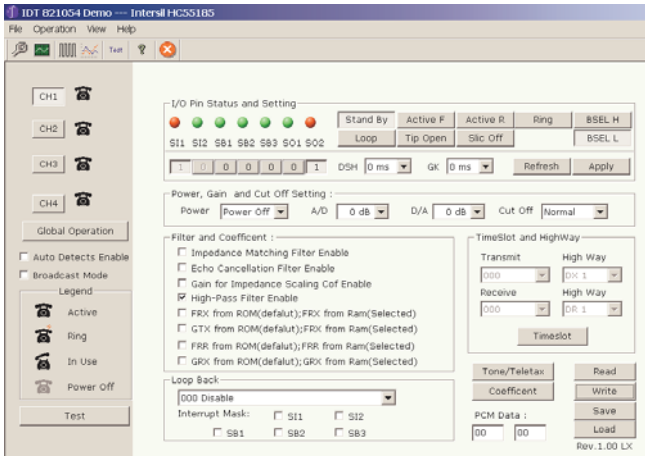


FIGURE 3. MPI OPERATION GENERAL INTERFACE

When power is applied to the SLIC, a loop current will flow from tip to ring through a load placed across tip and ring. Loop current detection occurs when this loop current triggers an internal detector that pulls the output of $\overline{SHD}$ low. This is detected by the software and the I/O Pin SI1 turns Green.

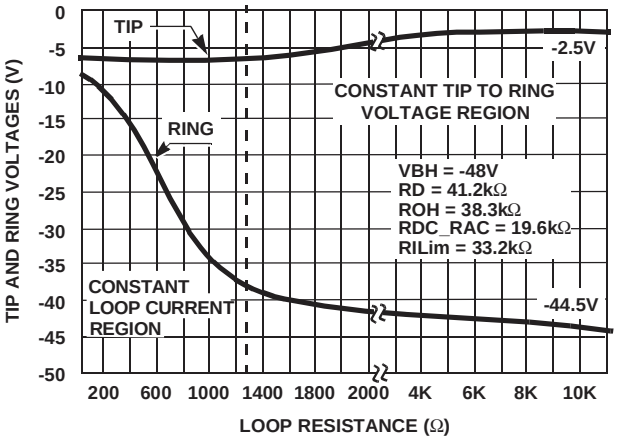


FIGURE 4. TIP AND RING VOLTAGES vs LOOP RESISTANCE

The Ground Key detector ($\overline{GKD}$) operation is verified by configuring the HC55142 in the tip open state and grounding the ring pin. Grounding the ring pin results in a current that triggers an internal detector that pulls the output of $\overline{GKD}\_\overline{LVM}$ pin low. This is detected by the software and the I/O Pin SI2 and SI1 turn Green.

Most of the SLICs in the UniSLIC14 family feature 2-Wire loopback testing. This loopback function is only activated when the subscriber is **on hook** and the logic command to the SLIC is in the Test Active State. (Note: if the subscriber is **off hook** and in the Test Active State, the function performed is the Line Voltage Measurement. Reference data sheet for information on Line Voltage Measurement. This test platform is not setup to enable testing of the line voltage measurement function). During the 2-wire loopback test, a 2kΩ internal resistor (Figure 5) is switched across the tip and ring terminals of the SLIC.

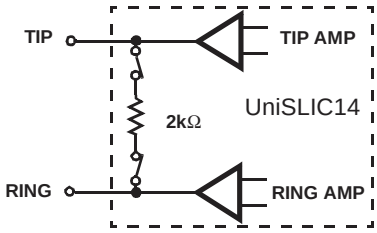


FIGURE 5. 2-WIRE LOOP BACK INTERNAL TERMINATION

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{SHD}$ low. This is detected by the software and the I/O Pin SI1 turns Green.

Measuring Tip and Ring Voltages

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:

- Jumper JP1 is IN,
- JP2 is IN,
- JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select: Active F, TSD, Power On.
4. Measure the tip and ring voltages (reference Figure 6) and compare to those in Table 1 (onhook).
5. Terminate TIP and RING with a 600Ω load via the RJ11 jack.
6. Measure tip and ring voltages with respect to ground and compare to those in Table 1 (offhook 600Ω).
7. From MPI Software screen, Select: Active R,TSD, Power On.
8. Disconnect the 600Ω load from across tip and ring.
9. Repeat steps 4, 5, 6 and 8.

TABLE 1. TIP AND RING VOLTAGES

LOGIC STATE	R_L (Ω)	TIP VOLTAGE REFERENCEDTO GND	RING VOLTAGE REFERENCED TO GND
Forward Active V_{BH} = -48V V_{BL} = NA V_{CC} = +5V	Onhook	≅-2.5	≅-44.0
	Offhook 600Ω	≅-6.0	≅-24.0
Reverse Active V_{BH} = -48V V_{BL} = NA V_{CC} = +5V	Onhook	≅-44.0	≅-2.5
	Offhook 600Ω	≅-24.0	≅-6.0

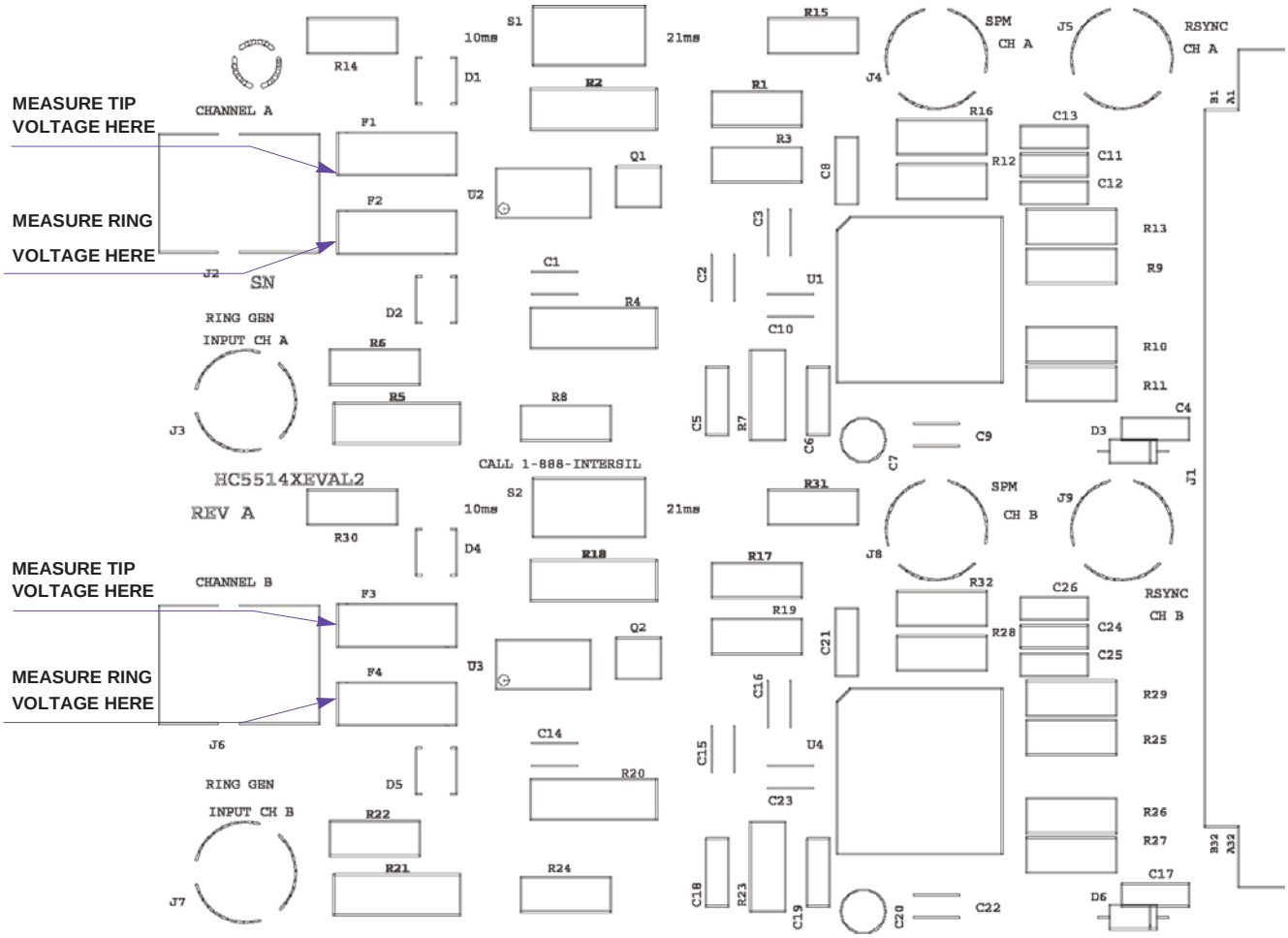


FIGURE 6. DAUGHTER BOARD LAYOUT

Test # 2 Loop Supervisory Detection

Verification of Switch Hook Detect

If previous test was Test #1, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:

- Jumper JP1 is IN,
- JP2 is IN,
- JP3 is set to Internal BCLK.
  NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select: Active F, TSD, Power On.
4. With the SLIC in either the forward active state (Active F) or reverse active state (Active R), the phone icon (left shaded area of the MPI screen) indicates In Use and the I/O Pin SI1 turns Green when tip and ring are terminated with 600Ω load and Red when tip and ring are an open circuit.
   NOTE: The I/O pin SI1 gives the status of the UniSLIC14 $\overline{SHD}$ output. Red is logic level high and Green is logic level low.
5. Disconnect the 600Ω load from across tip and ring.

Verification of Ground Key Detect

1. From MPI Software screen, Select: Tip Open, TSD, Power On.
2. The phone icon (left shaded area of the MPI screen) indicates Active and the I/O Pin SI2 is Red.
3. Momentarily Grounding the ring terminal will verify Ground Key Detect when the phone icon (left shaded area of the MPI screen) indicates In Use and the I/O Pin SI2 and SI1 turn Green.
   NOTE: The I/O pin SI2 gives the status of the UniSLIC14 $\overline{GKD\_LVM}$ output. Red is logic level high and Green is logic level low.

Verification of 2-wire Loopback

1. From MPI Software screen, Select: Active F and then Test A F, TSD, Power On.
   NOTE: The Test Active State requires previous state to be in the Forward Active state to determine the On hook or Off hook status of the line. To activate the 2-wire loop back function from the Test Active state, the line must be in a On hook condition when in the Active F state.

2. Verification of 2-wire Loopback operation is when the phone icon (left shaded area of the MPI screen) indicates In Use and the I/O Pin SI1 is Green.

Operation of the ISL5571A Latch

This test verifies the operation of the ISL5571A Latch.

Discussion

With the LATCH pin of the ISL5571A enabled, the logic state of the ISL5571A will remain in the last state programmed. The logic state of the UniSLIC14 will continue to follow the logic command of the IDT821054. Verification of the operation of the ISL5571A latch is accomplished by latching the ISL5571A in the idle/talk state. Now if we change the logic state of the UniSLIC14 to the ringing state, the tip voltage (which under normal conditions would measure about 0 volts for this state) continues to measure about -2.5V. This is because the ISL5571A was latched in the idle/talk state and the UniSLIC14's tip voltage in the ringing state will measure about -2.5V. Further verification of the operation of the ISL5571A's latch state is verified by unlatching the ISL5571A and noticing that the tip voltage now reads about 0 volts. This occurs because the relay has disconnected tip of the UniSLIC14 and connected it to ground through the ring return switch (SW3) Figure 9.

Verification of the ISL5571A Latch

1. From MPI Software screen, Select: Active F, TSD, Power On.
2. Verify tip voltage (no load, reference Figure 6) is around -2.5 volts.
3. From MPI Software screen, Select: Active F, TSD, LATCH,
   Power On.
4. Verify tip voltage measures about -2.5 volts.
5. From MPI Software screen, Select: Ring, TSD, LATCH, Power On. Tip voltage continues to measure around -2.5V.
6. From MPI Software screen, Select: Ring, TSD, Power On. Deselecting LATCH will configure the ISL5571A into the ringing state and tip will measure about 0 volts.

Test # 3 Ringing Verification and Operation of the ISL5571A

This test will demonstrate the ability of the IDT821054 to control the logic state of the UniSLIC14 and the onboard Line Card Access Switch (ISL5571A) when ringing a phone. A telephone and a battery backed ring generator are required to complete this test.

Discussion

The UniSLIC14 family handles all the popular ringing formats with high or low side ring trip detection. The daughter card is configured for battery backed ring injected ringing.

When the subscriber goes off hook during ringing, the UniSLIC14 family automatically controls the ISL5571A to open the ringing path and reconnect the tip and ring to the phone. Ring trip detection will occur when the DR pin goes more positive than DT by approximately 4V. The UniSLIC14 family has the capability to reduce impulse noise by synchronizing the ISL5571A to apply the ringing signal at zero ringing voltage and opening the ringing signal at zero ringing current.

APPLYING THE RING SIGNAL AT ZERO VOLTAGE

Applying the ring signal at zero voltage is accomplished by providing a ring sync pulse to the RSYNC CH A/B BNC on the daughter board (Figure 6). The ring sync pulse is synchronized to go low at the zero voltage crossing of the ring signal.

The RSYNC input is designed to allow the ring sync pulse to be present at all times. There is no need to gate the ring sync pulse on and off. When the RSYNC CH A/B is high the ISL5571A connects the SLIC to the phone. When the RSYNC CH A/B is low the ISL5571A is activated the instant the logic code for ringing is applied.

Operation of the ISL5571A does not require a RSYNC pulse be present. The daughter board is configured so the RSYNC pin is grounded through one of two resistors via SI or S2, channel A and B respectively (Figure 6).

The RSYNC pin performs two functions. The first is synchronization for zero voltage of the ring signal and the second function is polarity reversal time. The board is configured to provide 10msec or 21msec reversal times via S1 or S2. Reference UniSLIC14 data sheet for more information concerning this topic.

REMOVING THE RING SIGNAL AT ZERO CURRENT

The ISL5571A is automatically opened at zero current by the SLIC. The SLIC logic requires zero ringing current in the loop and either a valid switch hook detect ($\overline{SHD}$) or a change in the operating mode (cadence of the ringing signal) to control the ISL5571A to open at zero current. If the subscriber goes off hook during ringing, the $\overline{SHD}$ output will go low. An internal latch will sense $\overline{SHD}$ is low and instruct the ISL5571A to stop ringing. This prevents the ring signal from being reapplied to the line. To ring the line again, the SLIC must toggle between logic states. (Note: The previous state can not be the Reverse Active State. In the reverse state, the voltage on the CRT_REV_$\overline{LVM}$ capacitor will activate an internal latch prohibiting the ringing of the line.)

Figure 7 shows the sequence of events from ringing the phone to ring trip. The ISL5571A rings the phone when both the ringing code and ring sync pulse are present (A). $\overline{SHD}$ is high at this point. When the subscriber goes off hook the $\overline{SHD}$ pin goes low and stays low until the ringing control code is removed (B). This prevents the $\overline{SHD}$ output from pulsing after ring trip occurs. At the next zero current

crossing of the ring signal, ring trip occurs and the ring relay releases the line to allow loop current to flow in the loop (C).

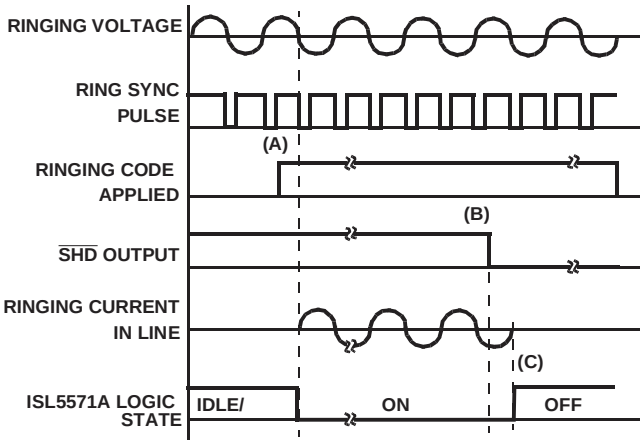


FIGURE 7. COEFFICIENT RAM OPERATION SCREEN

If the RSYNC_REV pin is low (by either a ring sync pulse or through a polarity reversal resistor), the ring relay driver pin (RRLY) pin goes low after the SLIC is placed in the ringing state. This will automatically configure the ISL5571A in the ringing state as shown in Figure 9. The ISL5571A disconnects tip and ring from the phone and connects the path for the ringing signal. The D_T and D_R comparator inputs will sense the flow of DC loop current, enabling the ring trip comparator to sense when the phone is either onhook or offhook. When an offhook condition is detected, the HC55142 will automatically disconnect the ringing signal to the phone reducing impulse noise to the system at the zero current crossing of the ring signal.

Ringing the Phone

If previous test was either Test #1 or #2, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:

- Jumper JP1 is IN,
- JP2 is IN,
- JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select: CH 1, Active F, TSD, Power On.
4. Connect a 20 Hz 90Vrms Battery backed (-48V) ringing signal to the Ring GEN BNC CH A on the daughter board.
5. Connect a phone to Channel 1 using the RJ11 jack on the Daughter Board
6. From MPI Software screen, Select Ring and the phone will start to ring. Cadencing of the ring signal is accomplished by switching between Ring and Active F (or Active R). Note: the command to the SLIC is immediate, you don't have to press Write for the command to be invoked.

Test # 4 Programming of Coefficients

Using the DSP coefficients provided by IDT, the overall performance of the system will pass ITU-T requirements.

When the COF RAM button is selected from the MPI Operation General Interface screen, the COF RAM Operation screen will appear (Figure 8). From this screen, the user can load the coefficients for the current channel.

For IDT to calculate IDT821054 DSP coefficient, customers should provide the following information about their subscriber line card:

- Accurate SLIC PSPICE model. It can be provided in.lib file or PSPICE schematic file.
- System Impedance
- Gain (Transmit path and Receive path)

IDT will then provide the user with 4 files, one for each channel. An example of a file name is: HC55142_600_1. The first portion of the file name is the SLIC being used (HC55142). The second portion of the file name is the line impedance the coefficients are matching (600Ω) and the last portion is the channel (1).

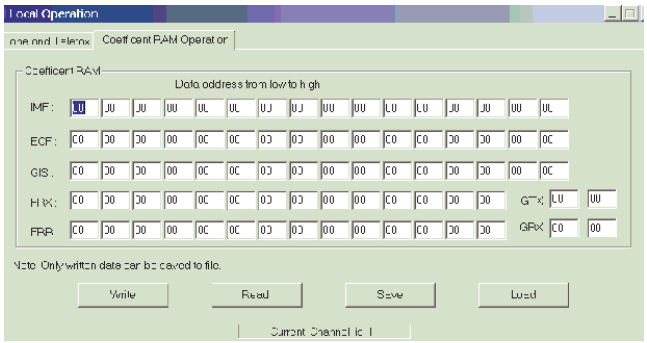


FIGURE 8. COEFFICIENT RAM OPERATION SCREEN

Loading Coefficients

If previous test was Test #1, #2 or #3, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started".

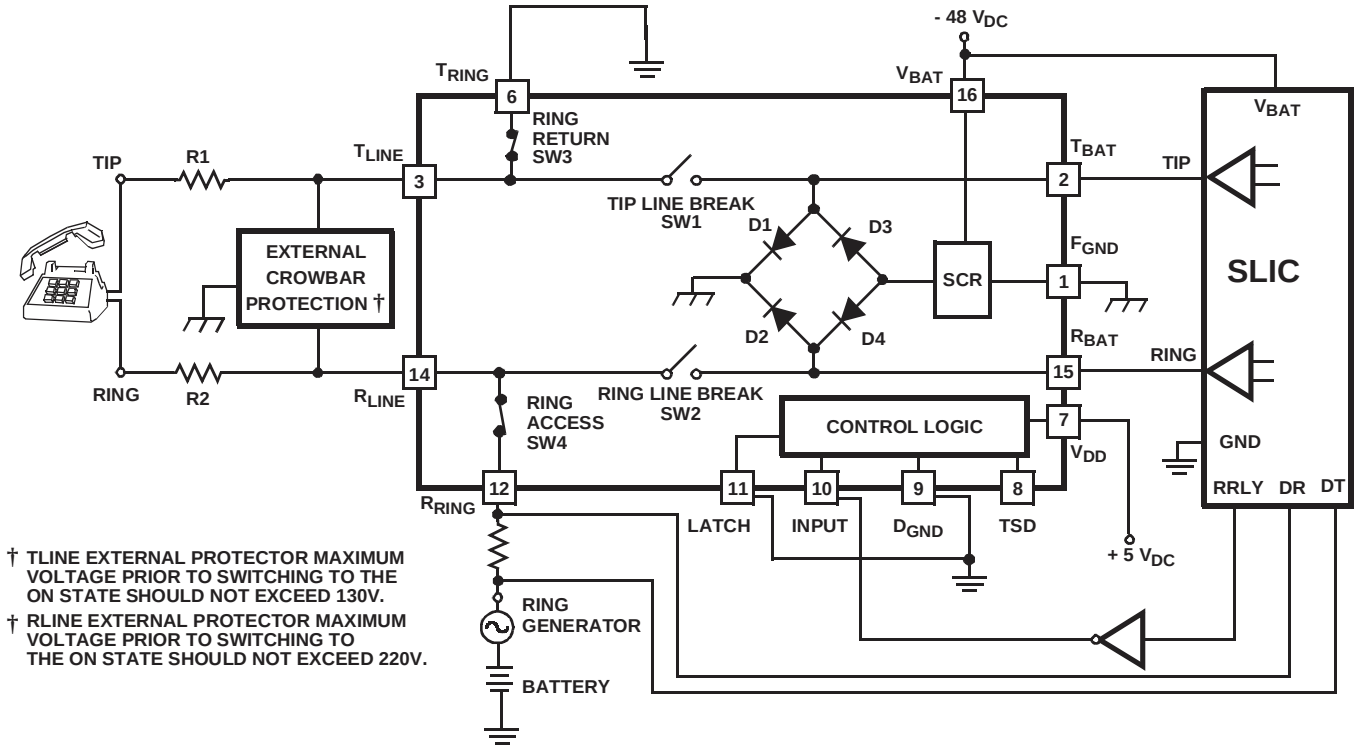


FIGURE 9. APPLICATION CIRCUIT

TABLE 2. TRUTH TABLE - ISL5571A

	LOGIC INPUTS			SWITCH CONDITION			
LOGIC STATE	LATCH	INPUT	T_{SD}	TIP LINE BREAK SWITCH	RING LINE BREAK SWITCH	RINGING RETURN SWITCH	RING ACCESS SWITCH
IDLE / TALK	0	0	1 or Floating (Note 11)	ON	ON	OFF	OFF
POWER RINGING	0	1	1 or Floating (Note 11)	OFF	OFF	ON	ON
IDLE / TALK LATCHED (Note 12)	1	0	1 or Floating (Note 11)	ON	ON	OFF	OFF
POWER RINGING LATCHED (Note 12)	1	1	1 or Floating (Note 11)	OFF	OFF	ON	ON
All OFF	X	X	0 (Note 13)	OFF	OFF	OFF	OFF

NOTES:

1. Thermal shutdown mechanism is active with TSD floating or equal to 5V.
2. If the LATCH pin is low, the logic state of the device is controlled by the INPUT pin. When the LATCH pin goes high, the current logic state is latched. As long as the LATCH pin is held high, the device will no longer respond to any changes applied to the INPUT control pin. The state of the device will be permanently latched until the LATCH pin is taken low.
3. Setting TSD to a logic low overrides the LATCH and INPUT logic pins and forces all switches to turn OFF.

2. Configure Mother Board for Emulation Mode. Verify:

- Jumper JP1 is IN,
- JP2 is IN,
- JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section “Getting Started”), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select the desired Channel by clicking on the channel button in the left shaded area
4. From MPI Software screen, Select COF RAM. The Coefficient Ram Operation screen will appear (Figure 8).

Down loading Coefficients from a File:

•Click on Load and the desk top window opens. Navigate to where the file is stored and select the coefficients for the channel being programmed. Opening the file will automatically load the coefficients into COF RAM screen. Another window will appear to inform you that the file successfully loaded.

•Click OK. Exit the screen by clicking the Close button (don’t write files from this screen). This will return you to the MPI Software screen. Click Write from this screen.

5. Repeat steps 3 and 4 to load the coefficients for the other channels.

Test # 5 Emulation of Phone Conversation

This test will demonstrate an end to end phone conversation between Channel 1 and Channel 2. Setting up an end to end phone conversation is accomplished with the Timeslot and PCM Highway Assignment screen (Figure 10). The user can select any time slot for Channels transmit and receive. If the time slot assigned to the receive path of Channel X is the same one assigned to the transmit path of Channel Y, and the time slot assigned to the transmit path of Channel X is the same one assigned to the receive path of Channel Y, then Channel X and Channel Y can communicate with each other.

Assigning Timeslots

If previous test was Test #1, #2, #3 or #4, skip to step 3.

1. Configure Hardware and Software as described in section titled” Getting Started”
2. Configure Mother Board for Emulation Mode. Verify:

•Jumper JP1 is IN,

•JP2 is IN,

•JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section “Getting Started”), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select Dual Tone Setting and verify that both the High Tone and Low Tone are Disabled. This will prevent the high or low tone signals from interfering with the Channel to Channel communication.
4. From MPI Software screen, Select Timeslot. The Timeslot and PCM Highway Assignment screen will appear (Figure 10).
5. For communications between Channel 1 and Channel 2, one possible configuration is:
   Set Channel 1 Transmit = 000, DX1
   Set Channel 1 Receive = 001,DR1
   Set Channel 2 Transmit = 001,DX1
   Set Channel 2 Receive = 000, DR1
6. Set the transmit and receive paths as shown in step 5 and click the Write button.
7. Connect Phones to the RJ11 jacks of both Channels 1 and Channel 2. Communication between Channels 1 and 2 is now possible.

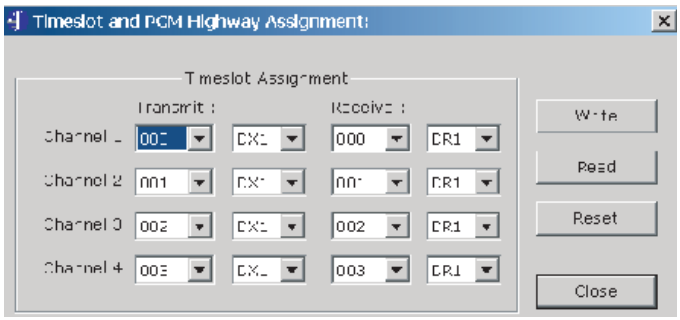
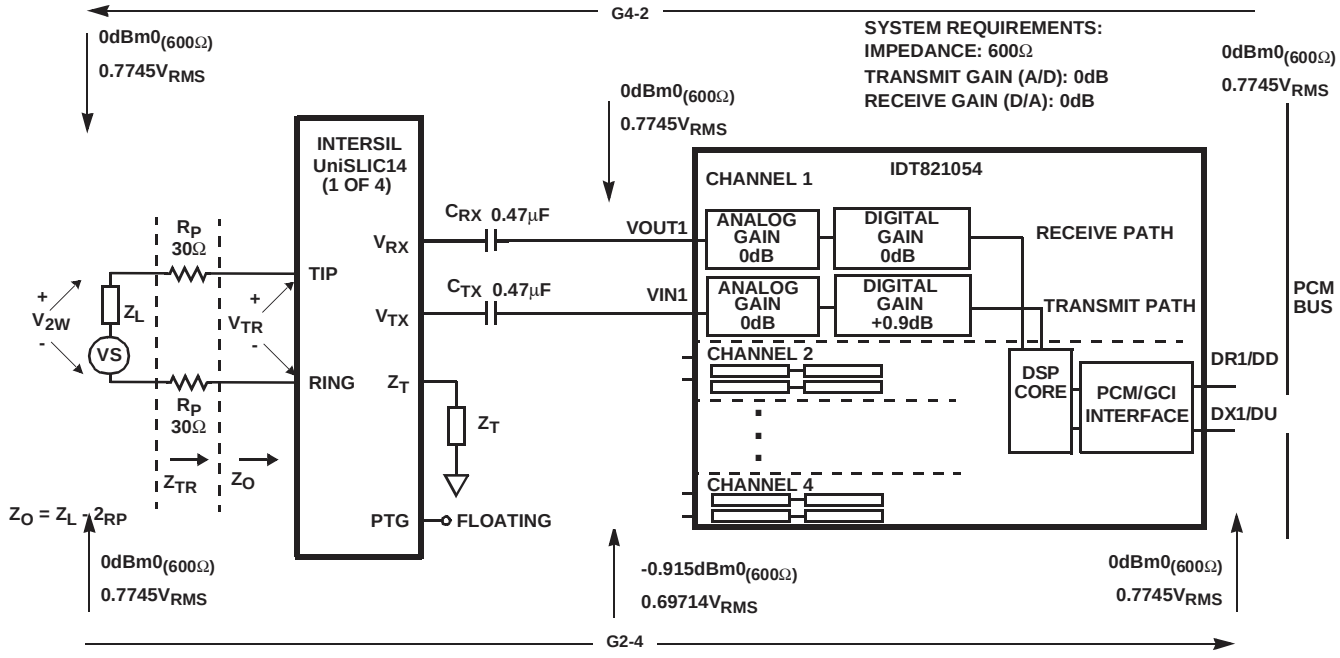


FIGURE 10. TIMESLOT & PCM HIGHWAY ASSIGNMENTS

Test # 6 Gain Verification

This test will verify the gains through the IDT821054 and the UniSLIC14 are operating properly. The test will show, with the proper coefficients loaded into the CODEC, the Digital to Analog gain across both the CODEC and the SLIC is equal to -1.0 (0.0dB), and the Analog to Digital gain across both the SLIC and the CODEC is also equal to 1.0 (0dB). Both D/A and A/D gains will be verified by performing a Digital to Digital gain using the PCM4.

Figure 11 shows the reference design of the UniSLIC14 and the IDT821054 with a 600Ω load impedance and transmit and receive gains of 0dB. Reference AN9999 for a detailed engineering analysis of the reference design.



NOTE: Reference Table 1 Application Note AN9999 for coefficients.

FIGURE 11. REFERENCE DESIGN OF THE UniSLIC14 AND THE IDT821054 WITH A 600Ω LOAD IMPEDANCE

Total System Gain (D/D)

If previous test was Test #1, #2, #3, #4 or #5, skip to step 2.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Prerequisite for this test is that test #4 "Programming of Coefficients" be completed using the 600Ω coefficients, system gains: (A/D = 0dB, D/A = 0dB) and CODEC analog gains: (A/D = +6dB, D/A = 0dB) Table 1 of application note AN9999.
3. Terminate tip and ring with a 600Ω load via the RJ11 jack.
4. Configure Mother Board for TEST Mode. Verify:

- Jumper JP1 is OUT,
- JP2 is OUT,
- JP3 is set to External BCLK.

   Note: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

5. Set the General Parameters of the PCM4 as shown in Table 3.
6. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel 1 PCM time slot. To test channel 2 of the Mother Board, set the PCM4 to channel 1. Continue this pattern for remaining channels.
7. From MPI Software screen, set the A/D (Transmit) Gain = 0dB and the D/A (Receive) Gain = 0dB.
8. Configure the PCM4 for the MODE A 11 test. Set PCM4 to D-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 12

TABLE 3. PCM4 GENERAL PARAMETERS SETTINGS

GENERAL PARAMETER	SETTING	PARM
(1) Digital Configuration:		
General configuration	TX/RX 2M/2Mbits/s selected	11
Digital Loop (A - A)	OPEN/AUX.SIGN.	23
(2) Frame Selection:		
TX frame type	All 32 TS teleph	14
RX frame type	All 32 TS teleph	24
CRC-4 Multiframe	Off	31
(3) Digital TX Interface:		
Line Code	NRZ	13
Output Impedance	75 ohms unbalanced	22
Clock	Int. 2048 kHz	31
(4) Digital RX I nterface:		
Line Code	NRZ	13
Input Impedance	> 3kΩ	22
(5) Digital Words in TX Frame:	Reset to standard values	11
Frame Words	ALL CHAN.	22
Send Signal		
(6) TX Error Insertion	Off	11
(7) PCM Coding:		
TX Encoding Law	Must match switch S7-6 on IDT821054 EVM. Default setting on EVM is A-law	11
RX Encoding Law	Must match encoding law	21

TABLE 3. PCM4 GENERAL PARAMETERS SETTINGS (Continued)

GENERAL PARAMETER	SETTING	PARM
(8) Scanner Parameter:		
VF-Input no.	1	11
VF-Output no.	1	21
(9) Special Parameter:		
Level Display	dBm0	11
Two wire Term.	Infinite	13
Digital Channel no.	Time Slot	16
	Mark and cont.	22
Tolerance mask set 2		23
	Mark and cont.	27
Clock display	OFF	33
OFF		35

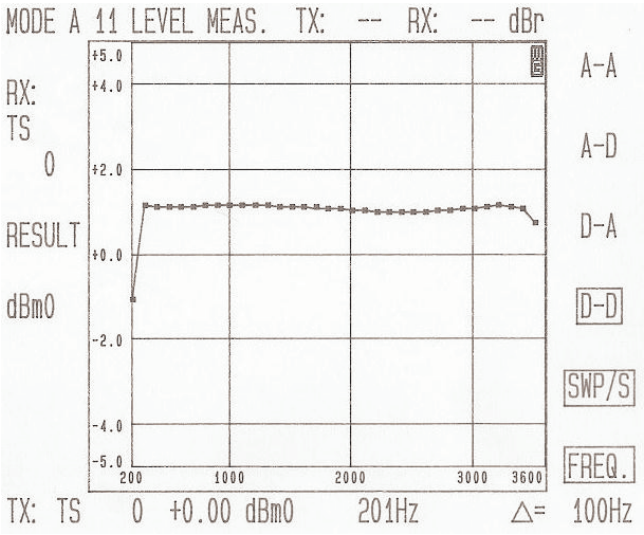


FIGURE 12. TOTAL SYSTEM GAIN (D/D)

Test # 7 Variation of Gain / Frequency

This test will configure the UniSLIC14 in the loopback mode and evaluate the IDT821054 and the UniSLIC14's AC performance across frequency.

Discussion

Most of the SLICs in the UniSLIC14 family feature 2-Wire loopback testing. During the 2-wire loopback test, a 2kΩ internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{SHD}$ function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested.

Variable Gain / Frequency (D/A) Test #7a

If previous test was Test #1, #2, #3, #4, or #5, skip to step 2. If previous test was Test # 6 skip to step 7.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Prerequisite for this test is that test #4 "Programming of Coefficients" be completed using the 600Ω coefficients, system gains: (A/D = 0dB, D/A = 0dB) and CODEC analog gains: (A/D = +6dB, D/A = 0dB) Table 1 of application note AN9999.
3. Configure Mother Board for TEST Mode. Verify:

- Jumper JP1 is OUT,
- JP2 is OUT,
- JP3 is set to External BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

4. Set the General Parameters of the PCM4 as shown in Table 3.
5. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel 1 PCM time slot. To test channel 2 of the Mother Board, set the PCM4 to channel 1. Continue this pattern for remaining channels.
6. From MPI Software screen, set the A/D (Transmit) Gain = 0dB and the D/A (Receive Gain) = 0dB.
7. Remove the 600Ω load from across tip and ring.
8. From MPI Software screen, Select: Active F and then Test A F, TSD, Power On.
9. Configure the PCM4 for the MODE A 33 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 13.

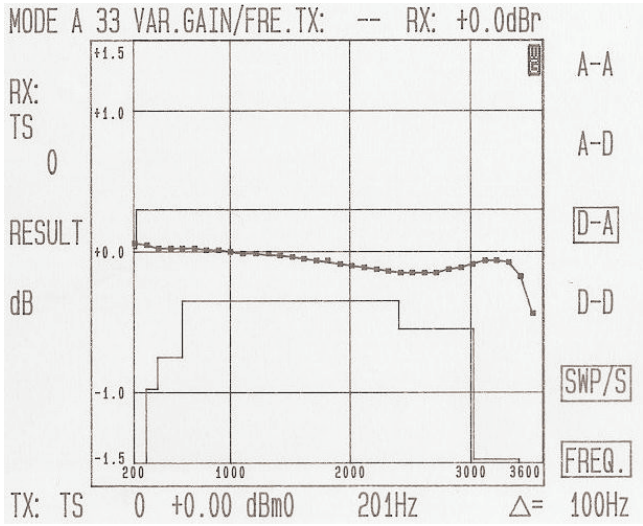


FIGURE 13. (D/A) VARIABLE GAIN vs. FREQUENCY

Variable Gain / Frequency (A/D) Test #7b

1. Configure the PCM4 for the MODE A 33 test. Set PCM4 to A-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 14.

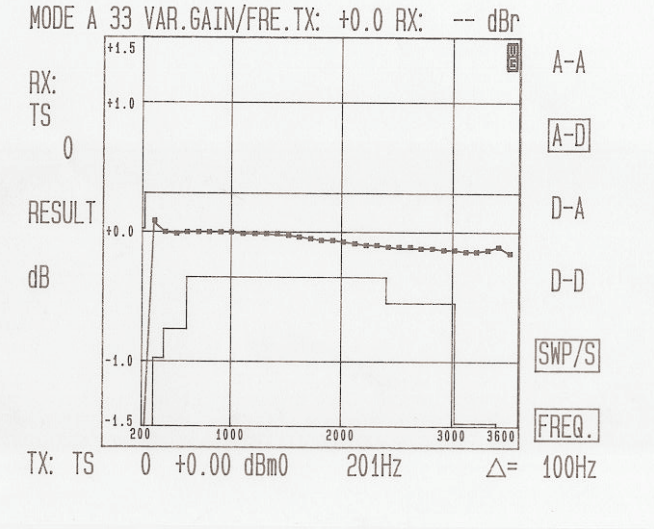


FIGURE 14. (A/D) VARIABLE GAIN vs. FREQUENCY

Test # 8 Total Distortion

This test will configure the UniSLIC14 in the loopback mode and evaluate the IDT821054 and the UniSLIC14's Total Distortion.

Total Distortion (D/A) Test #8a

If previous test was Test # 1, #2, #3, #4, or #5, skip to step 2.
If previous test was Test # 6 skip to step 7.
If previous test was Test #7a/b skip to step 9.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Prerequisite for this test is that test #4 "Programming of Coefficients" be completed using the 600Ω coefficients, system gains: (A/D = 0dB, D/A = 0dB) and CODEC analog gains: (A/D = +6dB, D/A = 0dB) Table 1 of application note AN9999.
3. Configure Mother Board for TEST Mode. Verify:
   •Jumper JP1 is OUT,
   •JP2 is OUT,
   •JP3 is set to External BCLK.
   NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.
4. Set the General Parameters of the PCM4 as shown in Table 3.
5. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel 1 PCM time slot. To test channel 2 of the Mother Board, set the PCM4 to channel 1. Continue this pattern for remaining channels.
6. From MPI Software screen, set the A/D (Transmit) Gain = 0dB and the D/A (Receive Gain) = 0dB.
7. Remove the 600Ω load from across tip and ring.
8. From MPI Software screen, Select: Active F and then Test A F, TSD, Power On.
9. Configure the PCM4 for the MODE A 55 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 15.

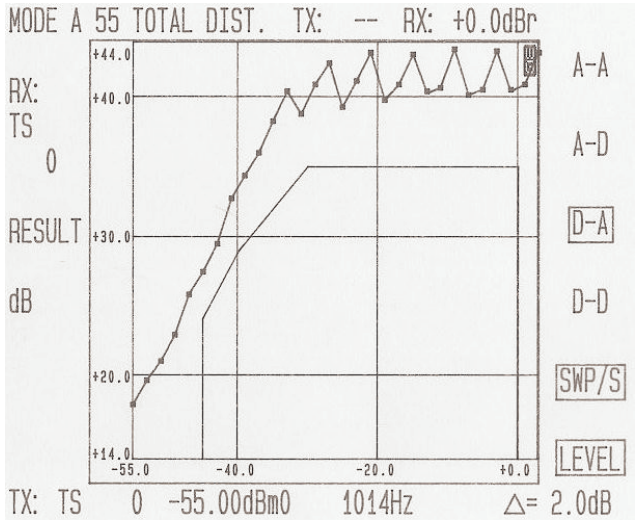


FIGURE 15. (D/A) TOTAL DISTORTION

Total Distortion (A/D) Test #8b

1. Configure the PCM4 for the MODE A 55 test. Set PCM4 to A-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 16.

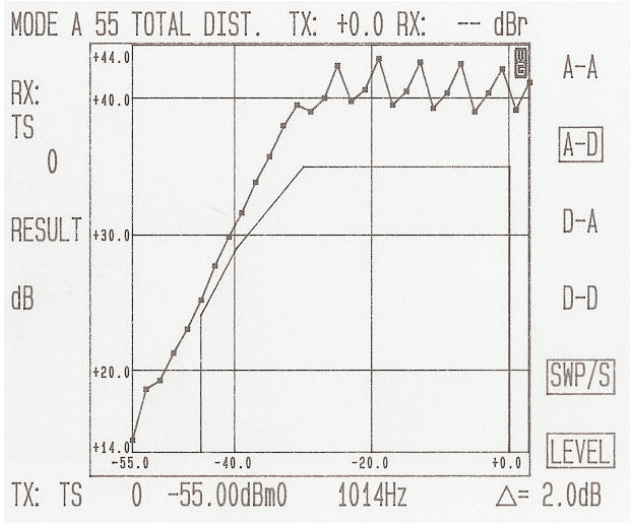


FIGURE 16. (A/D) TOTAL DISTORTION

Layout Considerations

Systems with Dual Supplies (V_{BH} and V_{BL})

If the V_{BL} supply is ***not*** derived from the V_{BH} supply, it is recommended that an additional diode be placed in series with the V_{BH} supply (D3 and D6 Figure 17). The orientation of this diode is anode on pin 8 of the device and cathode to the external supply. This external diode will inhibit large currents and potential damage to the SLIC, in the event the V_{BH} supply is shorted to GND. If V_{BL} is derived from V_{BH} then this diode is not required.

Floating the PTG Pin

The PTG pin is a high impedance pin (500kΩ) that is used to program the 2-wire to 4-wire gain to either 0dB or -6dB.

If 0dB is required, it is necessary to float the PTG pin. The PC board interconnect should be as short as possible to minimize stray capacitance on this pin. Stray capacitance on this pin forms a low pass filter and will cause the 2-wire to 4-wire gain to roll off at the higher frequencies.

If a 2-wire to 4-wire gain of -6dB is required, the PTG pin should be grounded as close to the device as possible.

SPM Pin

For optimum performance, the PC board interconnect to the SPM pin should be as short as possible. If pulses metering is not being used, then this pin should be grounded as close to the device pin as possible.

RLIM Pin

The current limiting resistor R_{LIM} needs to be as close to the RLIM pin as possible.

Layout of the 2-Wire Impedance Matching Resistor Z_T

Proper connection to the ZT pin is to have the external Z_T network as close to the device pin as possible.

The ZT pin is a high impedance pin that is used to set the proper feedback for matching the impedance of the 2-wire side. This will eliminate circuit board capacitance on this pin to maintain the 2-wire return loss across frequency.

Daughter Board Schematic

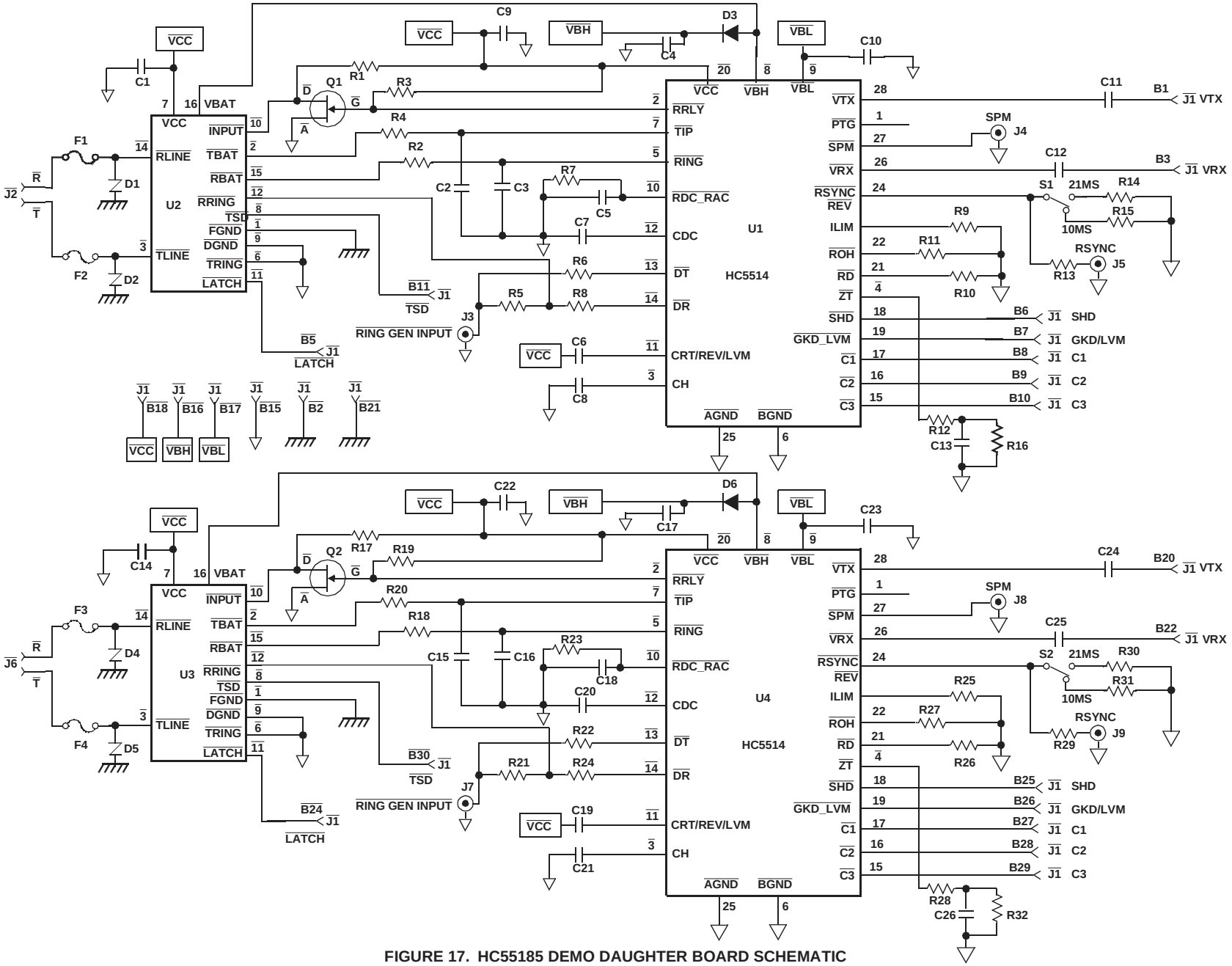


FIGURE 17. HC55185 DEMO DAUGHTER BOARD SCHEMATIC

TABLE 4. DAUGHTER BOARD COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1, U4 - SLIC	UniSLIC14 Family	N/A	N/A
U2, U3 - LCAS	ISL5571A	N/A	N/A
R1, R17	10K	1%	1/16W
R3, R19	1K	1%	1/16W
R2, R4, R18, R20 (Line feed resistors)	30Ω	Matched 1%	2.0W
R7, R23 (RDC_RAC) R = 50*RFEED, RFEED = 381Ω	21.0kΩ	1%	1/16W
R6, R8, R22, R24 (Input current limiting resistors for DT and DR)	3MΩ	1%	1/16W
R10, R26 (RD resistor) R = 500/I_{SH}, I_{SH} = 9.78mA	41.2kΩ	1%	1/16W
R11, R27 (ROH resistor) R = 500/Iloop(min)-I_{SH}- (Iloop(min) = 20mA, I_{SH}- 6.54mA)	38.3kΩ	1%	1/16W
R9, R25 (R_{ILIM} resistor) R = 1000/ILIM (ILIM = 30mA)	33.2kΩ	1%	1/16W
R15, R31 (RSYNC_REV resistors) R = 3.47k/µs (10ms)	34.8kΩ	1%	1/16W
R12, R28 (RZT, 2-Wire Impedance Matching Resistor) R = 200(ZO-2RF) Z0 = 600Ω, RF = 30Ω	107KΩ	1%	1/4W
R13,R29 (Current limit resistor for Ring Sync Pulse)	49.9kΩ	1%	1/16W
R14, R30 (RSYNC_REV resistor) R = 3.47k/µs (21ms)	69.8kΩ	1%	1/16W
R5, R21 (Sense resistor for DC current during ringing)	400Ω	1%	2W
R16, R32, C13,C26 (For matching a complex 2-Wire impedance)	R16, R32 = 0Ω C13, C26 = Open	-	-
C1, C8, C9, C14, C21, C22	0.1µF	20%	10V
C10, C23	0.1µF	20%	50V
C7, C20	4.7µF	10%	50V or (V_{BH}/2)
C5, C6, C11, C12, C18, C19, C24, C25	0.47µF	20%	10V
C4, C17	0.1µF	20%	100V
C2, C3, C15, C16	2200pF	20%	100V
D3,D6 Recommended if the V_{BL} supply is not derived from the V_{BH} supply.	1N4004	-	-
Q1, Q2	IRFD120		
F1, F2, F3, F4	F1250T		
D1, D4	P2000SC		
D2, D5	P1200SC		

Design Parameters: Switch Hook Threshold = 12mA, Loop Current Limit = 30mA, Synthesize Device Impedance = 600-60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.