Operation of the UniSLIC14 Family of SLICs Evaluation Board

Application Note | February 2001 | AN9871.1

Functional Description

Evaluation Board

The HC5514X evaluation board, due to the common pinout of the UniSLIC14 family, is capable of evaluating the performance of the following parts in the UniSLIC14 family (HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150).

This evaluation board also has provisions for the evaluation of the 758XX Access Switch, which is not covered in this application note. For information about the operation of the Access Switch reference application note AN9870 “Operation of the 758XX Line Card Access Switch”.

The sample provided with this board (HC5514X) will illustrate the electrical performance for all members of the family listed above. The board is configured to match a 600Ω line impedance, have a minimum loop current of 20mA, a maximum loop current of 30mA, onhook transmission of $0.775V_{RMS}$, offhook voice transmission of $3.2V_{PEAK}$, and a maximum loop resistance of 1777Ω.

For evaluation of the programmability of the HC5514 family, reference the data sheet for calculation of external components. An Excel spread sheet can be downloaded from the web for easy calculation of external components (www.intersil.com/telecom/unislic14.xls).

The board is equipped with eleven Single Pole Double Throw (SPDT) switches. The switches control the logic state and performance of the HC5514 and the 758XX Access Switch.

The logic control (C3, C2, C1), $\overline{SHD}$ and $\overline{GKD}/\overline{LVM}$ switches are center open toggle switches. If off-board mode control of the SLIC is desired, these switches can be set to center open position and driven by logic at the logic terminal port. The logic terminal port is located at the bottom right hand side of the board.

The logic control for the Access Switch (lower left hand side of the board) can also be set to center open position and driven by logic at the logic terminal port if desired.

Power Requirements for the HC5514X

Power Supply Connections

The HC5514X requires as many as three external power supplies. V_{BH} = -48V (Typ), V_{BL} = -24V (Typ) and V_{CC} = +5V. If the design requires only two supplies, it is recommended that the V_{BL} supply pin float.

Ground Connections

The three external power supplies should each be grounded at the evaluation board.

Features

- Toggle Switch Programming for Logic States
- Monitoring of Switch Hook Detect ($\overline{SHD}$) and Ground Key / Line Voltage Measurement ($\overline{GKD}\_\overline{LVM}$) via On Board LEDs
- Selectable Transmit Gain 0dB/-6dB
- Selectable Power Sharing
- Single/Dual Battery Operation
- Logic Terminal Port for Easy Evaluation in Existing Systems
- Includes a Ring Relay for Evaluation of Ring Trip and Provisions for Evaluation of Intersil’s 758XX Linecard Access Switch
- Selectable/Programmable Polarity Reversal Time
- Programmable 2-Wire Impedance
- Programmable Loop Detect Threshold
- Programmable Onhook and Offhook Overheads
- Provisions for Pulse Metering
- Provisions for Internal Transhybrid Balance
- Provisions for Line Voltage Measurement Test

Getting Started

Verify that the sample is oriented in its socket correctly. Correct orientation is with pin 1 pointing towards the top of the board (tip and ring terminals to the left). (Reference the data sheet for device pinout.)

Verifying Basic SLIC Operation

The operation of the sample part can be verified by performing the following tests: (The board comes with a standard ring relay. The following set of tests, evaluate the operation of the HC5514X with the ring relay.)

1. Power Supply Current Verification
   - Forward Active and Reverse States
2. Normal Loop Feed Verification
   - Forward Active and Reverse Active States
3. Gain Verification
   - 4-Wire to 2-Wire and 2-Wire to 4-Wire
4. Polarity Reversal Time
5. Battery Selection/Power Sharing
6. Ring Trip Verification
7. Pulse Metering
8. Transhybrid Balance
9. Line Voltage Measurement Test

The evaluation of all 9 tests require the following equipment: a 600Ω (1 watt, 1%) load, a 1777Ω (2 watt, 1%) load, a 26.1kΩ (1/4 watt, 1%) RDC_RAC resistor, two sine wave generators, an AC/DC volt meter, three external supplies (V_{BH}, V_{BL}, V_{CC}), a dual channel storage oscilloscope, a telephone, BNC to banana adaptor, a battery backed AC source and a dynamic signal analyzer.

Application Tip: When terminating tip and ring, it is handy to assemble terminators using a Pomona MDP dual banana plug connector as the terminating resistor receptacle. Refer to Figure 1 for details.

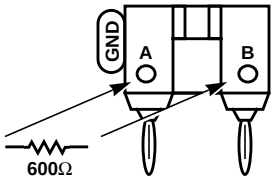

FIGURE 1. TERMINATION ADAPTER

Using the termination shown in Figure 1 provides an unobtrusive technique for terminating tip and ring while still providing access to both signals using the banana jack feature of the MDP connector. Posts are also available that fit into holes A and B, providing a solderable connection for the terminating resistor.

Test #1, Power Supply Current Verification

A quick check of the evaluation board and sample is to measure the supply currents. The readings should be similar to the values listed in Table 1. The measurements can be made using a series ammeter on each supply, or power supplies with current displays.

Setup

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Verify the thermal management switch (S9, located towards the top middle of the board) is in the $V_{BL} = V_{BL}$ position.
4. Verify that the POL/REV switch S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Configure the $\overline{SHD}$ switch (S5) to be in the JACK position. This will allow an accurate reading of the V_{CC} current by removing the $\overline{SHD}$ LED current.
6. Configure the $\overline{GKD}\_\overline{LVM}$ switch (S6) to be in the BNC position. This will allow an accurate reading of the V_{CC} current by removing the $\overline{GKD}\_\overline{LVM}$ LED current.
7. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0). Measure the supply currents and compare to those in Table 1.
8. Terminate tip and ring with a 600Ω load. Measure the supply currents and compare to those in Table 1. Remove 600Ω load.
9. Configured the SLIC in the reverse active state (C3 = 1, C2 = 1, C1 = 0). Measure the supply currents and compare to those in Table 1. Repeat step 8.

TABLE 1. SUPPLY CURRENTS AND POWER DISSIPATIONS

LOGIC STATE	R_L (Ω)	SUPPLY VOLTAGE (DC)	SUPPLY CURRENT TYP (mA)	POWER DISSIPATION (mW)
Forward Active	Onhook Without Load	V_{BH} = -48V	0.8	38.4
		V_{BL} = -24V	0.0001	0.0024
		V_{CC} = +5V	2.91	14.5
Forward Active	Offhook with 600Ω Load	V_{BH} = -48V	30.0	1440
		V_{BL} = -24V	2.68	64.3
		V_{CC} = +5V	4.2	21
Reverse Active	Onhook Without Load	V_{BH} = -48V	0.85	40.8
		V_{BL} = -24V	0.0001	0.0024
		V_{CC} = +5V	2.97	14.8
Reverse Active	Offhook with 600Ω Load	V_{BH} = -48V	29.74	1427
		V_{BL} = -24V	1.9	45.6
		V_{CC} = +5V	4.27	21.3

Test #2, Normal Loop Feed Verification

This test verifies the correct tip and ring voltages in both onhook and offhook forward active and reverse active states. Loop current and ground key detect are also verified via the onboard $\overline{SHD}$ and $\overline{GKD}\_\overline{LVM}$ LEDs.

Discussion

The HC5514 is designed to have its most positive 2-wire terminal (tip in the forward active state and ring in the reverse active state) fixed at a set voltage. This set voltage depends upon the required overheads for the application. The most negative 2-wire terminals voltage is dependent upon the load across tip and ring and the programmable current limit.

The tip and ring voltages for various loop resistances are shown in Figure 2. The tip voltage remains relatively constant as the ring voltage moves to limit the loop current for short loops.

When power is applied to the SLIC, a loop current will flow from tip to ring through the 600Ω load. Loop current detection occurs when this loop current triggers an internal detector that pulls the output of $\overline{SHD}$ low, illuminating the LED through the +5V supply.

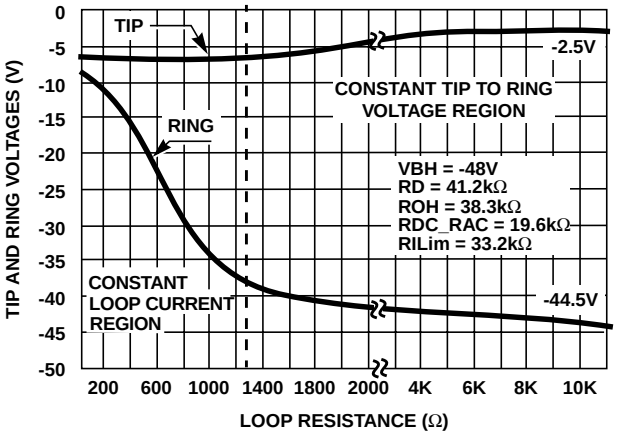

FIGURE 2. TIP AND RING VOLTAGES vs LOOP RESISTANCE

The Ground Key detector ($\overline{GKD}$) operation is verified by configuring the HC5514X in the tip open state and grounding the ring pin. Grounding the ring pin results in a current that triggers an internal detector that pulls the output of $\overline{GKD}\_\overline{LVM}$ low, illuminating the LED through the +5V supply.

Setup (Tip and Ring Voltages)

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
4. Verify that the POL/REV pin (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Configure S5 and S6 switches to be in the LED position.
6. Disconnect any loads from across tip and ring.
7. Measure tip and ring voltages with respect to ground and compare to those in Table 2 (onhook).
8. Terminate tip and ring with a 600Ω load.
9. Measure tip and ring voltages with respect to ground and compare to those in Table 2 (600Ω).
10. Configure the SLIC to be in the Reverse Active State (C3 = 1, C2 = 1, C1 = 0).
11. Repeat steps 6 through 9.

TABLE 2. TIP AND RING VOLTAGES

HC5514X			
LOGIC STATE	**R_L (Ω)**	**TIP VOLTAGE REFERENCE D TO GND**	**RING VOLTAGE REFERENCED TO GND**
Forward Active V_{BH} = -48V V_{BL} = -24V V_{CC} = +5V	Onhook	-2.6	-44.6
	Offhook 600	-6.3	-24.5
Reverse Active V_{BH} = -48V V_{BL} = -24V V_{CC} = +5V	Onhook	-44.6	-2.5
	Offhook 600	-24.4	-6.3

Verification of $\overline{SHD}$:

1. With the SLIC in the forward active state, the $\overline{SHD}$ LED is on when tip and ring are terminated with 600Ω and off when tip and ring are an open circuit.

Verification of $\overline{GKD}$:

1. Configure the SLIC to be in the Tip Open State (C3 = 1, C2 = 0, C1 = 0).
2. The $\overline{GKD}\_\overline{LVM}$ LED is on when ring is shorted to ground and off when ring is an open circuit. Notice that the $\overline{SHD}$ LED will also be on.

Test #3, Gain Verification

This test will verify the SLIC is operating properly and that the 4-wire to 2-wire gain (Equation 1) is -1.0 (0.0dB).

$$A_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_{TR}} = -2\frac{Z_L}{Z_L + \left(\frac{Z_T}{200} + 2R_P\right)} \quad \text{(EQ. 1)}$$

The programmable 2-wire to 4-wire transmission gain (Equation 2) will also be verified by measuring the SLIC's 4-wire to 4-wire gain with the PTG pin floating ($A_{2\text{-}4}$ is 0.9 (0.91dB) and grounded ($A_{2\text{-}4}$ is 0.56 (-5.0dB).)

$$A_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_{TR} - 2R_P}{Z_{TR}} \quad \text{(EQ. 2)}$$

Discussion

When tip and ring are terminated with 600Ω load, the SLIC will exhibit unity gain from the 4-wire VRX input pin to across the 2-wire tip and ring pins (V_{TR}). The dB gain is calculated in Equation 3. When an open circuit exists, a mismatch occurs and the tip to ring voltage doubles.

An easy way to measure the 2-wire to 4-wire transmit gain, without a floating signal generator on the 2-wire side, is to measure the 4-wire to 4-wire gain. This way the source can be applied on the ground referenced 4-wire side to the VRX pin. Given that the 4-wire to 2-wire gain is approximately one, it follows that the 2-wire to 4-wire transmission gain is also approximately equal to the 4-wire to 4-wire gain. The dB 4w to 4w gain is calculated in Equation 4.

$$dB_{4W-2W} = 20\log\frac{V_{TR}}{V_{RX}} \quad \text{(EQ. 3)}$$

$$dB_{4W-4W} = 20\log\frac{V_{TX}}{V_{RX}} \quad \text{(EQ. 4)}$$

Setup (4-Wire to 2-Wire Gain)

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
4. Verify that the POL/REV pin S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Terminate tip and ring with a 600Ω load.

6. Connect a sine wave generator, referenced to ground, to the VRX input.
7. Set the generator for $1V_{RMS}$ at 1kHz.
8. Connect an AC voltmeter across tip and ring.

Verification

1. Tip to ring AC voltage of $1V_{RMS}$ when terminated with a 600Ω load. The dB (A_{4-2}) gain is approximately 0dB.
2. Tip to ring AC voltage of $2V_{RMS}$ when not terminated. The dB (A_{4-2}) gain is approximately 6dB.
3. Configure the SLIC to be in the Reverse Active state (C3 = 1, C2 = 1, C1 = 0) and repeat above test.

Setup (2-Wire to 4-Wire Gain)

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
4. Verify that the POL/REV pin (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Terminate tip and ring with a 600Ω load.
6. Verify that pin 2 of the PTG jumper (S8, located towards the middle of board near the upper right hand corner of the SLIC) is floating. This condition floats the PTG pin. Reference section titled “Layout Considerations” for more information about the PTG pin.
7. Connect a sine wave generator, referenced to ground, to the VRX input.
8. Set the generator for $1V_{RMS}$ at 1kHz.
9. Connect an AC voltmeter, referenced to ground, to the VTX output.

Verification

1. VTX voltage of $1V_{RMS}$ when pin 2 of the PTG jumper is floating. The dB (A_{2-4}) gain is approximately -0.9dB.
2. VTX voltage of $0.5V_{RMS}$ when pin 2 of the PTG jumper is shorted to pin 1, via the supplied jumper. This condition grounds the PTG pin. The dB (A_{2-4}) gain is approximately -5.0dB.
3. Configure the SLIC to be in the Reverse Active state (C3 = 1, C2 = 1, C1 = 0) and repeat above test.

Test #4, Polarity Reversal Time

This test will illustrate the operation and programming of the polarity reversal feature.

Discussion

The HC5514X has a programmable polarity reversal time. The evaluation board is equipped with a toggle switch for evaluation of a 10µs and 20µs reversal times. Equation 5 gives the formula for programming a desired reversal time.

$$RSYNC\text{–}REV = (3.47k\Omega)(ReversalTime(ms)) \quad \text{(EQ. 5)}$$

$$34.7k\Omega < RSYNC\text{–}REV > 73.2k\Omega$$

Capacitor C4 performs three different functions, ring trip filtering, polarity reversal time and line voltage measurement. C4 and R7/R10 set the timing for the polarity reversal time. It is recommended that programming of the reversal time be accomplished by changing the value of R7/R10 (see Figure 7).

Setup

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
4. Remove Generator.
5. Verify that the POL/REV pin S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
6. Terminate tip and ring with a 600Ω load.
7. Select either 10µs or 20µs polarity reversal time via the POL / REV switch at the bottom right hand side of the board.
8. Monitor the tip and ring voltage levels with a dual channel storage scope. Toggle the SLIC between the Forward Active state and the Reverse Active states to trigger the scope.
9. Measure the time of reversal. Compare results to that listed in Table 3.
10. Switch the POL / REV (S4) switch to the other reversal time and compare results to that listed in Table 3.

TABLE 3. POLARITY REVERSAL TIME

POLARITY REVERSAL SWITCH SETTING	FORWARD ACTIVE TO REVERSE	REVERSE ACTIVE TO FORWARD
10µs	≈10µs	≈10µs
20µs	≈20µs	≈20µs

Test #5, Battery Selection/Power Sharing

Discussion (Battery Selection)

This test will illustrate the automatic switching of the supplies by monitoring the V_{BH} and V_{BL} supply currents during onhook and offhook with a 600Ω load across tip and ring.

Battery selection is a technique, for a two battery supply system, where the SLIC automatically diverts the loop current to the most appropriate supply for a given loop length. This results in significant power savings and lowers the total power consumption on short loops. This technique is particularly useful if most of the lines are short, and the on hook condition requires a -48V battery. In Figure 3, it can be seen that for long loops the majority of the current comes for the high battery supply (V_{BH}) and for short loops from the low battery supply (V_{BL}).

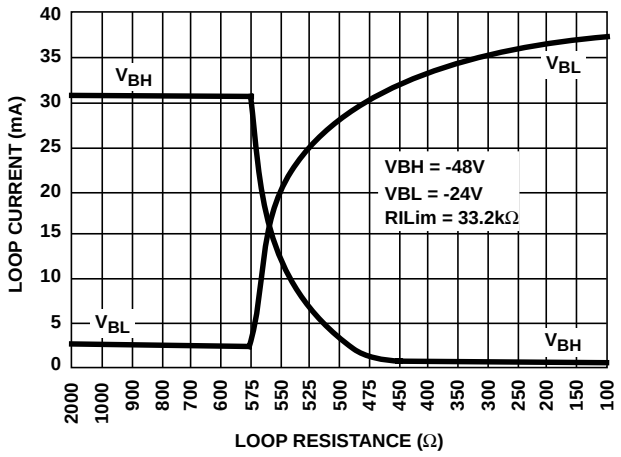

FIGURE 3. BATTERY SELECTION (DUAL SUPPLY SYSTEMS)

Setup

1. Reference Test #1 “Power Supply Current Verification” and the results in Table 1.

Verification

1. Notice for the onhook condition (extremely long line) that all the current is provided by V_{BH}. This feature enables onhook transmission on the longest loop for a given battery voltage.
2. Notice for a 600Ω load, the current is shared by both V_{BH} and V_{BL}. If tip and ring are shorted, then most of the loop current will come from V_{BL}.
3. Notice the same is true for the reverse active state.

Discussion (Power Sharing)

Power sharing is a method of redistributing the power away from the SLIC in short loop applications. The total system power is the same, but the die temperature of the SLIC is much lower. Power sharing becomes important if the application has a single battery supply (-48V on hook requirements for faxes and modems) and the possibility of high loop currents (reference Figure 4). This technique would prevent the SLIC from getting too hot and thermally shutting down on short loops.

The power dissipation in the SLIC is the sum of the smaller quiescent supply power and the much larger power that results from the loop current. The power that results from the loop current is the loop current times the voltage across the SLIC. The power sharing resistor (R_{PS}) reduces the voltage across the SLIC, and thereby the on-chip power dissipation. The voltage across the SLIC is reduced by the voltage drop across R_{PS}. This occurs because R_{PS} is in series with the loop current and the negative supply.

A mathematical verification follows:

Given: $V_{BH} = V_{BL}$ = -48V, Loop current = 30mA, R_L (load across tip and ring) = 600Ω, Quiescent battery power = (48V) (0.8mA) = 38.4mW, Quiescent VCC power = (5V) (2.7mA) = 13.5mW, Power sharing resistor = 600Ω.

1. Without power sharing, the on-chip power dissipation would be 952mW (Equation 6).
2. With power sharing, the on-chip power dissipation is 412mW (Equation 7). A power redistribution of 540mW.

On-chip power dissipation without power sharing resistor.

$$P_D = (V_{BH})(30mA) + 38.4mW + 13.5mW - (RL)(30mA)^2$$

$$P_D = 952mW \quad \text{(EQ. 6)}$$

On-chip power dissipation with 600Ω power sharing resistor.

$$P_D = (V_{BH})(30mA) + 38.4mW + 13.5mW - (R_L)(30mA)^2 - (R_{PS})(30mA)^2$$

$$P_D = 412mW \quad \text{(EQ. 7)}$$

The design trade-off in using the power sharing resistor is loop length verses on-chip power dissipation.

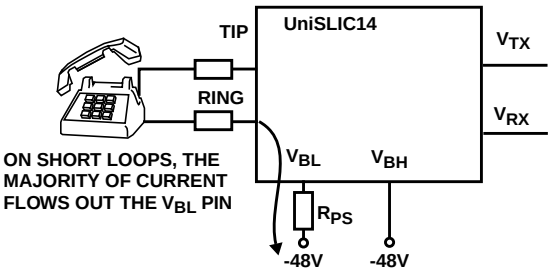

FIGURE 4. POWER SHARING (SINGLE SUPPLY SYSTEMS)

Test #6, Ring Trip Verification

This test will verify the ringing function of the HC5514X. A telephone, a battery referenced AC signal source, and a BNC to banana adaptor are the only additional hardware required to complete the test.

Discussion

The 600Ω termination is not necessary for this test since the phone provides this nominal impedance when offhook. If the RSYNC_REV pin is grounded, the ring relay driver pin (RRLY) pin goes low after the SLIC is placed in the ringing state. This will energize the ring relay. The ring relay disconnects tip and ring from the phone and connects the path for the ringing signal. The D_T and D_R comparator inputs will sense the flow of DC loop current, enabling the ring trip comparator to sense when the phone is either onhook or offhook. When an offhook condition is detected, the HC5514X will automatically disconnect the ringing signal to the phone at zero current crossing. This reduces impulse noise to the system. Refer to the HC5514 Subscriber Line Interface Circuit electrical data sheet for more information about the functionality of the ring trip detector.

Setup

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.

3. Configure the SLIC to be in the Ringing State (C3 = 0, C2 = 0, C1 = 1).
4. Configure S5 and S6 to be in the LED position.
5. Verify that the POL/REV pin S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
6. Connect the telephone across tip and ring.
7. Ground the RSYNC_REV terminal.
8. Connect battery backed AC (20Hz, $90V_{RMS}$ $+V_{BH}$) source to “RINGING” located just below the tip and ring terminals on the board.

Verification

1. Phone starts ringing when power is applied to the test setup; if not, toggle C1.
2. While ringing and Onhook, $\overline{SHD}$ LED is not illuminated.
3. While ringing, going offhook will illuminate the $\overline{SHD}$ LED. When an offhook condition is detected, the HC5514X will automatically disable the RRLY pin (pin goes high) at zero current crossing. This will disable the ring relay and reconnect the tip and ring lines to the phone.
4. When the phone is returned to the Onhook condition, SHD light will remain on until the logic state of the SLIC is changed. This precludes any false on hook detection during the transition between off hook (during ringing) and the off hook active state.

Test #7, Pulse Metering

This test will verify that an offhook $3.1V_{PEAK}$ pulse metering signal and a $1.1V_{PEAK}$ voice signal can be transmitted simultaneously across a complex loop resistance, on tip and ring, with less than 1% Total Harmonic Distortion. The complex loop impedance is equal to 200Ω at the pulse metering frequency of 16kHz, and consist of a series 200Ω resistor and a parallel combination of an 820Ω resistor and a 0.1µF capacitor. Programming of the offhook overhead voltage required for simultaneously operation of both signals is achieved by changing the value of RDC_RAC to 27.4kΩ.

A 27.4kΩ RDC_RAC resistor (provided with kit), two signal generators, the complex load listed above and a dynamic signal analyzer are required to complete this test.

Setup

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Forward Active state (C3 = 0, C2 = 1, C1 = 0).
4. Verify that the POL/REV switch S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Change R1 resistor RDC_RAC to 27.4kΩ.
6. Verify that pin 2 of the PTG jumper (S8, located towards the middle of board near the upper right hand corner of the SLIC) is shorted to pin 1. This condition grounds the PTG pin.
7. Connect a series 200Ω resistor and a parallel combination of an 820Ω resistor and a 0.1µF capacitor across tip and ring terminals.
8. Put a $0.777V_{RMS}$ ($1.1V_{PEAK}$) 1kHz signal into the VRX input.
9. Put a $0.55V_{RMS}$ 16kHz signal into the SPM input. (Equivalent to $3.1V_{PEAK}$ across tip and ring due to gain of 4 from the SPM pin to tip and ring.)
10. Measure the THD across the complex test load.

Verification

1. The THD of the 1kHz signal is less than 1%.

Test #8, Transhybrid Balance

This test will illustrate a method of performing transhybrid balance using the PTG pin. The solution is to use the **P**rogrammable **T**ransmit **G**ain pin (PTG) as an input for the receive signal (V_{RX}). When the PTG pin is connected to a divider network (R14 and R15, Figure 5) and the value of R14 and R15 is much less than the internal 500kΩ resistor RB, two things happen. First, the transmit gain from V_{RX} to V_{TX} is reduced by half. This is the result of shorting out the bottom 500kΩ resistor with the much smaller external resistor. And second, the input signal from V_{RX} is also divided in half by resistors R14 and R15. Transhybrid balance occurs when these two, equal but opposite in phase, signals are cancelled at the input to the output buffer.

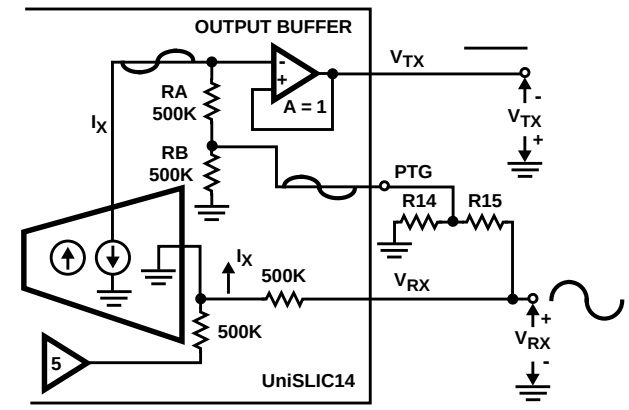

FIGURE 5. TRANSHYBRID BALANCE USING THE PTG PIN

Setup

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
4. Verify that the POL/REV pin S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Terminate tip and ring with a 600Ω load.
6. Verify that pin 2 of the PTG jumper (S8, located towards the middle of board near the upper right hand corner of the SLIC) is short to pin 3. This condition connects resistors R14 and R15 to the PTG pin.

7. Connect a sine wave generator, referenced to ground, to the VRX input.
8. Set the generator for $1V_{RMS}$ at 1kHz.
9. Connect an AC voltmeter, referenced to ground, to the VTX output.

Verification

1. 1. The 4-wire to 4-wire transhybrid balance is about -24dB as calculated in Equation 8.

$$dB_{4W-4W} = 20\log\frac{V_{TX}}{V_{RX}} \quad \text{(EQ. 8)}$$

Test #9, Line Voltage Measurement

Discussion

A few of the SLICs in the UniSLIC14 family feature Line Voltage Measurement (LVM) capability. This feature provides a pulse on the $\overline{GKD}\_\overline{LVM}$ output pin that is proportional to the loop voltage. Knowing the loop voltage and thus the loop length, other basic cable characteristics such as attenuation and capacitance can be inferred. Decisions can be made about gain switching in the CODEC to overcome line losses and verification of the 2-wire circuit integrity.

The LVM function can only be activated in the off hook condition in either the forward or reverse operating states. The LVM uses the ring signal supplied to the SLIC as a time base generator. The loop resistance is determined by monitoring the pulse width of the output signal on the $\overline{GKD}\_\overline{LVM}$ pin. The output signal on the $\overline{GKD}\_\overline{LVM}$ pin is a square wave for which the average duration of the low state is proportional to the average voltage between the tip and ring terminals. The loop resistance is determined by the tip to ring voltage and the constant loop current. Reference Figure 6.

Although the logic state changes to the Test Active State when performing this test, the SLIC is still powered up in the active state (forward or reverse) and the subscriber is unaware the measurement is being taken.

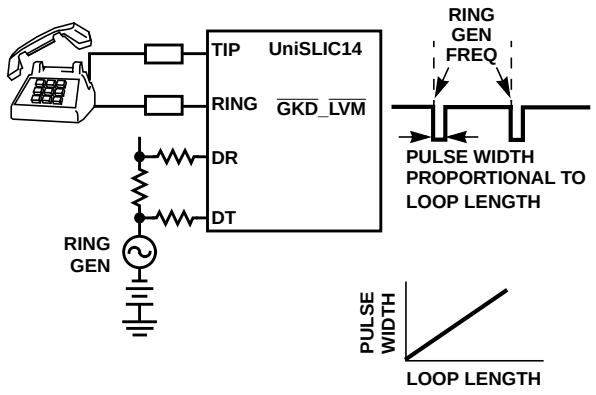

FIGURE 6. OPERATION OF THE LINE VOLTAGE MEASUREMENT CIRCUIT

Setup

1. Connect the power supplies to the Evaluation board.
2. Set V_{BH} to -48V, V_{BL} to -24V and V_{CC} to +5V.
3. Configure the SLIC to be in the Test Active State (C3 = 0, C2 = 1, C1 = 1).
4. Verify that the POL/REV pin S4 (lower right hand side of the board) is in either the 10ms or 20ms position.
5. Terminate tip and ring with a 600Ω load.
6. Connect battery backed AC (20Hz, $90V_{RMS}$ +V_{BH}) source to RING GEN INPUT located just below the tip and ring terminals on the board.
7. Verify that pin 2 of the PTG jumper (S8, located towards the middle of board near the upper right hand corner of the SLIC) is floating.
8. Monitor the output signal on the $\overline{GKD}\_\overline{LVM}$ pin with a scope.

Verification

1. The output signal on the $\overline{GKD}\_\overline{LVM}$ pin is a square wave for which the average duration of the low state is proportional to the average voltage between the tip and ring terminals.
2. Change the load to 1777Ω load and notice the change in the pulse width of the $\overline{GKD}\_\overline{LVM}$ pulse.
3. Notice the same is true for the Test Reversal Active State (C3 = 1, C2 = 1, C1 = 1).

Functional Circuit Component Descriptions

A brief description of each component is provided below. The components will be grouped by function to provide further insight into the operation of the HC5514X board.

TABLE 4. TWO WIRE SIDE, TIP AND RING

RP1, RP2	Protection Resistors used for limiting the current into the transient voltage suppressor in the event of a surge.
U2	Secondary Surge Protection.

TABLE 5. POWER SHARING

R13, S9	R13 (R_{PS}) is used to provide off-chip power dissipation to prevent the SLIC from going into thermal shutdown in short loop high power applications.

TABLE 6. PROGRAMMABLE FEATURES OF THE HC5514X

R1, C7	R1 is used to set the overhead voltage. C7 provides filtering for the DC loop and Anti Clipping circuitry.
C3	CDC Provides filtering of the DC loop.
R4	RD Resistor. Used to set the offhook detect threshold.
R5	ROH Resistor. Used to set the minimum loop current with maximum overhead voltage.

TABLE 6. PROGRAMMABLE FEATURES OF THE HC5514X

R7, R9, R10, S4	RSYNC_REV resistor. Used to set the polarity reversal time with C4 and provide an input for ring Synchronization.
R6	RILIM Resistor. Used to set the current limit.
R14, R15	Used for transhybrid balance of the voice signal.
R2, R3, R11, R12	Used in the detection of ring trip.
R8, R16, C13	Z_T Resistor. Used in the impedances matching of the 2-wire side.
R17, R18, S5, S6	Current Limiting Resistors for $\overline{SHD}$ and $\overline{GKD}\_\overline{LVM}$ LEDs.
S8	Switch 8 is used to program the 2-wire to 4-wire transmission gain and 4-wire to 4-wire transhybrid balance.
C4	CRT_REV_$\overline{LVM}$ Capacitor. Filters ring trip and is used in setting both the polarity reversal time and line voltage measurement.
C2	CH Capacitor. Provides AC and DC separation on the 2-wire side.
S1, S2, S3	Toggle switches to set the logic state of the SLIC.

TABLE 7. SUPPLY DECOUPLING CAPACITORS

C1, C5, C6, C10, C11, C12	Supply decoupling capacitors.

Layout Considerations

Systems with Dual Supplies (V_{BH} and V_{BL})

If the V_{BL} supply is ***not*** derived from the V_{BH} supply, it is recommended that an additional diode be placed in series with the V_{BH} supply. The orientation of this diode is anode on pin 8 of the device and cathode to the external supply.

This external diode will inhibit large currents and potential damage to the SLIC, in the event the V_{BH} supply is shorted to GND. If V_{BL} is derived from V_{BH} then this diode is not required.

Floating the PTG Pin

The PTG pin is a high impedance pin (500kΩ) that is used to program the 2-wire to 4-wire gain to either 0dB or -6dB.

If 0dB is required, it is necessary to float the PTG pin. The PC board interconnect should be as short as possible to minimize stray capacitance on this pin. Stray capacitance on this pin forms a low pass filter and will cause the 2-wire to 4-wire gain to roll off at the higher frequencies.

If a 2-wire to 4-wire gain of -6dB is required, the PTG pin should be grounded as close to the device as possible.

SPM Pin

For optimum performance, the PC board interconnect to the SPM pin should be as short as possible. If pulses metering is not being used, then this pin should be grounded as close to the device pin as possible.

RLIM Pin

The current limiting resistor R_{LIM} needs to be as close to the RLIM pin as possible.

Layout of the 2-Wire Impedance Matching Resistor Z_T

Proper connection to the ZT pin is to have the external Z_T network as close to the device pin as possible.

The ZT pin is a high impedance pin that is used to set the proper feedback for matching the impedance of the 2-wire side. This will eliminate circuit board capacitance on this pin to maintain the 2-wire return loss across frequency.

Demo Board Schematic

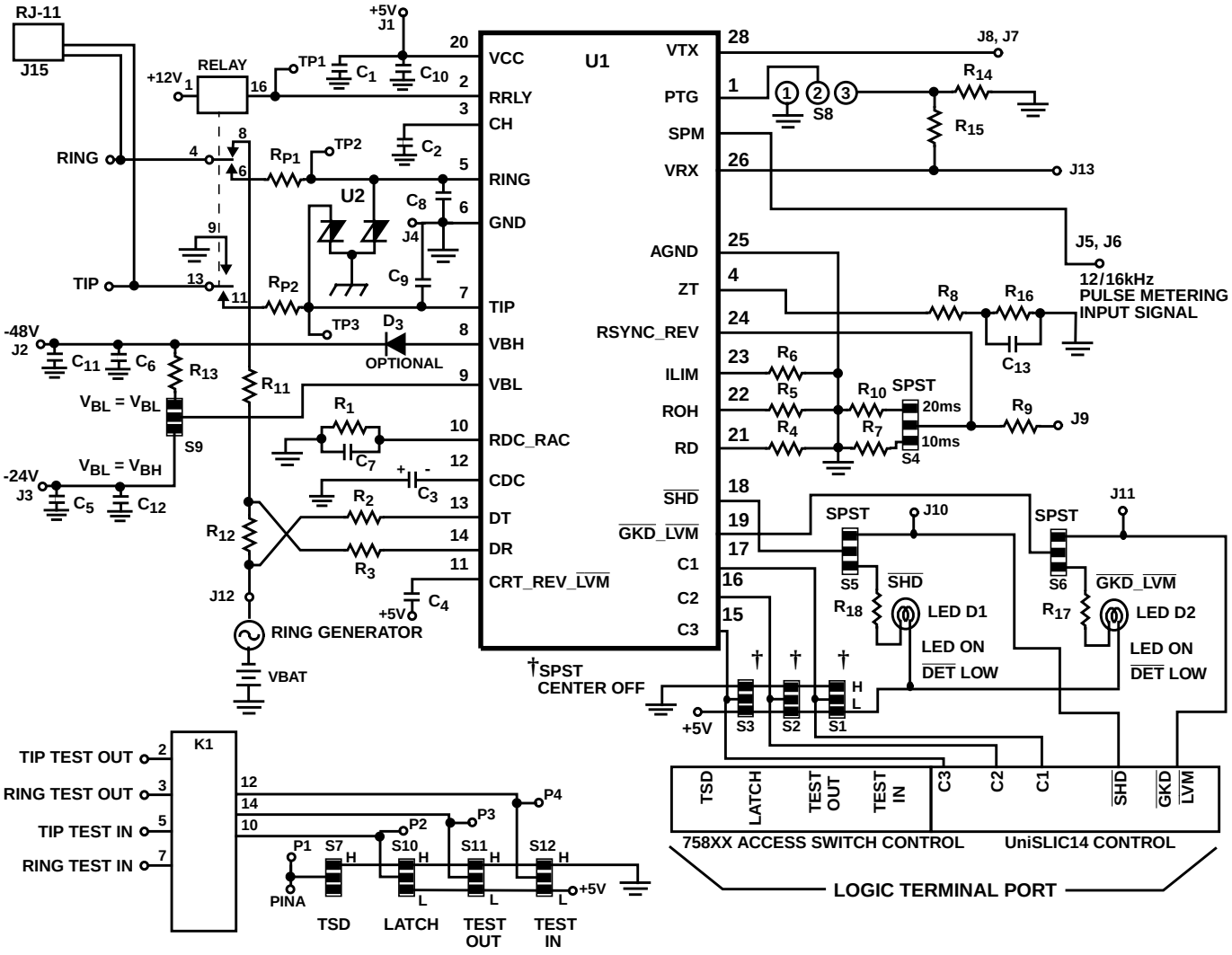

FIGURE 7. UniSLIC14 DEMO BOARD SCHEMATIC

TABLE 8. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	UniSLIC14 Family	N/A	N/A
U2 - Dual Asymmetrical Transient Voltage Suppressor	TISP1082F3	N/A	N/A
RP1, RP2 (Line feed resistors)	30Ω	Matched 1%	2.0W
R1 (RDC_RAC) R = 50*RFEED, RFEED = 381Ω	21.0kΩ	1%	1/16W
R2, R3 (Input Current Limiting Resistors for DT and DR)	2MΩ	1%	1/16W
R4 (RD resistor) R = 500/I_{SH}, I_{SH} = 9.78mA	41.2kΩ	1%	1/16W
R5 (ROH resistor) R = 500/Iloop(min)-I_{SH}- (Iloop(min) = 20mA, I_{SH}- 6.54mA)	38.3kΩ	1%	1/16W
R6 (R_{ILIM} resistor) R = 1000/ILIM (ILIM = 30mA)	33.2kΩ	1%	1/16W

TABLE 8. BASIC APPLICATION CIRCUIT COMPONENT LIST (Continued)

COMPONENT	VALUE	TOLERANCE	RATING
R7 (RSYNC_REV resistors) R = 3.47k/µs (10µs)	34.8kΩ	1%	1/16W
R8 (RZT, 2-Wire Impedance Matching Resistor) R = 200(ZO-2RF) Z0 = 600Ω, RF = 30Ω	107kΩ	1%	1/4W
R9 (Current Limit Resistor for Ring Sync Pulse)	49.9kΩ	1%	1/16 W
R10 (RSYNC_REV resistor) R = 3.47k/µs (2µs)	69.8kΩ	1%	1/16 W
R11 (Series Resistor to simulate loop length during ringing)	600Ω	1%	2W
R12 (Sense Resistor for DC current during ringing)	400Ω	1%	2W
R13 (R_{PS}, Power Sharing Resistor)	Open	-	-
R14, R15 (Transhybrid Resistors)	10kΩ	1%	1/16W
R16, C13 (For matching a complex 2-Wire impedance)	R = 0Ω C13 = Open	-	-
R17, R18 (Current Limiting Resistors for LEDs)	510	5%	1/4W
C1, C5	0.01µF	20%	50V
C2	0.1µF	20%	10V
C3	4.7µF	10%	50V or (V_{BH}/2)
C4, C7	0.47µF	20%	10V
C6	0.01µF	20%	100V
C8, C9	2200pF	20%	100V
C10, C12	0.1µF	20%	50V
C11	0.1µF	20%	100V
D1, D2 ($\overline{SHD}$ and $\overline{GKD}$_$\overline{LVM}$ LEDs)	Red	-	-
D3, Recommended if the V_{BL} supply is not derived from the V_{BH} supply.	1N4004	-	-

Design Parameters: Switch Hook Threshold = 12mA, Loop Current Limit = 30mA, Synthesize Device Impedance = 600-60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.

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