

Description

The ICS348 field programmable clock synthesizer generates up to 9 high-quality, high-frequency clock outputs including multiple reference clocks from a low frequency crystal or clock input. The ICS348 has 4 independent on-chip PLLs and is designed to replace crystals and crystal oscillators in most electronic systems.

Using IDT's VersaClock™ software to configure PLLs and outputs, the ICS348 contains a One-Time Programmable (OTP) ROM to allow field programmability. Programming features include eight selectable configuration registers, up to two sets of four low-skew outputs.

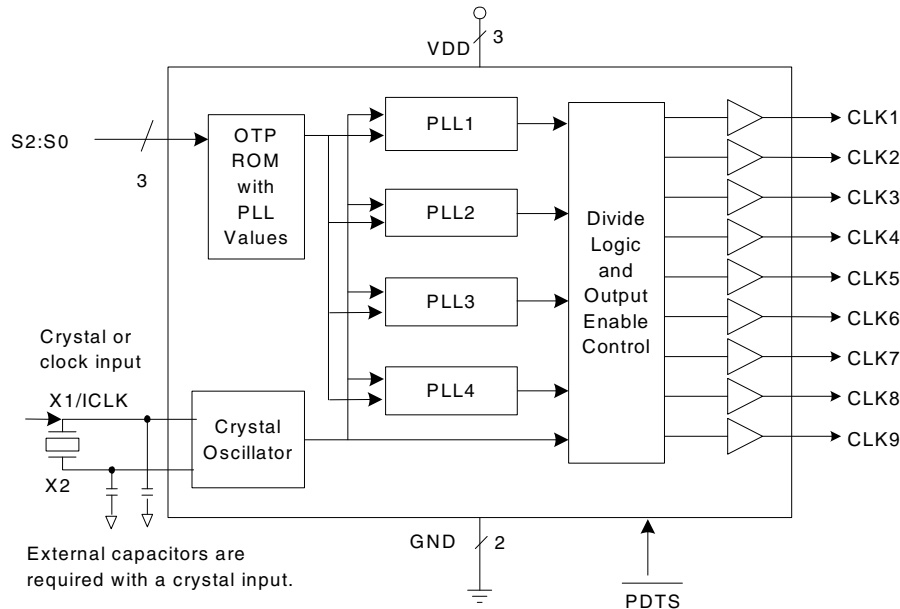
Using Phase-Locked Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

The ICS348 is also available in factory programmed custom versions for high-volume applications.

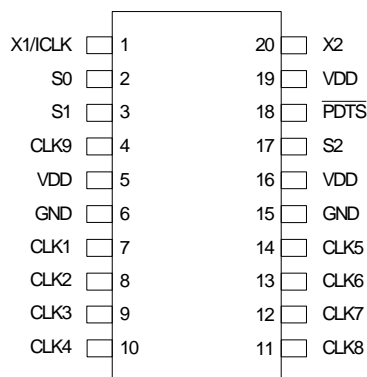
Features

- Packaged as 20-pin SSOP (QSOP) (Pb-free)
- Eight addressable registers
- Replaces multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3V
- Input crystal frequency of 5 to 27 MHz
- Input clock frequency of 2 to 50 MHz
- Up to nine reference outputs
- Up to two sets of four low-skew outputs
- Operating voltages of 3.3 V
- Advanced, low power CMOS process
- For one output clock, use the ICS341 (8-pin). For two output clocks, use the ICS342 (8-pin). For three output clocks, use the ICS343 (8-pin). For more than three outputs, use the ICS345 or ICS348.

Block Diagram



Pin Assignment



20-pin (150 mil) SSOP (QSOP)

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|---------------------------------|----------|---|
| 1 | X1 | XI | Crystal Input. Connect this pin to a crystal or external input clock. |
| 2 | S0 | Input | Select pin 0. Internal pull-up resistor. |
| 3 | S1 | Input | Select pin 1. Internal pull-up resistor. |
| 4 | CLK9 | Output | Output clock 9. Weak internal pull-down when tri-state. |
| 5 | VDD | Power | Connect to +3.3 V. |
| 6 | GND | Power | Connect to ground. |
| 7 | CLK1 | Output | Output clock 1. Weak internal pull-down when tri-state. |
| 8 | CLK2 | Output | Output clock 2. Weak internal pull-down when tri-state. |
| 9 | CLK3 | Output | Output clock 3. Weak internal pull-down when tri-state. |
| 10 | CLK4 | Output | Output clock 4. Weak internal pull-down when tri-state. |
| 11 | CLK8 | Output | Output clock 8. Weak internal pull-down when tri-state. |
| 12 | CLK7 | Output | Output clock 7. Weak internal pull-down when tri-state. |
| 13 | CLK6 | Output | Output clock 6. Weak internal pull-down when tri-state. |
| 14 | CLK5 | Output | Output clock 5. Weak internal pull-down when tri-state. |
| 15 | GND | Power | Connect to ground. |
| 16 | VDD | Power | Connect to +3.3 V. |
| 17 | S2 | Input | Select pin 2. Internal pull-up resistor. |
| 18 | $\overline{\text{PDT\text{S}}}$ | Input | Power down tri-state. Powers down entire chip and tri-states clock outputs when low. Internal pull-up resistor. |
| 19 | VDD | Power | Connect to +3.3 V. |
| 20 | X2 | XO | Crystal Output. Connect this pin to a fundamental crystal. Float for clock input. |

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS348 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01μF must be connected between each VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 6 \text{ pF})^2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF $[(16-6) \times 2] = 20$.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.
- 2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.
- 3) To minimize EMI, the 33Ω series termination resistor, if needed, should be placed close to the clock output.
- 4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers.

ICS348 Configuration Capabilities

The architecture of the ICS348 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 2048 and N = 1 to 1024.

The ICS348 also provides separate output divide values, from 2 through 20, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

$$\text{OutputFreq} = \frac{\text{REFFreq}}{\text{OutputDivide}} \cdot \frac{M}{N}$$

IDT VersaClock Software

IDT applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

Using VersaClock Products with an Input Clock Source

In order to ensure proper startup with an input clock rather than a crystal, the supply voltage must be within the operating range (3.3V ±10%) and the input signal must be stable and free from glitching. The input clock must provide pulses of at least 20ns, and no more than 500ns, for at least 160 clock cycles without any interruptions to the clock or power during this period. It may take up to 4ms for output frequencies to reach their target frequency values.

An alternative method is to have the $\overline{\text{PDT\text{S}}}$ pin asserted low while power supplies and clock sources stabilize. Once the power supply and input clock source are constant and within the acceptable frequency range, bring $\overline{\text{PDT\text{S}}}$ high. This approach is preferred if the clock source is derived from another PLL, or the source oscillator produces unpredictable output pulses prior to stabilization. No considerations need to be taken when using a crystal input source with VersaClock products.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS348. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Parameter | Condition | Min. | Typ. | Max. | Units |
|-----------------------|-------------------|------|------|---------|-------|
| Supply Voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Clock Outputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Storage Temperature | | -65 | | 150 | °C |
| Soldering Temperature | Max 10 seconds | | | 260 | °C |
| Junction Temperature | | | | 125 | °C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature (ICS348RP) | 0 | | +70 | °C |
| Ambient Operating Temperature (ICS348RIP) | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V |
| Power Supply Ramp Time | | | 4 | ms |

DC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, Ambient Temperature -40 to $+85^{\circ}\text{C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------|--|--------------|----------|--------------|------------------|
| Operating Voltage | V_{DD} | | 3.15 | | 3.45 | V |
| Operating Supply Current Input High Voltage | I_{DD} | Configuration Dependent - See VersaClock™ Estimates | | | | mA |
| | | Nine 33.3333 MHz outs, $\overline{PDTS} = 1$, no load, Note 1 | | 23 | | mA |
| | | $\overline{PDTS} = 0$, no load | | 20 | | μA |
| Input High Voltage | V_{IH} | S2:S0 | 2 | | | V |
| Input Low Voltage | V_{IL} | S2:S0 | | | 0.4 | V |
| Input High Voltage, \overline{PDTS} | V_{IH} | | $V_{DD}-0.5$ | | | V |
| Input Low Voltage, \overline{PDTS} | V_{IL} | | | | 0.4 | V |
| Input High Voltage | V_{IH} | ICLK | $V_{DD}/2+1$ | | | V |
| Input Low Voltage | V_{IL} | ICLK | | | $V_{DD}/2-1$ | V |
| Output High Voltage (CMOS High) | V_{OH} | $I_{OH} = -4\text{ mA}$ | $V_{DD}-0.4$ | | | V |
| Output High Voltage | V_{OH} | $I_{OH} = -12\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 12\text{ mA}$ | | | 0.4 | V |
| Short Circuit Current | I_{OS} | | | ± 70 | | mA |
| Nominal Output Impedance | Z_O | | | 20 | | Ω |
| Internal pull-up resistor | R_{PUS} | S2:S0, \overline{PDTS} | | 250 | | $\text{k}\Omega$ |
| Internal pull-down resistor | R_{PD} | CLK outputs | | 525 | | $\text{k}\Omega$ |
| Input Capacitance | C_{IN} | Inputs | | 4 | | pF |

Note 1: Example with 25 MHz crystal input with nine outputs of $33.\overline{3}$ MHz, no load, and $V_{DD} = 3.3\text{ V}$.

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|----------------------------------|-----------------|--|------|-------|------|-------|
| Input Frequency | F _{IN} | Fundamental Crystal | 5 | | 27 | MHz |
| | | Input Clock | 2 | | 50 | MHz |
| Output Frequency | | VDD=3.3 V | 0.25 | | 200 | MHz |
| Output Rise Time | t _{OR} | 20% to 80%, Note 1 | | 1 | | ns |
| Output Fall Time | t _{OF} | 80% to 20%, Note 1 | | 1 | | ns |
| Duty Cycle | | Note 2 | 40 | 49-51 | 60 | % |
| Output Frequency Synthesis Error | | Configuration Dependent | TBD | | | ppm |
| Power-up time | | PLL lock-time from power-up, Note 3 | | 3 | 10 | ms |
| | | $\overline{\text{PDT\!S}}$ goes high until stable CLK output, Note 3 | | 0.2 | 2 | ms |
| One Sigma Clock Period Jitter | | Configuration Dependent | | 50 | | ps |
| Maximum Absolute Jitter | t _{ja} | Deviation from Mean. Configuration Dependent | | ±200 | | ps |
| Pin-to-Pin Skew | | Low Skew Outputs | -250 | | 250 | ps |

Note 1: Measured with 15 pF load.

Note 2: Duty Cycle is configuration dependent. Most configurations are minimum 45% and maximum 55%.

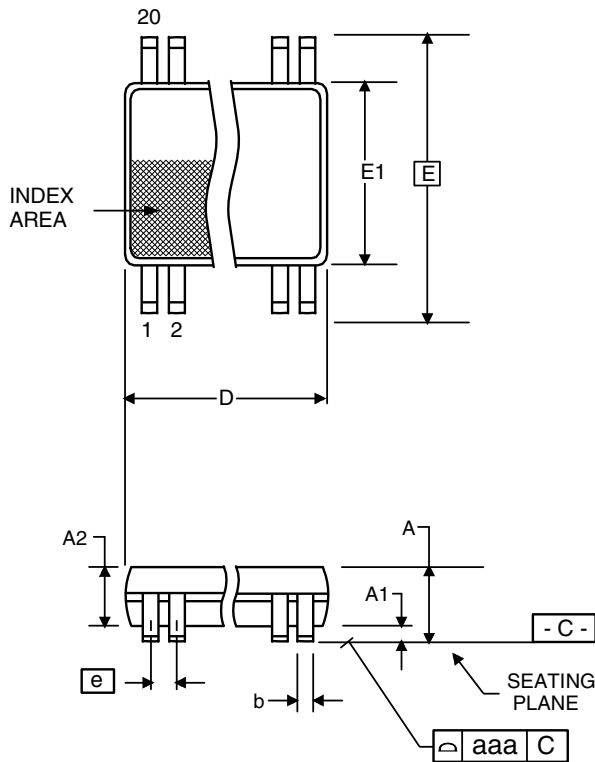
Note 3: IDT test mode output occurs for first 170 clock cycles on CLK7 for each PLL powered up. $\overline{\text{PDT\!S}}$ transition high on select address change.

Thermal Characteristics

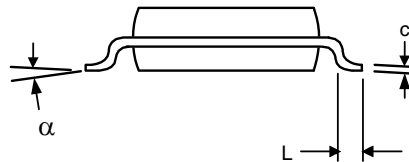
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 135 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 93 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 78 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 60 | | °C/W |

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches | |
|----------|-------------|------|------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | -- | 1.50 | -- | 0.059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | .635 Basic | | .025 Basic | |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|-------------|---------------|
| 348RPLF | ICS348RPLF | Tubes | 20-pin SSOP | 0 to +70° C |
| 348RPLFT | ICS348RPLF | Tape and Reel | 20-pin SSOP | 0 to +70° C |
| 348RIPLF | ICS348RIPLF | Tubes | 20-pin SSOP | -40 to +85° C |
| 348RIPLFT | ICS348RIPLF | Tape and Reel | 20-pin SSOP | -40 to +85° C |
| 348R-XXLF | 348R-XXLF | Tubes | 20-pin SSOP | 0 to +70° C |
| 348R-XXLFT | 348R-XXLF | Tape and Reel | 20-pin SSOP | 0 to +70° C |
| 348RI-XXLF | 348RI-XXLF | Tubes | 20-pin SSOP | -40 to +85° C |
| 348RI-XXLFT | 348RI-XXLF | Tape and Reel | 20-pin SSOP | -40 to +85° C |

“LF” suffix to the part number denotes Pb-Free configuration, RoHS compliant.

The 348R-XXLF and 348RI-XXLF are factory programmed versions of the 348RPLF and 348RIPLF. A unique “-XX” suffix is assigned by the factory for each custom configuration, and a separate data sheet is kept on file. For more information on custom part numbers programmed at the factory, please contact your local IDT sales and marketing representative.

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|---|
| N | 09/06/13 | S. Zheng | Added brief applications section/verbiage "Using VersaClock Products with an Input Clock Source" on page 3. |
| | | | |

ICS348

QUAD PLL FIELD PROGRAMMABLE VERSACLOCK SYNTHESIZER

EPROM CLOCK SYNTHESIZER

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