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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD151012

8-bit Binary Programmable Counter with Synchronous Preset Enable

REJ03D0299–0200Z
(Previous ADE-205-132 (Z))
Preliminary
Rev.2.00
Jul.16.2004

Description

The HD151012 has 8-bit binary down counter and D-type Flip Flop. The counter can set up to max 256 counts and synchronous preset ($\overline{SPE}$) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rise edge. It is applied to generate AC signal for STN type liquid crystal and general-use divider.

Features

- High speed operation
  tpd (CLK or $\overline{CLK}$ to Q) = 35 ns (typ)
- High output current
  Fanout of 10 LS TTL Loads
- Wide operating voltage
  V_{CC} = 2 to 6 V
- Low supply current (Ta = 25°C)
  I_{CC} (Static) = 4 µA (max)

- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD151012TELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

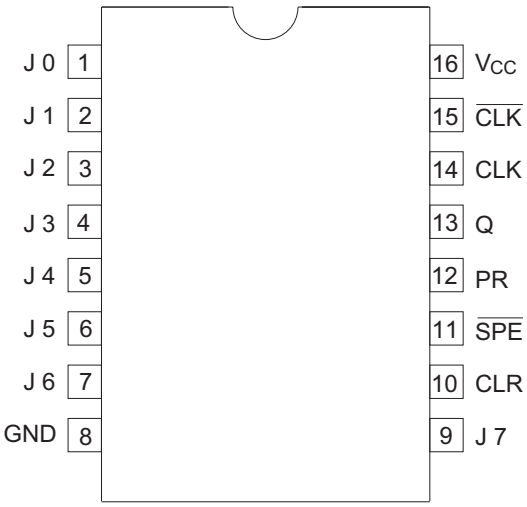
Function Table

Control Inputs			Mode	Operation Description
CLR	PR	$\overline{SPE}$		
H	H	H	Generally count	Down count at the rise edge of clock (CLK) Down count at the fall edge of clock (CLK)
X	X	L	Synchronous preset	Jn data is preset at the rise of clock (CLK), the fall of clock (CLK)
L	H	—	Initialize of Q output	Initialize of Q = “L”
H	L	—	Initialize of Q output	Initialize of Q = “H”

Notes: 1. Synchronous preset ($\overline{SPE}$) input can set max 256 down counts.
2. When the count value is 0, the next clock pulse presets the data to invert the output.
3. CLR and PR inputs initialize output state.

H : High level
L : Low level
X : Immaterial
— : Irrespective of condition

Pin Arrangement



(Top view)

Pin Description

Pin Name		Pin Description	
Input pins	J0 to J7	Count data input for option	
	CLK, $\overline{CLK}$	Clock inputs	CLK : Rise edge trigger $\overline{CLK}$: Fall edge trigger
	$\overline{SPE}$	Preset input for Jn data	
	PR	Preset input for D-type Flip Flop (Initialize “L” at Q output)	
	CLR	Clear input for D-type Flip Flop (Initialize “H” at Q output)	
Output pins	Q	Output for D-type Flip Flop	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.5 to 7.0	V
Input / output voltage	V_{IN}/V_{OUT}	–0.5 to V_{CC} +0.5	V
VCC, GND current	I_{CC}, IGND	±50	mA
Output current / pin	I_{OUT}	±25	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to 150	°C
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA

Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

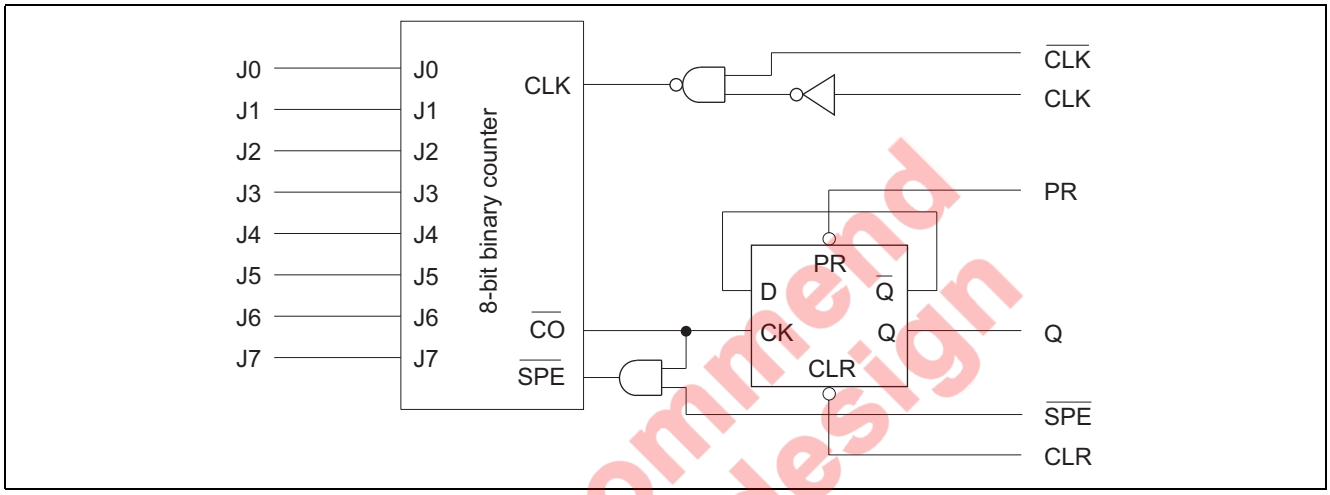
2. All voltage values except for differential input voltage are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	2	—	6	V
Input/output voltage		$V_{IN}/_{OUT}$	0	—	V_{CC}	V
Operating temperature		Topr	–40	—	+85	°C
Input rise/fall time*[1]	V_{CC} = 2.5 V	t_r, t_f	0	—	1000	ns
	V_{CC} = 4.5 V		0	—	500	
	V_{CC} = 5.5 V		0	—	400	

Note: 1. This item guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics

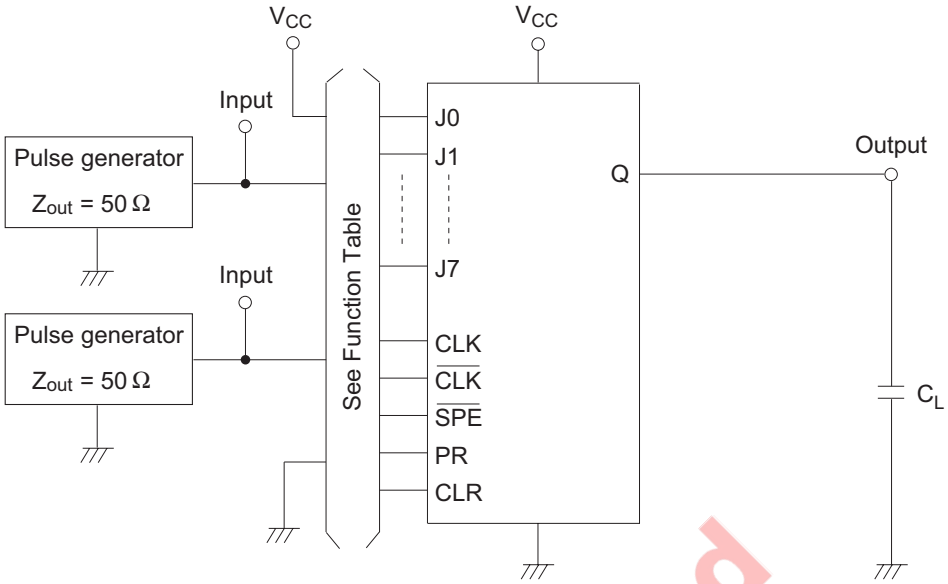
Item	Symbol	V_{CC}	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
High level input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	J0 to J7	
		4.5	3.15	—	—	3.15	—		$\overline{SPE}$	
		6.0	4.2	—	—	4.2	—		PR, CLR	
		2.0	1.5	—	—	1.5	—		$\overline{CLK}$, CLK	
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
Low level input voltage	V_{IL}	2.0	—	—	0.5	—	0.5	V	J0 to J7	
		4.5	—	—	1.35	—	1.35		$\overline{SPE}$	
		6.0	—	—	1.8	—	1.8		PR, CLR	
		2.0	—	—	0.5	—	0.5		$\overline{CLK}$, CLK	
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
High level output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –20 mA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	4.31	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	5.80	—	5.63	—			I_{OH} = –5.2 mA
Low level output voltage	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	0.17	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	0.18	0.26	—	0.33			I_{OL} = 5.2 mA
Input capacitance	I_{IN}	6.0	—	—	±0.1	—	±1.0	mA	V_{IN} = V_{CC} or GND	
Supply current	I_{CC}	6.0	—	—	4.0	—	40.0	mA	V_{IN} = V_{CC} or GND	

Switching Characteristics (C_L = 50 pF, t_r = t_f = 6 ns)

Item	Symbol	V_{CC}	Ta = 25°C Min	Ta = 25°C Typ	Ta = 25°C Max	Ta = –40 to 85°C Min	Ta = –40 to 85°C Max	Unit	Test Conditions
Maximum clock frequency	f_{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	36	20	—	16		
		6.0	—	—	24	—	19		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	30	75	—	95	ns	
		4.5	—	8	15	—	19		
		6.0	—	7	13	—	16		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	300	—	380		CLK or $\overline{CLK}$ to Q
		4.5	—	35	60	—	75		
		6.0	—	—	53	—	65		
	t_{PLH} t_{PHL}	2.0	—	—	150	—	185		PR or CLR to Q
		4.5	—	18	30	—	38		
		6.0	—	—	25	—	32		
Pulse width (CLK, $\overline{CLK}$, PR, CLR)	tw	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time (Jn - CLK, $\overline{CLK}$) ($\overline{SPE}$, CLK, $\overline{CLK}$)	ts	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time (Jn - CLK, $\overline{CLK}$) ($\overline{SPE}$, CLK, $\overline{CLK}$)	th	2.0	15	—	—	15	—	ns	
		4.5	10	—	—	10	—		
		6.0	5	—	—	5	—		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance*[1]	C_{PD}	—	—	48	—	—	—	pF	

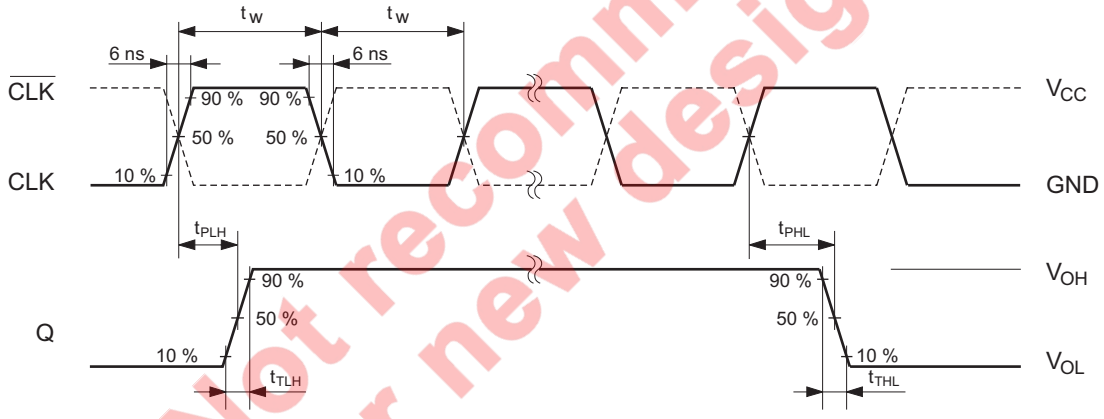
Note: 1. CPD is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.
I_{CC} (opr) = C_{PD} • V_{CC} • f_{IN} + I_{CC}

Test Circuit

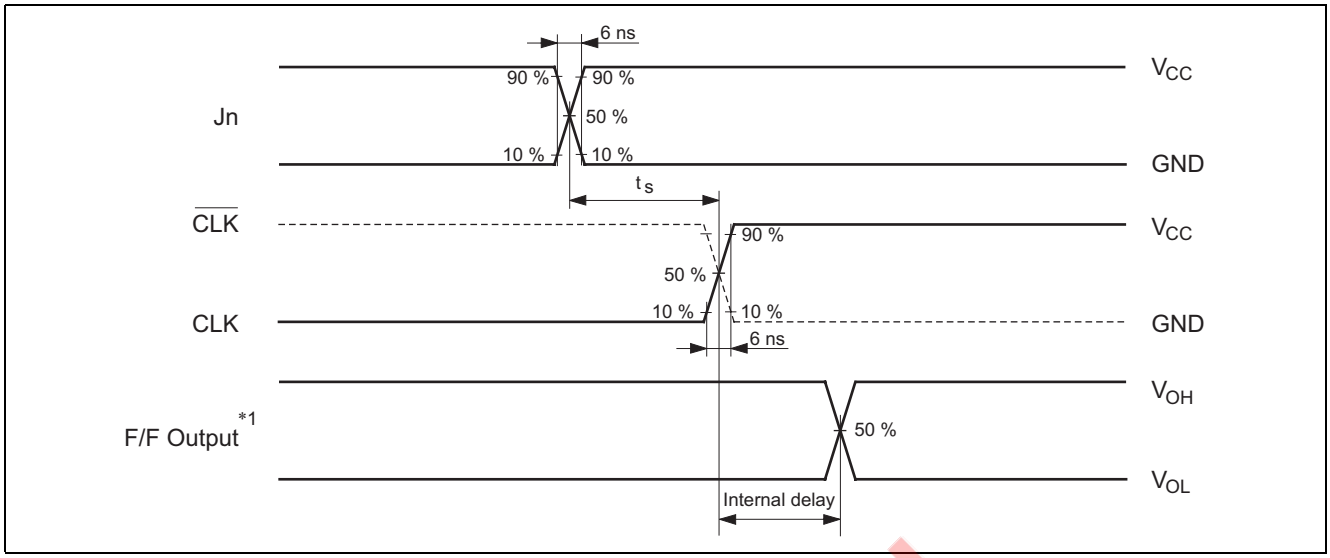


Note: 1. C_L includes probe and jig capacitance.

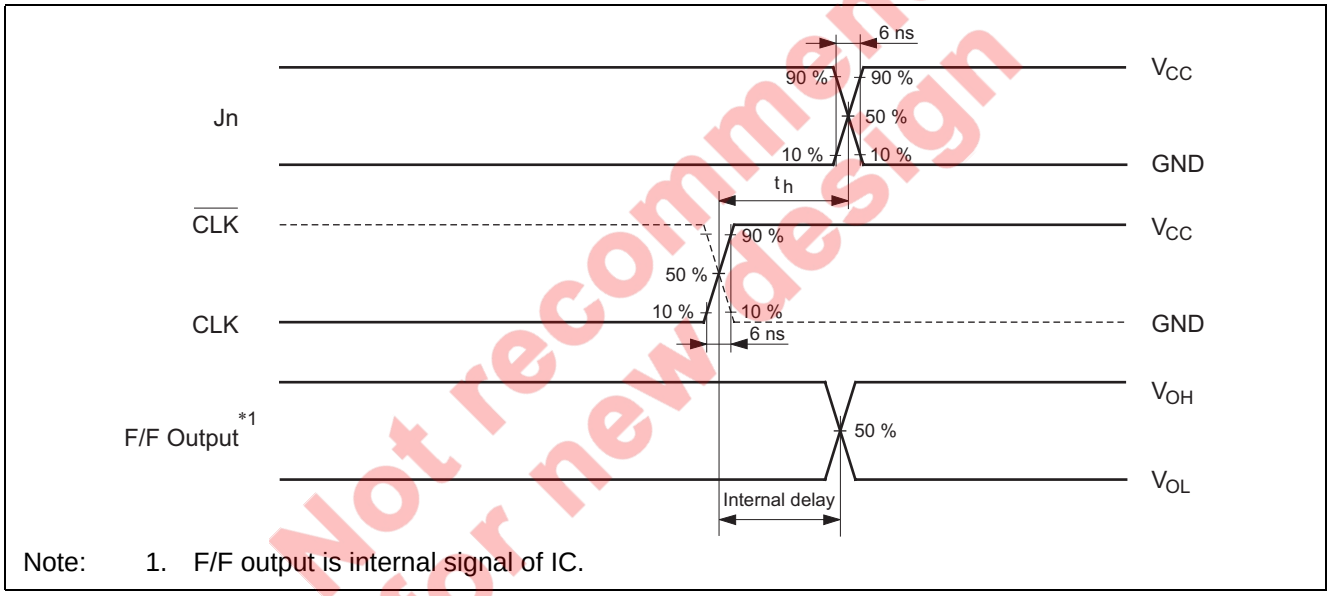
Waveforms – 1



Waveforms – 2

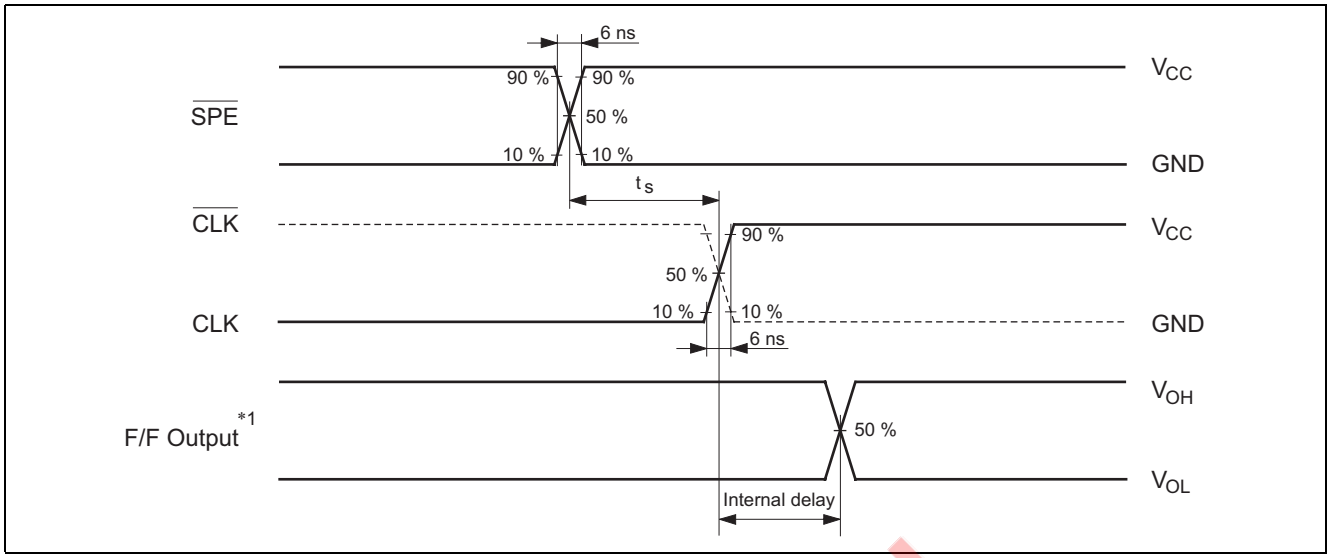


Waveforms – 3

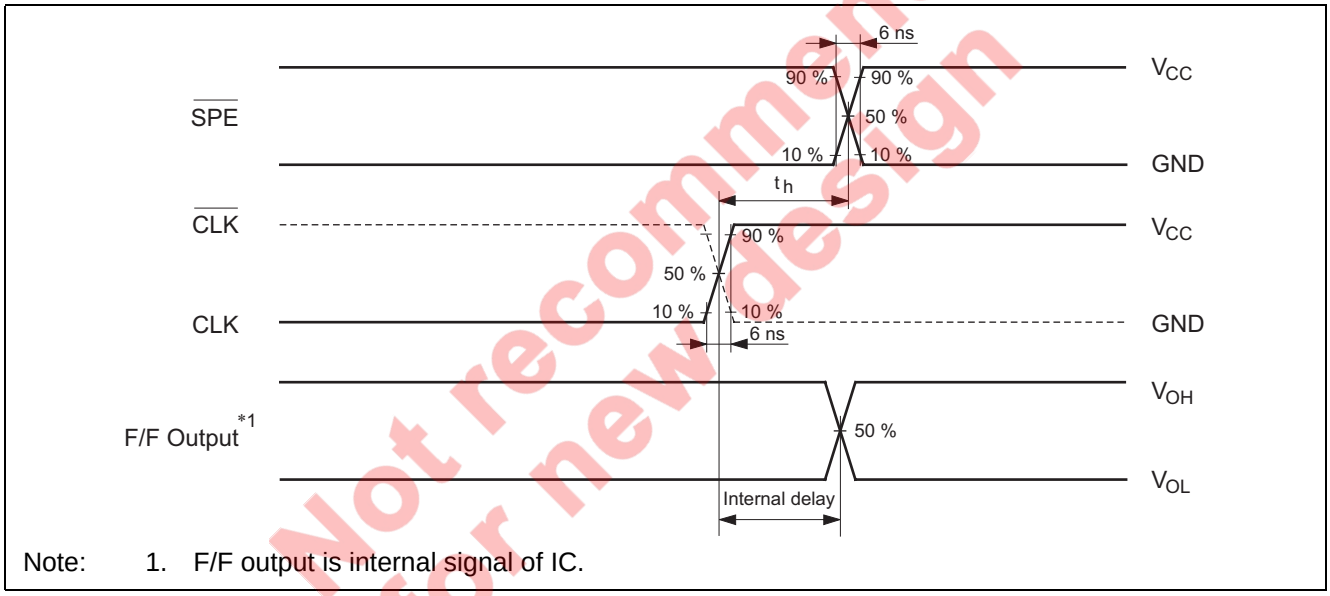


Note: 1. F/F output is internal signal of IC.

Waveforms – 4

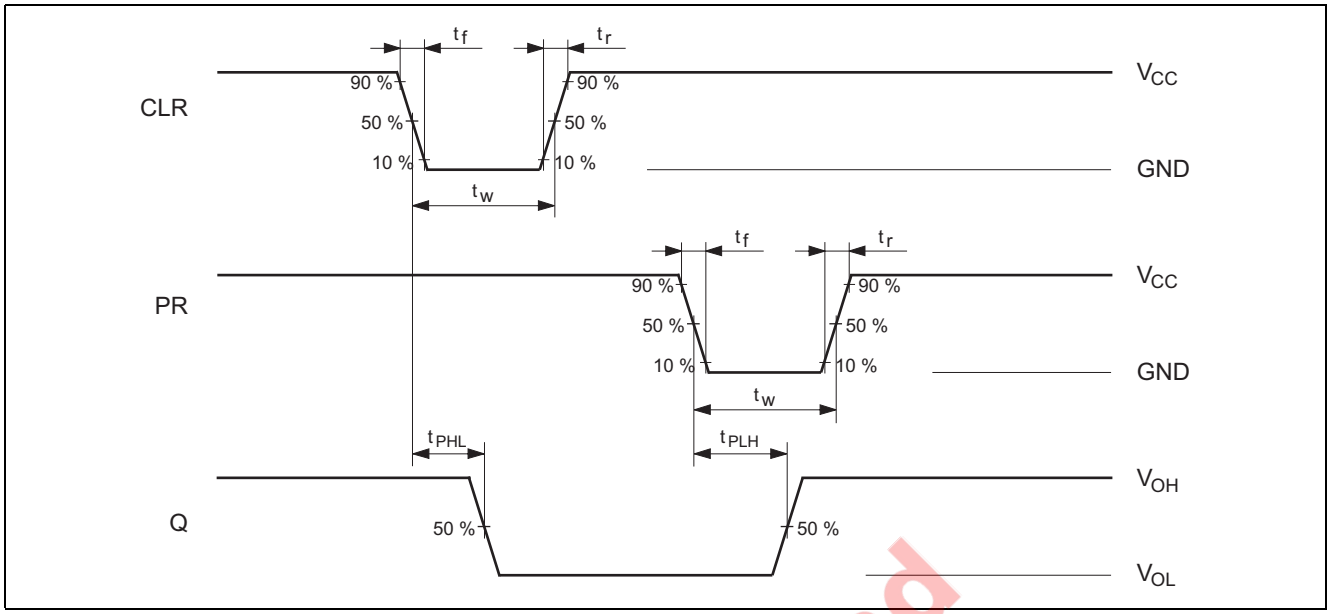


Waveforms – 5

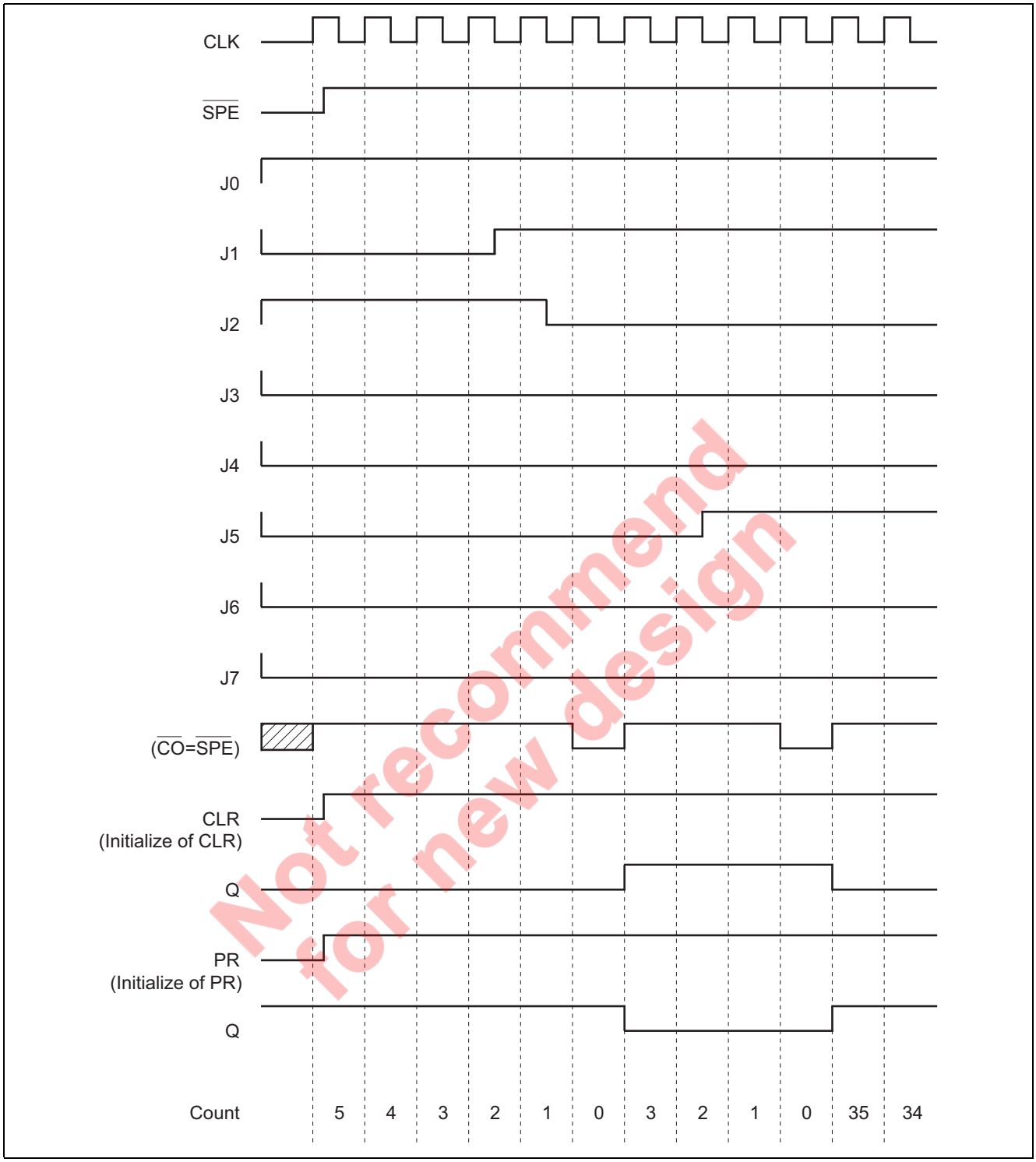


Note: 1. F/F output is internal signal of IC.

Waveforms – 6



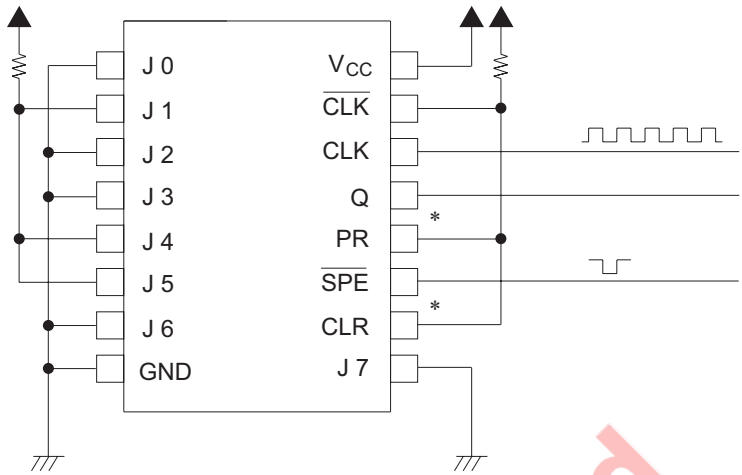
Timing Chart



Example of Application Circuit

AC Signal Generator for STN Type Liquid Crystal Panel

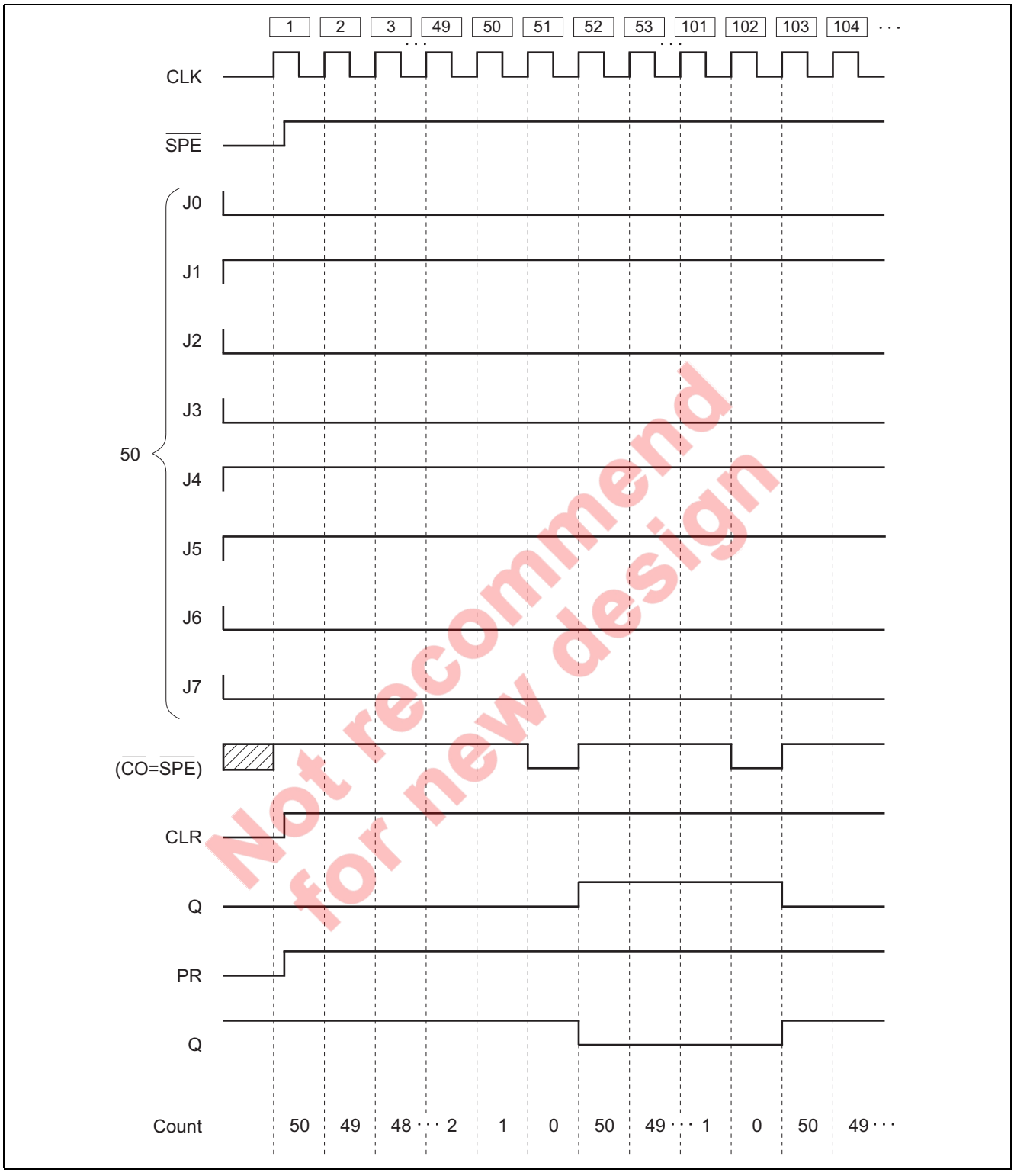
Initialize counter: 50



Note: When initializing output D-F/F apply “L”

Timing Chart

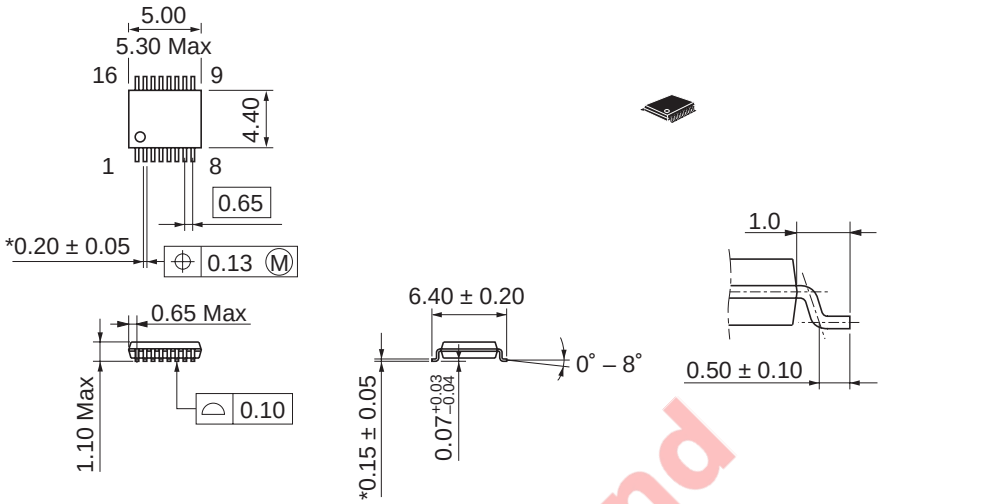
Example of AC Signal Generator



Package Dimensions

As of January, 2003

Unit: mm



Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

*Ni/Pd/Au plating

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