To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS93

4-bit Binary Counter

REJ03D0423–0200
Rev.2.00
Feb.18.2005

The HD74LS93 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-state binary counter for divide-by-eight. To use this maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

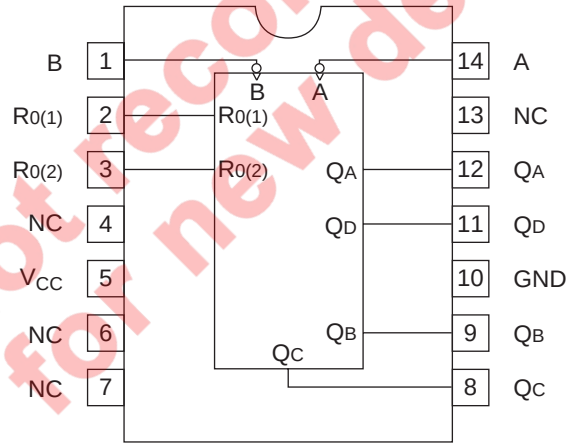
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS93P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS93FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Function Table

• Reset / Count Function Table

Reset inputs		Outputs			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

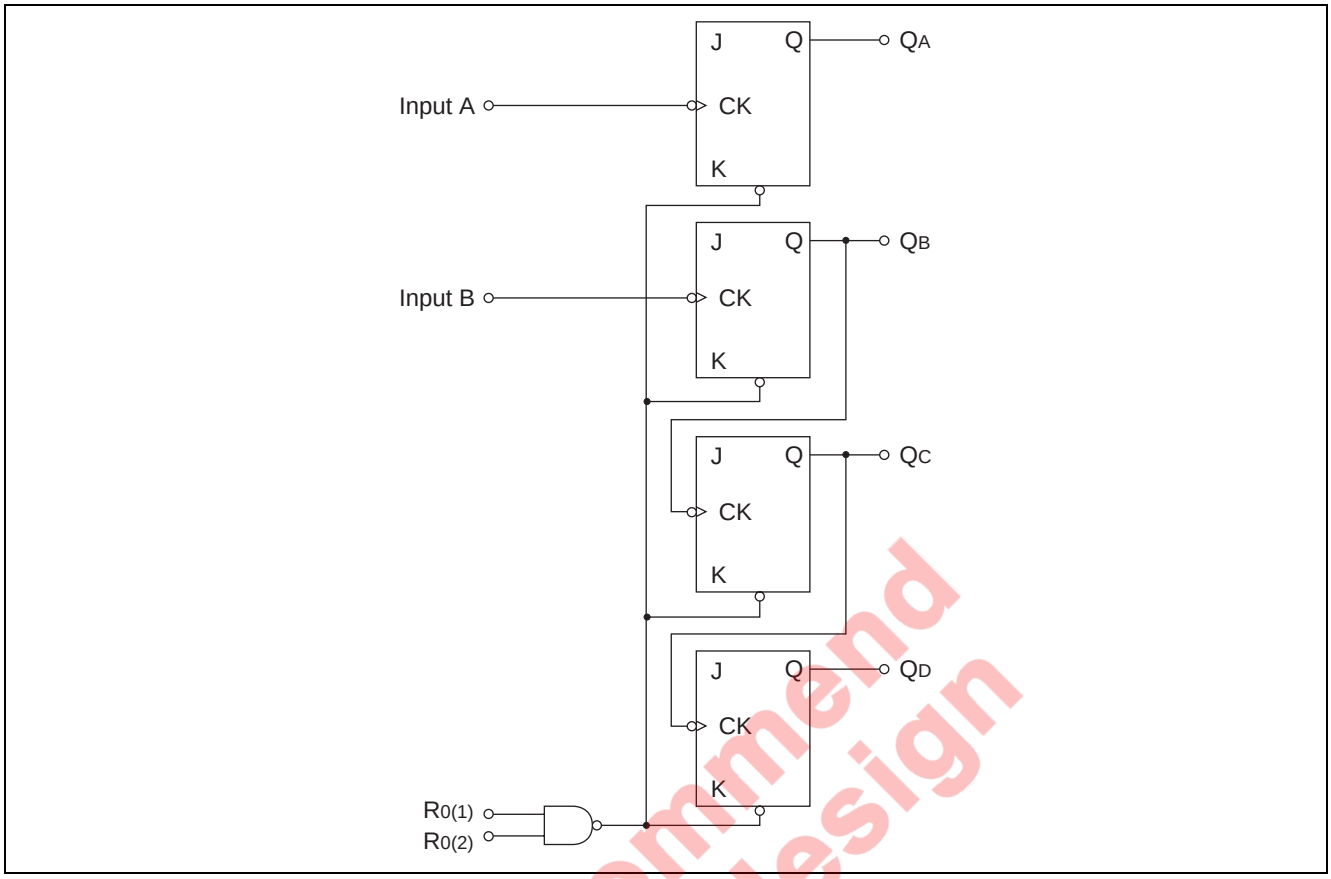
Note: H; high level, L; low level, X; irrelevant

• BCD Count Sequence (Notes 1)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	H
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes: 1. Output QA is connected to input B for BCD count.
2. H; high level, L; low level

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7	V
Input voltage	R Inputs	V_{IN}	7	V
	A, B Inputs	V_{IN}	5.5	V
Power dissipation		P_T	400	mW
Storage temperature		Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Count frequency	A input	f_{count}	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	t_w	15	—	—	ns
	B input		30	—	—	
	Reset input		15	—	—	
Setup time		t_{su}	25	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V_{IH}	2.0	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA	
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA**	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5		I_{OL} = 8 mA**	
Input current	Any reset	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	A input		—	—	–2.4			
	B input		—	—	–1.6			
	Any reset	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	A input		—	—	40			
	B input		—	—	40			
	Any reset	I_I	—	—	0.1	mA	V_I = 7 V	V_{CC} = 5.25 V
	A input		—	—	0.2		V_I = 5.5 V	
	B input		—	—	0.2		V_I = 5.5 V	
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V	
Supply current		I_{CC}***	—	9	15	mA	V_{CC} = 5.25 V	
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Notes: * V_{CC} = 5 V, Ta = 25°C

** Q_A output is tested at specified I_{OL} plus the limit value of IIL for the B input. This permits driving the B input while maintaining full fan-out capability.

*** I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

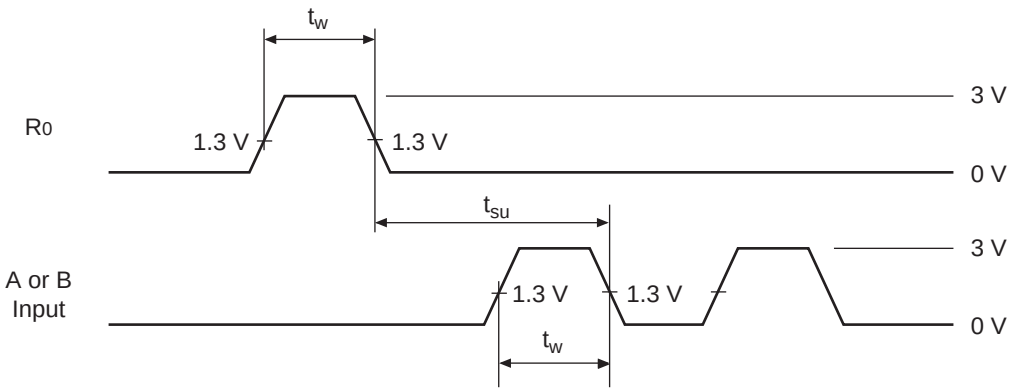
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	f_{max}	A	Q_A	32	42	—	MHz	C_L = 15 pF, R_L = 2 kΩ
		B	Q_B	16	—	—		
Propagation delay time	t_{PLH}	A	Q_A	—	10	16	ns	
	t_{PHL}			—	12	18		
	t_{PLH}	A	Q_D	—	46	70		
	t_{PHL}			—	46	70		
	t_{PLH}	B	Q_B	—	10	16		
	t_{PHL}			—	14	21		
	t_{PLH}	B	Q_C	—	21	32		
	t_{PHL}			—	23	35		
	t_{PLH}	B	Q_D	—	34	51		
	t_{PHL}			—	34	51		
	t_{PHL}	Set-to-0	Q_A to Q_D	—	26	40		

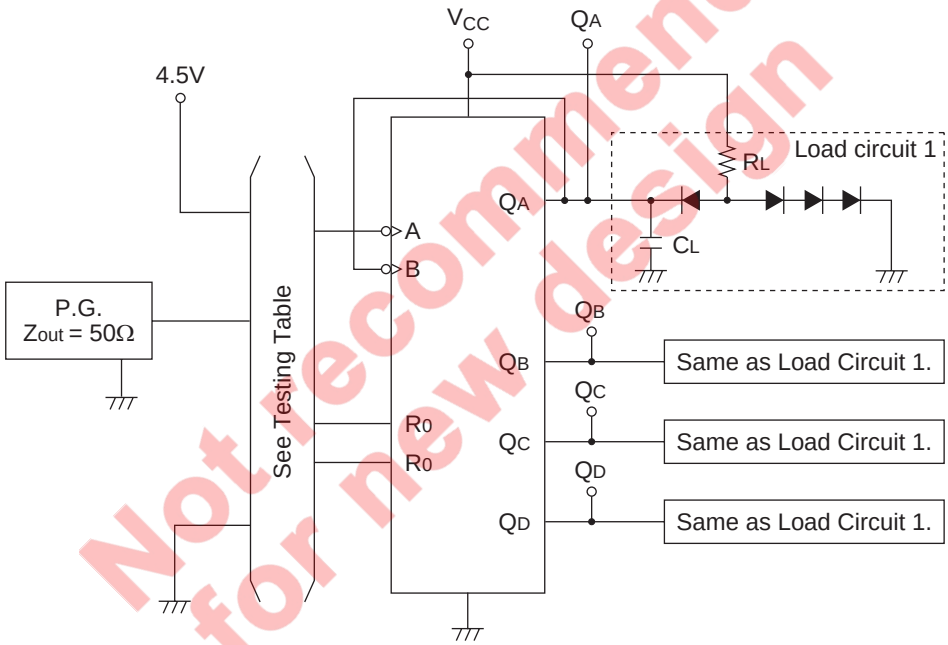
Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

Timing Definition



Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Testing Table

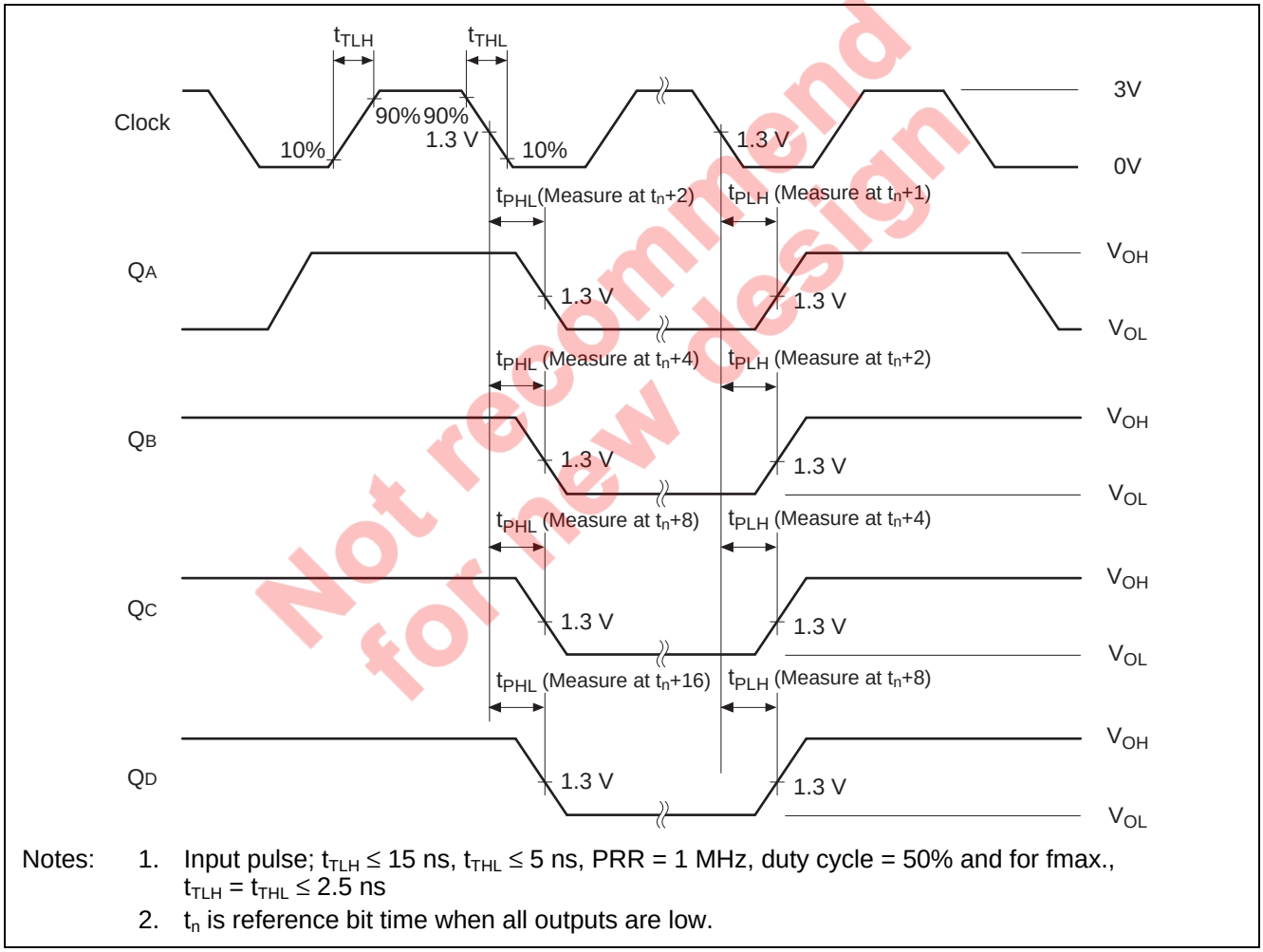
Item	From input to output	Inputs			Outputs			
		A	B	R_0	Q_A	Q_B	Q_C	Q_D
f_{max}	A → Q	IN	to Q_A	GND	Out	Out	Out	Out
	B → Q	4.5 V	IN	GND	—	Out	Out	Out
t_{PLH} t_{PHL}	A → Q_A	IN	to Q_A	GND	Out	—	—	—
	A → Q_D	IN	to Q_A	GND	—	—	—	Out
	B → Q_B	4.5 V	IN	GND	—	Out	—	—
	B → Q_C	4.5 V	IN	GND	—	—	Out	—
	B → Q_D	4.5 V	IN	GND	—	—	—	Out
	R_0** → Q	IN*	to Q_A	IN	Out	Out	Out	Out

* For initialized.

** Measured with each input and unused inputs at 4.5 V.

Waveform

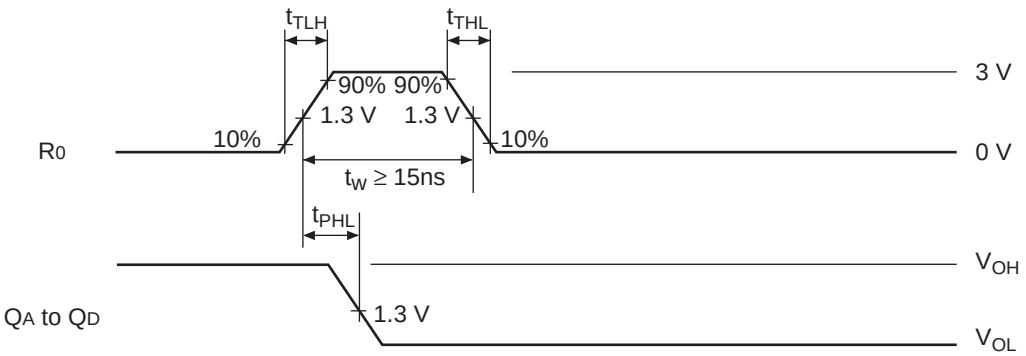
1. f_{max}, t_{PLH}, t_{PHL} (Clock → Q)



Notes: 1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 5$ ns, PRR = 1 MHz, duty cycle = 50% and for fmax., $t_{TLH} = t_{THL} \leq 2.5$ ns

2. t_n is reference bit time when all outputs are low.

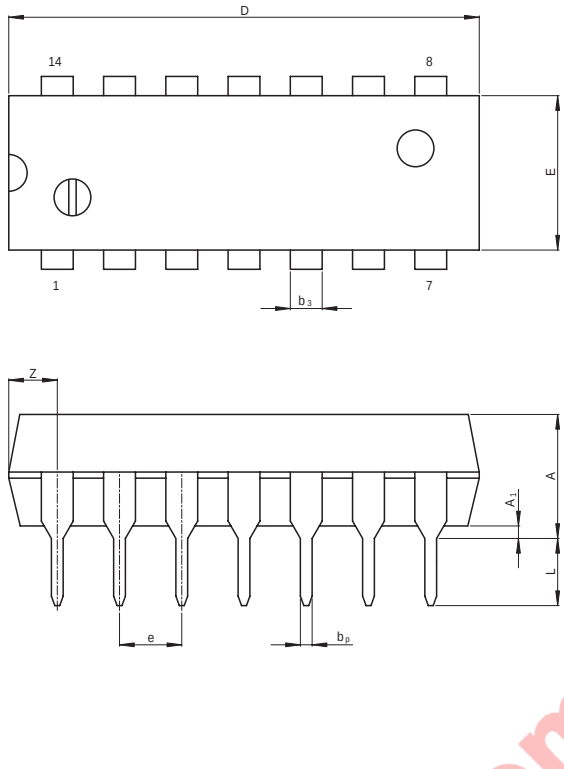
2. t_{PHL} ($R_0 \rightarrow Q$)



Notes: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 5$ ns

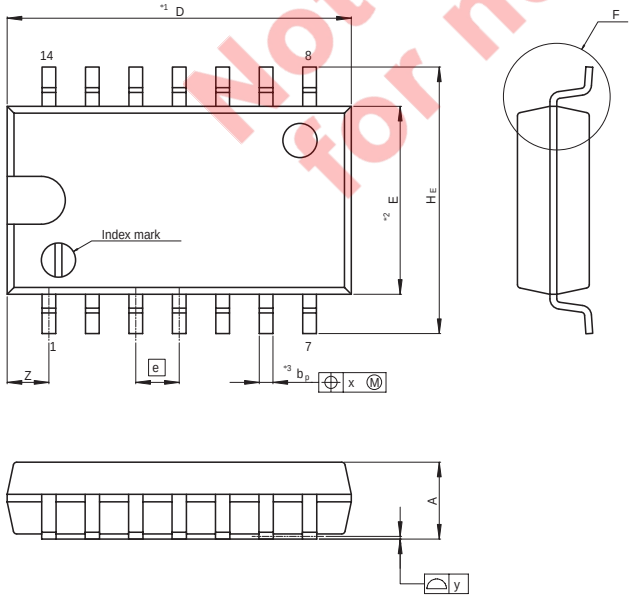
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g

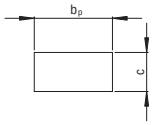


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	2.39
L	2.54	—	—

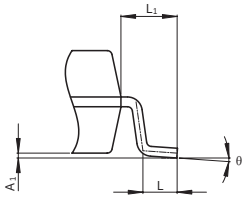
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	1.42
L	0.50	0.70	0.90
L_1	—	1.15	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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