

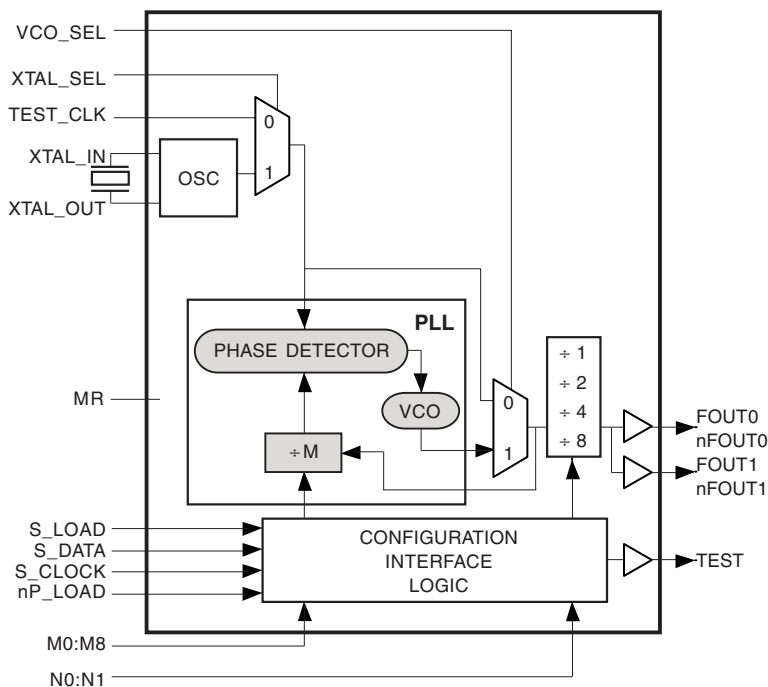
**GENERAL DESCRIPTION**

The ICS8442B is a general purpose, dual output Crystal-to-Differential LVDS High Frequency Synthesizer . The ICS8442B has a selectable TEST\_CLK or crystal input. The TEST\_CLK input accepts LVCMOS or LVTTTL input levels and translates them to LVDS levels. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interface to the configuration logic. The low phase noise characteristics of the ICS8442B makes it an ideal clock source for Gigabit Ethernet and Sonet applications.

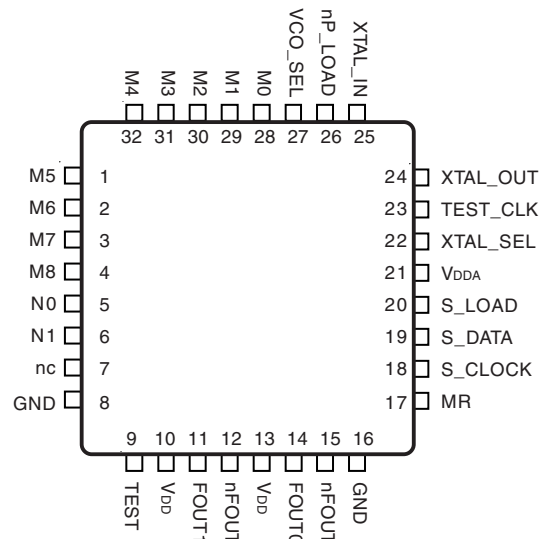
**FEATURES**

- Dual differential LVDS outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTTL TEST\_CLK
- Output frequency range: 31.25MHz to 700MHz
- Crystal input frequency range: 10MHz to 25MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 2.7ps (typical)
- Cycle-to-cycle jitter: 18ps (typical)
- 3.3V supply voltage
- 0°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

**BLOCK DIAGRAM**



**PIN ASSIGNMENT**



**ICS 8442B**  
**32-Lead LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View

**FUNCTIONAL DESCRIPTION**

*NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.*

The ICS8442B features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVDS output buffers. The divider provides a 50% output duty cycle.

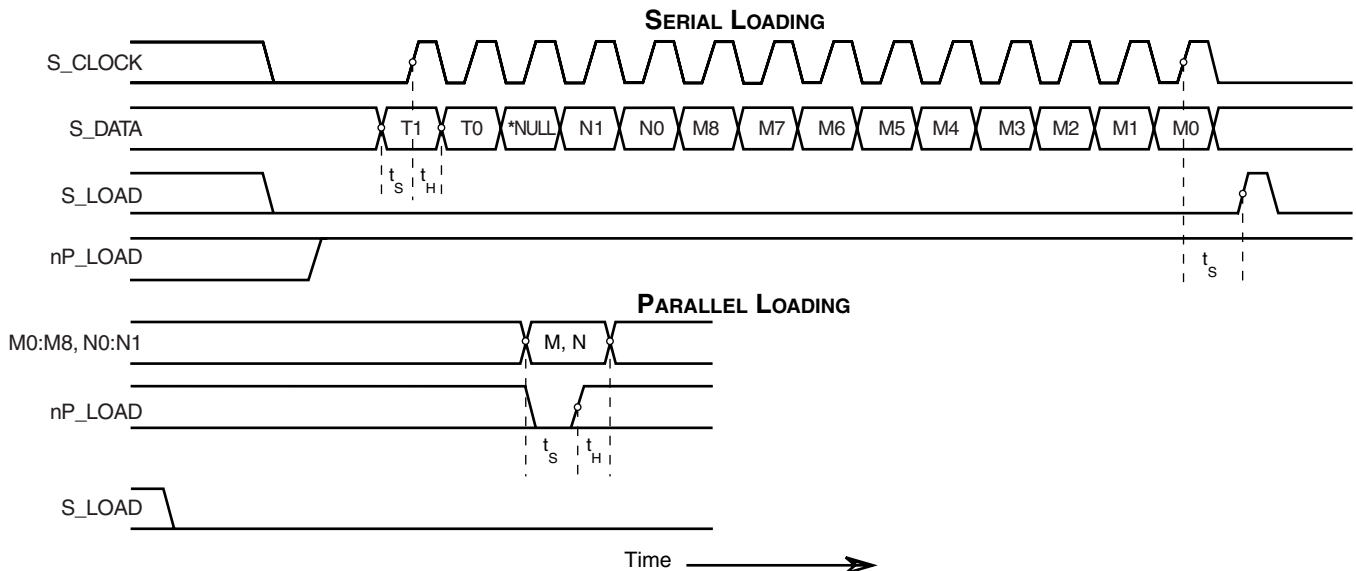
The programmable features of the ICS8442B support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. Figure 1 shows the timing diagram for each mode. In parallel mode, the nP\_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP\_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP\_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N

output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:  $f_{VCO} = f_{xtal} \times M$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as  $10 \leq M \leq 28$ . The frequency out is defined as follows:  $f_{OUT} = \frac{f_{VCO}}{N} = \frac{f_{xtal} \times M}{N}$

Serial operation occurs when nP\_LOAD is HIGH and S\_LOAD is LOW. The shift register is loaded by sampling the S\_DATA bits with the rising edge of S\_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S\_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S\_LOAD. If S\_LOAD is held HIGH, data at the S\_DATA input is passed directly to the M divider and N output divider on each rising edge of S\_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Input
1	0	Output of M divider
1	1	CMOS FOUT



**FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS**

\*NOTE: The NULL timing slot must be observed.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C Function Table. LVCMOS / LVTTTL interface levels.
7	nc	Unused		No connect.
8, 16	GND	Power		Power supply ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTTL interface levels.
10, 13	V <sub>DD</sub>	Power		Core supply pins.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. LVDS interface levels.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. LVDS interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M, N, and T values. LVCMOS / LVTTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTTL interface levels.
21	V <sub>DDA</sub>	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS / LVTTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS / LVTTTL interface levels.
24, 25	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. When HIGH, forces the outputs to a differential LOW state (FOUTx = LOW and nFOUTx = HIGH), but does not effect loaded M, N, and T values.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW  
 H = HIGH  
 X = Don't care  
 ↑ = Rising edge transition  
 ↓ = Falling edge transition

TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST\_CLK input frequency of 25MHz.

TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	250	700
0	1	2	125	350
1	0	4	62.5	175
1	1	8	31.25	87.5

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				182	mA
$I_{DDA}$	Analog Supply Current				16	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	M0-M8, N0, N1, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD, XTAL_SEL, VCO_SEL	2		$V_{DD} + 0.3$	V
		TEST_CLK	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	M0-M8, N0, N1, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD, XTAL_SEL, VCO_SEL	-0.3		0.8	V
		TEST_CLK	-0.3		1.3	V
$I_{IH}$	Input High Current	M0-M4, M6-M8, N0, N1, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD,	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		M5, XTAL_SEL, VCO_SEL	$V_{DD} = V_{IN} = 3.465V$		5	
$I_{IL}$	Input Low Current	M0-M4, M6-M8, N0, N1, MR, nP_LOAD, S_CLOCK, S_DATA, S_LOAD,	$V_{DD} = 3.465V,$ $V_{IN} = 0V$	-5		$\mu A$
		M5, XTAL_SEL, VCO_SEL	$V_{DD} = 3.465V,$ $V_{IN} = 0V$	-150		
$V_{OH}$	Output High Voltage	TEST; NOTE 1	2.6			V
$V_{OL}$	Output Low Voltage	TEST; NOTE 1			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DD}/2$ . See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

**TABLE 4C. LVDS DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		250	450	600	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.125	1.4	1.6	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**TABLE 5. INPUT FREQUENCY CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	TEST_CLK; NOTE 1	10		25	MHz
		XTAL_IN, XTAL_OUT; NOTE 1	10		25	MHz
		S_CLOCK			50	MHz

NOTE 1: For the input crystal and TEST\_CLK frequency range the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 10MHz valid values of M are  $25 \leq M \leq 70$ . Using the maximum frequency of 25MHz valid values of M are  $10 \leq M \leq 28$ .

**TABLE 6. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

**TABLE 7. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$F_{OUT}$	Output Frequency		31.25		700	MHz
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1, 3	N = 1, 2		18	28	ps
		N = 4		27	45	ps
$t_{jit(per)}$	Period Jitter, RMS; NOTE 1, 3			2.7	7	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				15	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	150		650	ps
$t_s$	Setup Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
$t_H$	Hold Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
odc	Output Duty Cycle; NOTE 4	N > 1	48		52	%
$t_{PW}$	Output Pulse Width	N = 1	$t_{Period}/2 - 150$		$t_{Period}/2 + 150$	ps
$t_{LOCK}$	PLL Lock Time				1	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: See Parameter Measurement Information section.

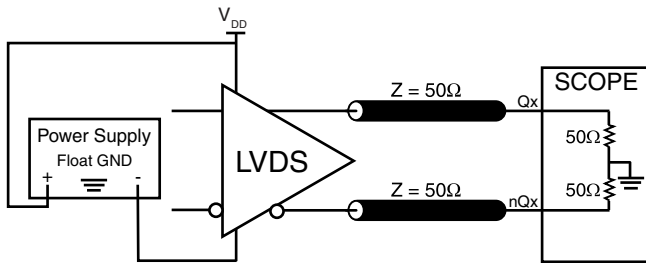
NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

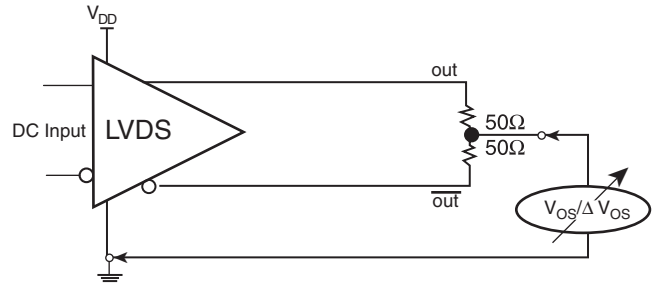
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: In the Applications Section, please refer to the application note, "Differential Duty Cycle Improvement."

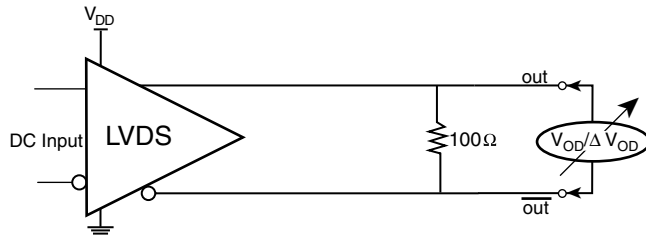
# PARAMETER MEASUREMENT INFORMATION



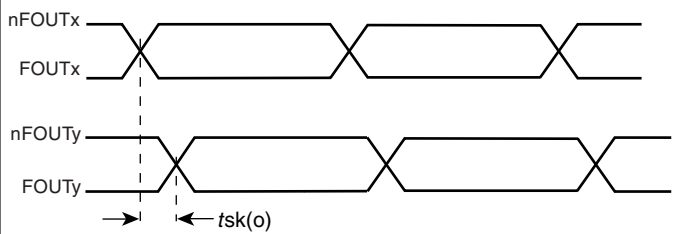
**3.3V OUTPUT LOAD TEST CIRCUIT**



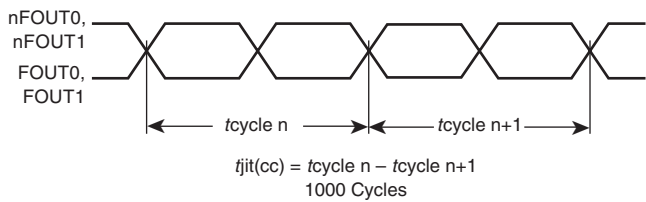
**OFFSET VOLTAGE SETUP**



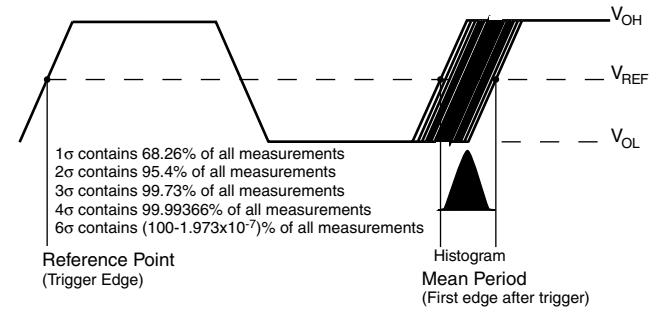
**DIFFERENTIAL OUTPUT VOLTAGE SETUP**



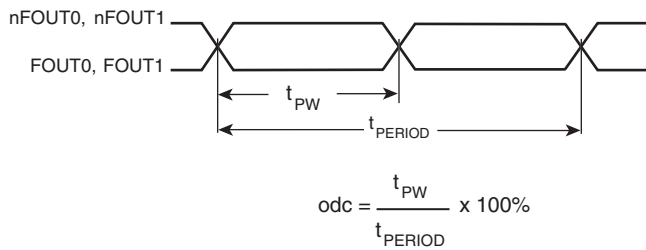
**OUTPUT SKEW**



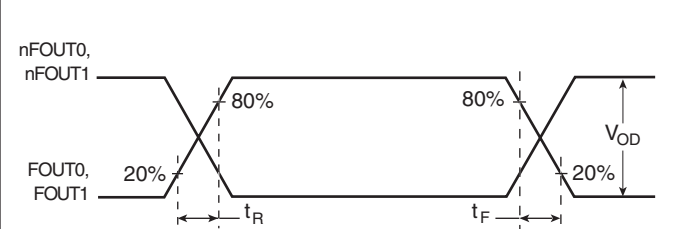
**Cycle-to-Cycle Jitter**



**Period Jitter**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**

## APPLICATION INFORMATION

### STORAGE AREA NETWORKS

A variety of technologies are used for interconnection of the elements within a SAN. The tables below lists the common frequencies used as well as the settings for the ICS8442B to generate the appropriate frequency.

**Table 8. Common SANs Application Frequencies**

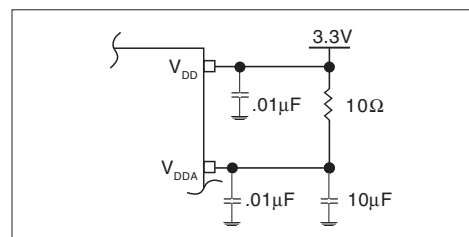
Interconnect Technology	Clock Rate	Reference Frequency to SERDES (MHz)	Crystal Frequency (MHz)
Gigabit Ethernet	1.25 GHz	125, 250, 156.25	25, 19.53125
Fibre Channel	FC1 1.0625 GHz FC2 2.1250 GHz	106.25, 53.125, 132.8125	16.6015625, 25
Infiniband	2.5 GHz	125, 250	25

**Table 9. Configuration Details for SANs Applications**

Interconnect Technology	Crystal Frequency (MHz)	ICS8442B Output Frequency to SERDES (MHz)	ICS8442B M & N Settings										
			M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1
	25	156.25	0	0	0	0	1	1	0	0	1	1	0
	19.53125	156.25	0	0	0	1	0	0	0	0	0	1	0
Fiber Channel 1	25	53.125	0	0	0	0	1	0	0	0	1	1	1
	25	106.25	0	0	0	0	1	0	0	0	1	1	0
Fiber Channel 2	16.6015625	132.8125	0	0	0	1	0	0	0	0	0	1	0
Infiniband	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8442B provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. Figure 2 illustrates how a  $10\Omega$  along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{DDA}$  pin.



**FIGURE 2. POWER SUPPLY FILTERING**



### CRYSTAL INPUT INTERFACE

A crystal can be characterized for either series or parallel mode operation. The ICS8442B has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate frequencies with accuracy

suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in Figure 3. Typical results using parallel 18pF crystals are shown in Table 10.

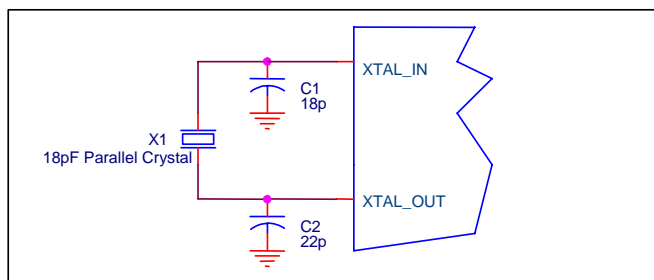


Figure 3. CRYSTAL INPUT INTERFACE

### LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 4. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver in-

put. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

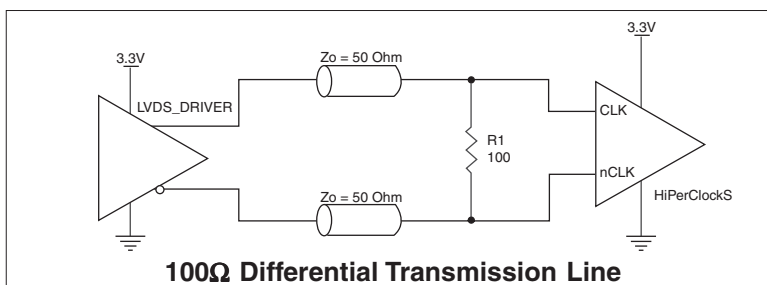


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

### DIFFERENTIAL DUTY CYCLE IMPROVEMENT

The schematic below is recommended for applications using the ÷1 output configuration for improving the differential duty cycle.

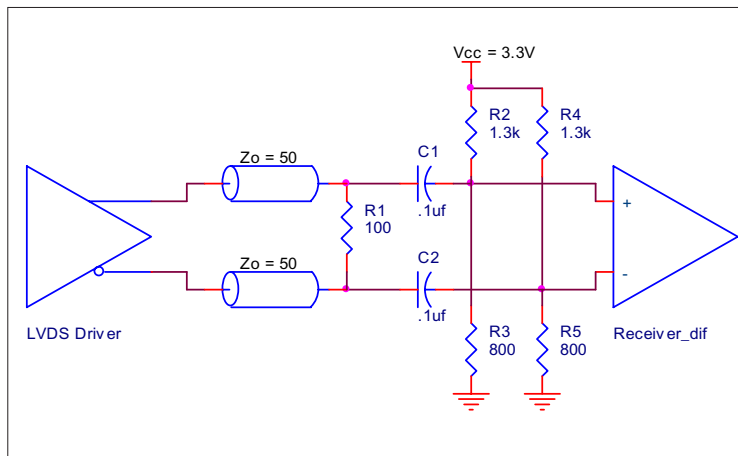
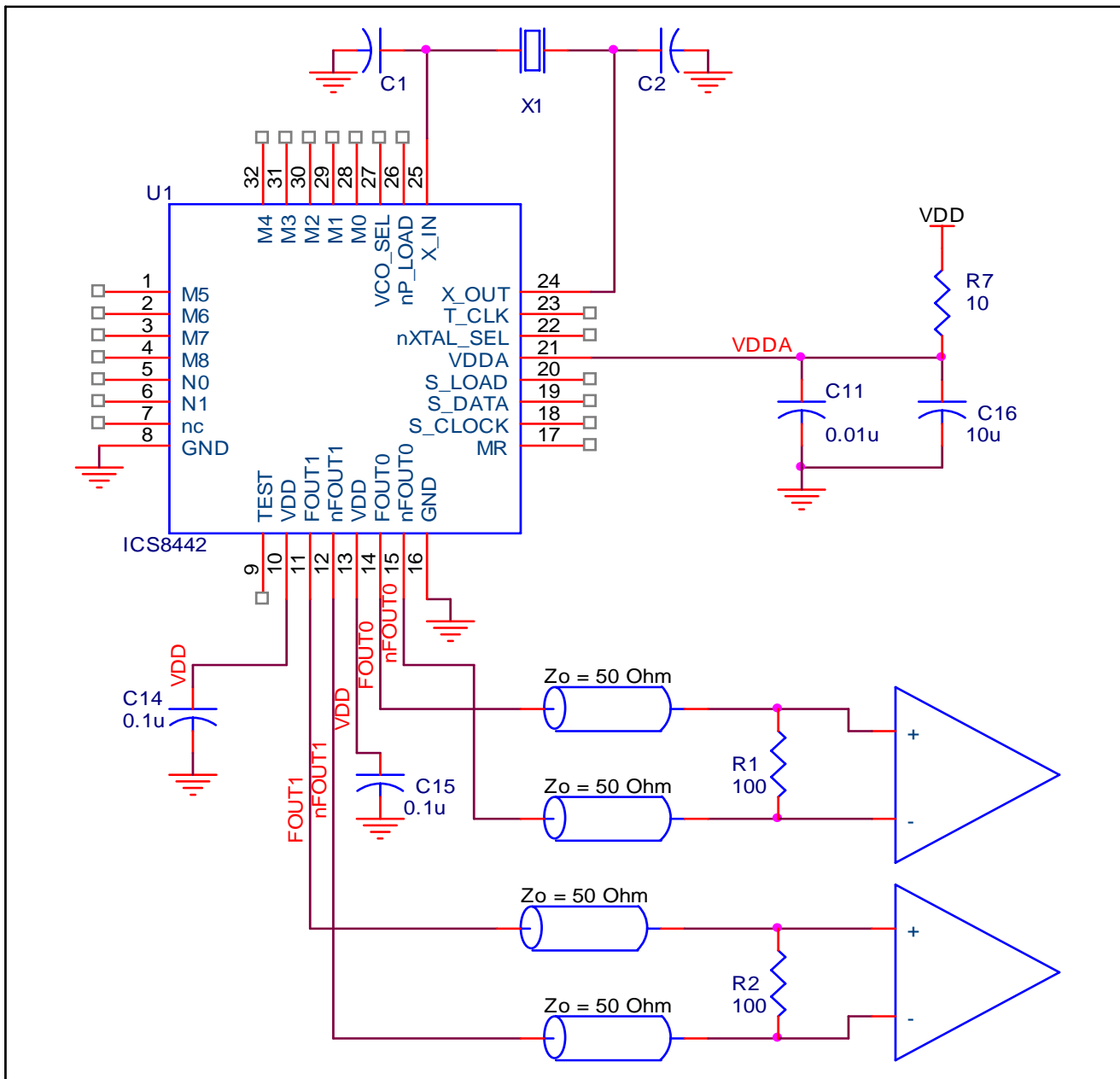


FIGURE 5. DIFFERENTIAL DUTY CYCLE IMPROVEMENT

**LAYOUT GUIDELINE**

The schematic of the ICS8442B layout example used in this layout guideline is shown in Figure 6A. The ICS8442B recommended PCB board layout for this example is shown in Figure 6B. This layout example is used as a general guideline. The

layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.



**FIGURE 6A. RECOMMENDED SCHEMATIC LAYOUT**

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

**POWER AND GROUNDING**

Place the decoupling capacitors C14 and C15 as close as possible to the power pins. If space allows, placing the decoupling capacitor at the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the pad size of the power (ground) at the decoupling capacitor. Maximize the number of vias between power (ground) and the pads. This can reduce the inductance between the power (ground) plane and the component power (ground) pins.

If  $V_{DDA}$  shares the same power supply with  $V_{DD}$ , insert the RC filter R7, C11, and C16 in between. Place this RC filter as close to the  $V_{DDA}$  as possible.

**CLOCK TRACES AND TERMINATION**

The component placements, locations and orientations should be arranged to achieve the best clock signal quality. Poor clock signal quality can degrade the system performance or cause system failure. In the synchronous high-speed digital system, the clock signal is less tolerable to poor signal quality than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The trace shape and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal

traces should be routed first and should be locked prior to routing other signal traces.

- The traces with 50Ω transmission lines TL1 and TL2 at FOUT and nFOUT should have equal delay and run adjacent to each other. Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock trace on same layer. Whenever possible, avoid any vias on the clock traces. Any via on the trace can affect the trace characteristic impedance and hence degrade signal quality.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow more space between the clock trace and the other signal trace.
- Make sure no other signal trace is routed between the clock trace pair.

The matching termination resistors R1 and R2 should be located as close to the receiver input pins as possible. Other termination scheme can also be used but is not shown in this example.

**CRYSTAL**

The crystal X1 should be located as close as possible to the pins 24 (XTAL\_OUT) and 25 (XTAL\_IN). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

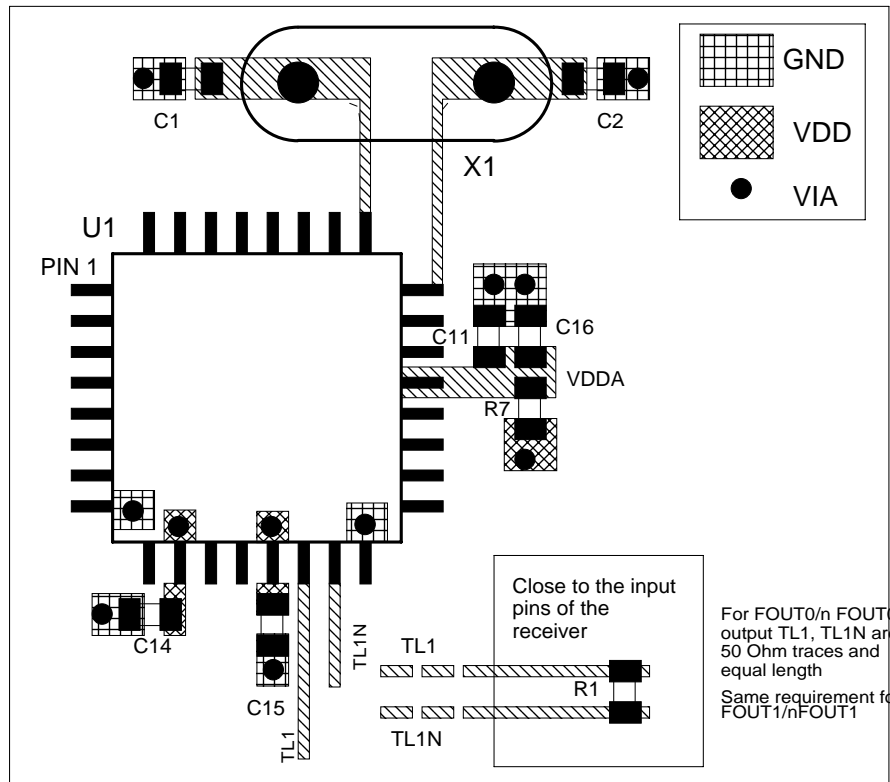


FIGURE 6B. PCB BOARD LAYOUT FOR ICS8442

## RELIABILITY INFORMATION

**TABLE 10.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TRANSISTOR COUNT**

The transistor count for ICS8442B is: 3662

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

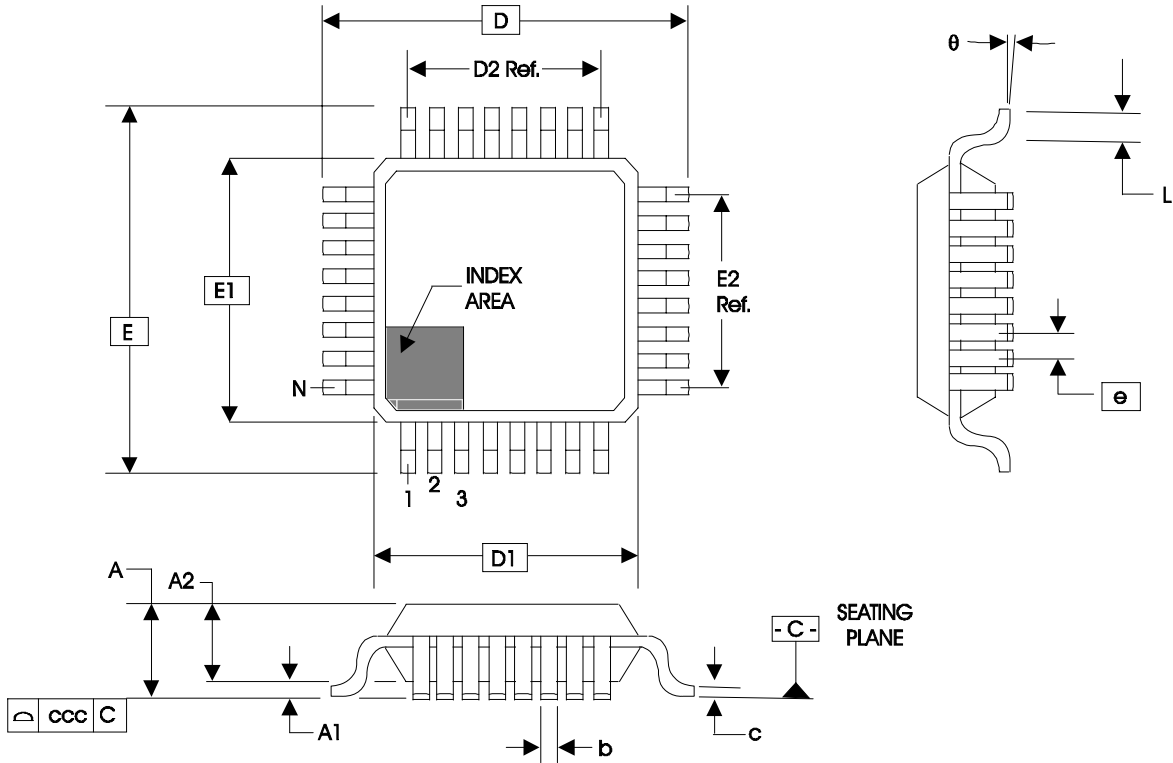


TABLE 11. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

**TABLE 12. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
8442BYLF	ICS8442BYLF	32 lead "Lead Free" LQFP	Tray	0°C to +85°C
8442BYLFT	ICS8442BYLF	32 lead "Lead Free" LQFP	Tape and Reel	0°C to +85°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T4A	5	Per PCN: N1308-01 Effective date 1/31/2014 Changed part number from ICS8442 to ICS8442B throughout the datasheet.	11/18/13
	T12	14	Power Supply DC Characteristics Table - changed $I_{DD}$ spec from 155mA max. to 182mA max; and changed $I_{DDA}$ spec from 20mA max. to 16mA max. Ordering Information Table - changed ordering information and marking revision from "A" to "B". Deleted leaded part information.	





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