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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M66257FP

5120 × 8-Bit × 2 Line Memory (FIFO)

REJ03F0251-0200
Rev.2.00
Sep 14, 2007

Description

The M66257FP is a high-speed line memory with a FIFO (First In First Out) structure of 5120-word × 8-bit double configuration which uses high-performance silicon gate CMOS process technology.

It allows simultaneous output of 1-line delay data and 2-line delay data, and is most suitable for data correction over multiple lines.

It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

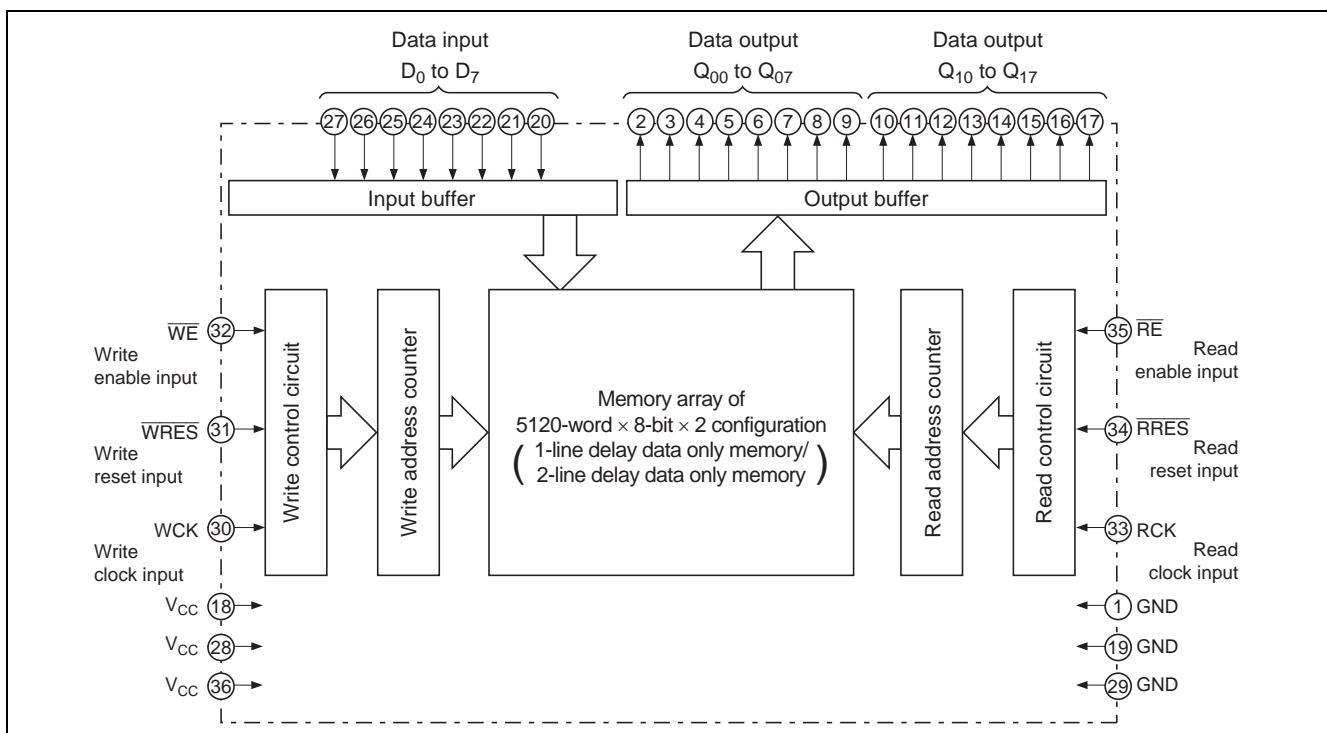
Features

- Memory configuration: 5120 words × 8 bits × 2 (dynamic memory)
- High-speed cycle: 25 ns (Min)
- High-speed access: 18 ns (Max)
- Output hold: 3 ns (Min)
- Fully independent, asynchronous write and read operations
- Output: 3 states
- Q₀₀ to Q₀₇: 1-line delay
- Q₁₀ to Q₁₇: 2-line delay

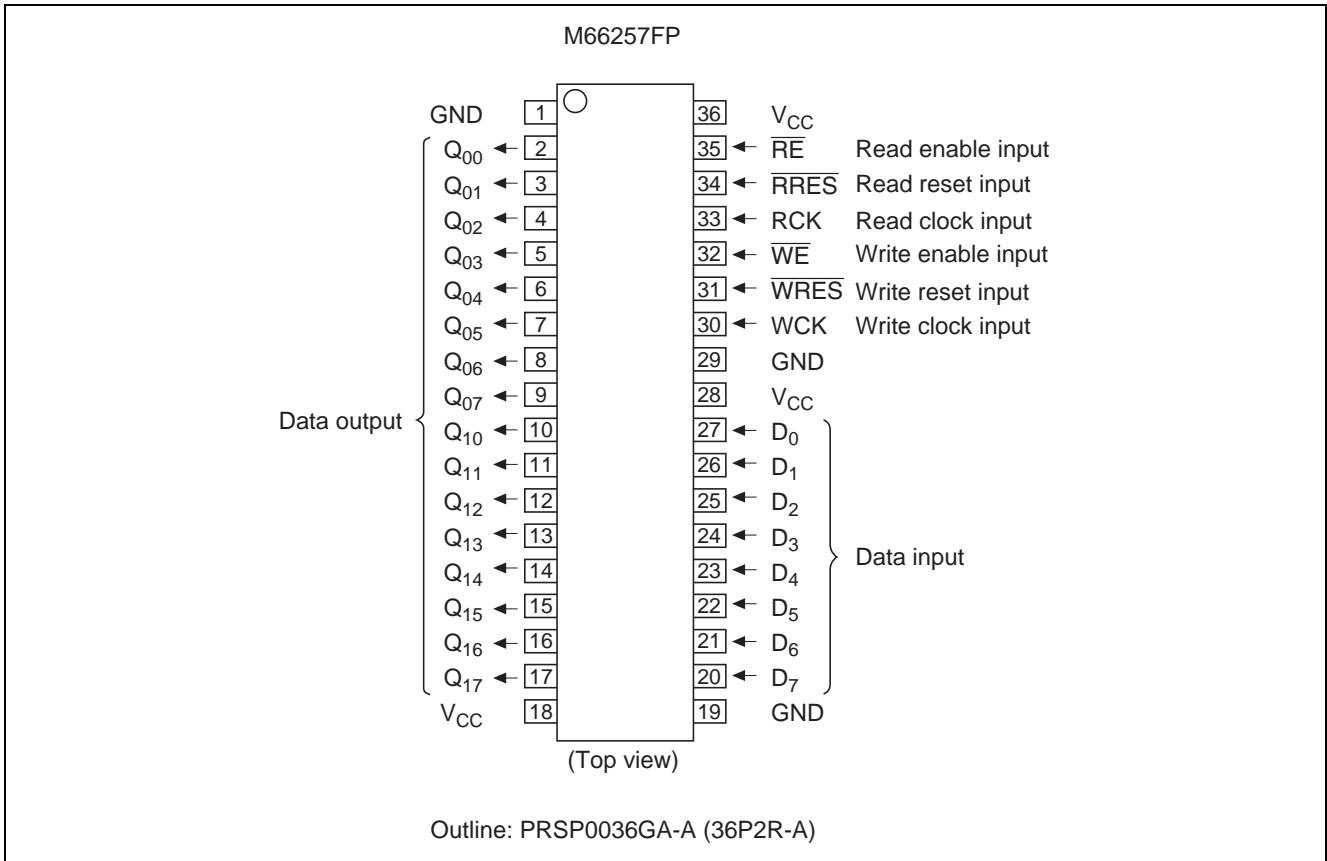
Application

Digital photocopiers, high-speed facsimile, laser beam printers.

Block Diagram



Pin Arrangement



Absolute Maximum Ratings

(Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.5 to +7.0	V	A value based on GND pin
Input voltage	V _I	-0.5 to V _{CC} + 0.5	V	
Output voltage	V _O	-0.5 to V _{CC} + 0.5	V	
Power dissipation	P _d	660	mW	Ta = 25°C
Storage temperature	T _{stg}	-65 to 150	°C	

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5	5.5	V
Supply voltage	GND	—	0	—	V
Operating ambient temperature	Topr	0	—	70	°C

Electrical Characteristics

(Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
"H" input voltage	V _{IH}	2.0	—	—	V	
"L" input voltage	V _{IL}	—	—	0.8	V	
"H" output voltage	V _{OH}	V _{CC} - 0.8	—	—	V	I _{OH} = -4 mA
"L" output voltage	V _{OL}	—	—	0.55	V	I _{OL} = 4 mA
"H" input current	I _{IH}	—	—	1.0	μA	V _I = V _{CC} WE, WRES, WCK, RE, RRES, RCK, D ₀ to D ₇
"L" input current	I _{IL}	—	—	-1.0	μA	V _I = GND WE, WRES, WCK, RE, RRES, RCK, D ₀ to D ₇
Off state "H" output current	I _{OZH}	—	—	5.0	μA	V _O = V _{CC}
Off state "L" output current	I _{OZL}	—	—	-5.0	μA	V _O = GND
Operating mean current dissipation	I _{CC}	—	—	120	mA	V _I = V _{CC} , GND, Output open t _{WCK} , t _{RCK} = 25 ns
Input capacitance	C _I	—	—	10	pF	f = 1 MHz
Off state output capacitance	C _O	—	—	15	pF	f = 1 MHz

Function

When write enable input $\overline{\text{WE}}$ is "L", the contents of data inputs D_0 to D_7 are written into 1-line delay data only memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter of 1-line delay data only memory is also incremented simultaneously.

The write functions given below are also performed in synchronization with rise edge of WCK.

When $\overline{\text{WE}}$ is "H", a write operation to 1-line delay data only memory is inhibited and the write address counter of 1-line delay data only memory is stopped.

When write reset input $\overline{\text{WRES}}$ is "L", the write address counter of 1-line delay data only memory is initialized.

When read enable input $\overline{\text{RE}}$ is "L", the contents of 1-line delay data only memory are output to data outputs Q_{00} to Q_{07} and those of 2-line delay data only memory to data outputs Q_{10} to Q_{17} in synchronization with the rise of read clock input RCK. At this time, the read address counters of 1-line and 2-line delay data only memories is also incremented simultaneously.

Moreover, data of Q_{00} to Q_{07} are written into 2-line delay data only memory in synchronization with rise edge of RCK. At this time, the write address of 2-line delay data only memory is incremented.

The read functions given below are also performed in synchronization with rise edge of RCK.

When $\overline{\text{RE}}$ is "H", a read operation from both of 1-line delay data only memory and 2-line delay data only memory is inhibited and the read address counter of each memory is stopped. The outputs of Q_{00} to Q_{07} and Q_{10} to Q_{17} are in the high impedance state.

Moreover, a write operation to 2-line delay data only memory is inhibited and the write address counter of 2-line delay data only memory is stopped.

When read reset input $\overline{\text{RRES}}$ is "L", the read address counter of 1-line delay data only memory, and the write address counter and read address counter of 2-line delay data only memory are initialized.

Switching Characteristics

($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Access time	t_{AC}	—	—	18	ns
Output hold time	t_{OH}	3	—	—	ns
Output enable time	t_{OEN}	3	—	18	ns
Output disable time	t_{ODIS}	3	—	18	ns

Timing Conditions

($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Write clock (WCK) cycle	t_{WCK}	25	—	—	ns
Write clock (WCK) "H" pulse width	t_{WCKH}	11	—	—	ns
Write clock (WCK) "L" pulse width	t_{WCKL}	11	—	—	ns
Read clock (RCK) cycle	t_{RCK}	25	—	—	ns
Read clock (RCK) "H" pulse width	t_{RCKH}	11	—	—	ns
Read clock (RCK) "L" pulse width	t_{RCKL}	11	—	—	ns
Input data setup time to WCK	t_{DS}	7	—	—	ns
Input data hold time to WCK	t_{DH}	3	—	—	ns
Reset setup time to WCK or RCK	t_{RESS}	7	—	—	ns
Reset hold time to WCK or RCK	t_{RESH}	3	—	—	ns
Reset nonselect setup time to WCK or RCK	t_{NRESS}	7	—	—	ns
Reset nonselect hold time to WCK or RCK	t_{NRESH}	3	—	—	ns
\overline{WE} setup time to WCK	t_{WES}	7	—	—	ns
\overline{WE} hold time to WCK	t_{WEH}	3	—	—	ns
\overline{WE} nonselect setup time to WCK	t_{NWES}	7	—	—	ns
\overline{WE} nonselect hold time to WCK	t_{NWEH}	3	—	—	ns
\overline{RE} setup time to RCK	t_{RES}	7	—	—	ns
\overline{RE} hold time to RCK	t_{REH}	3	—	—	ns
\overline{RE} nonselect setup time to RCK	t_{NRES}	7	—	—	ns
\overline{RE} nonselect hold time to RCK	t_{NREH}	3	—	—	ns
Input pulse rise/fall time	t_r, t_f	—	—	20	ns
Data hold time*	t_H	—	—	20	ms

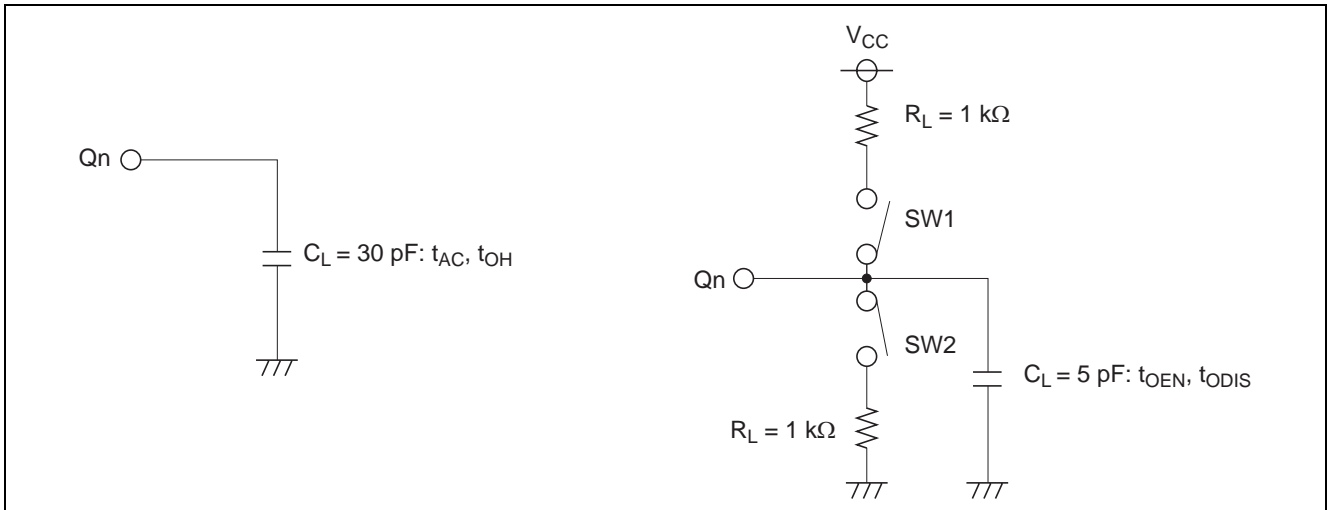
Notes: Reset the IC after power is turned on.

* For 1-line access, the following should be satisfied:

\overline{WE} "H" level period $< 20\text{ ms} - 5120 t_{WCK} - \overline{WRES}$ "L" level period

\overline{RE} "H" level period $< 20\text{ ms} - 5120 t_{RCK} - \overline{RRES}$ "L" level period

Test Circuit



Input pulse level: 0 to 3 V

Input pulse rise/fall time: 3 ns

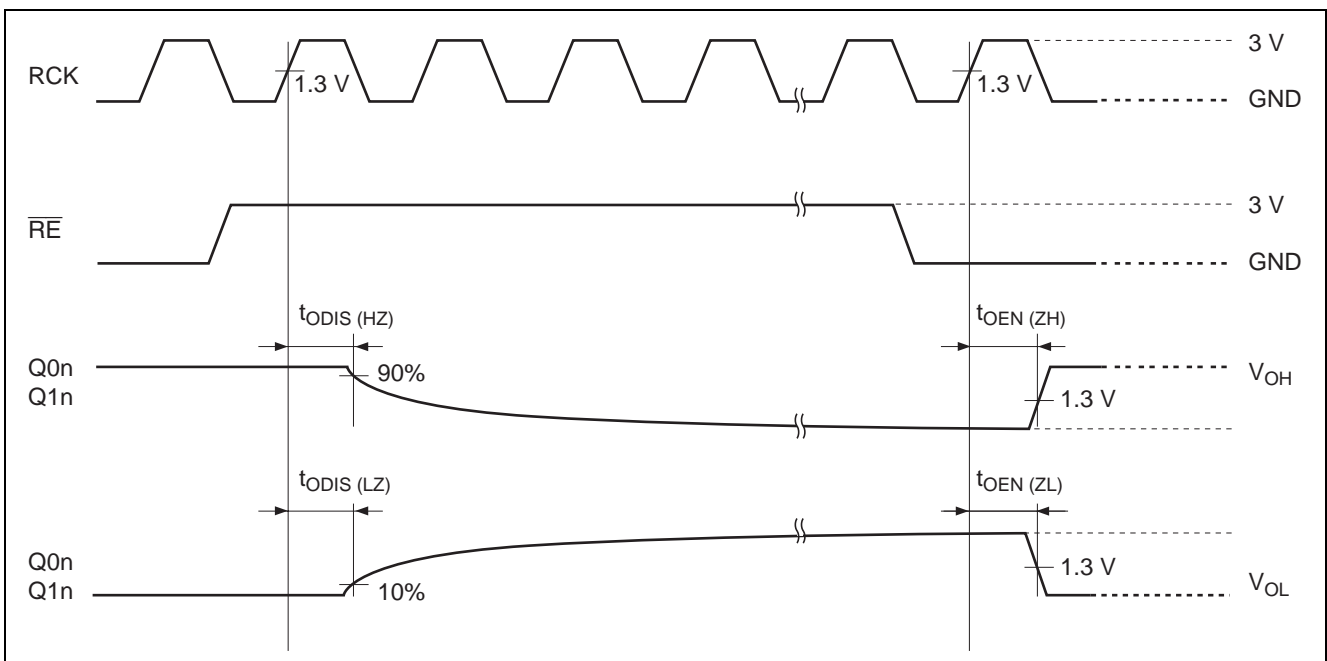
Decision voltage input: 1.3 V

Decision voltage output: 1.3 V (However, $t_{ODIS(LZ)}$ is 10% of output amplitude and $t_{ODIS(HZ)}$ is 90% of that for decision)

The load capacitance C_L includes the floating capacitance of connection and the input capacitance of probe.

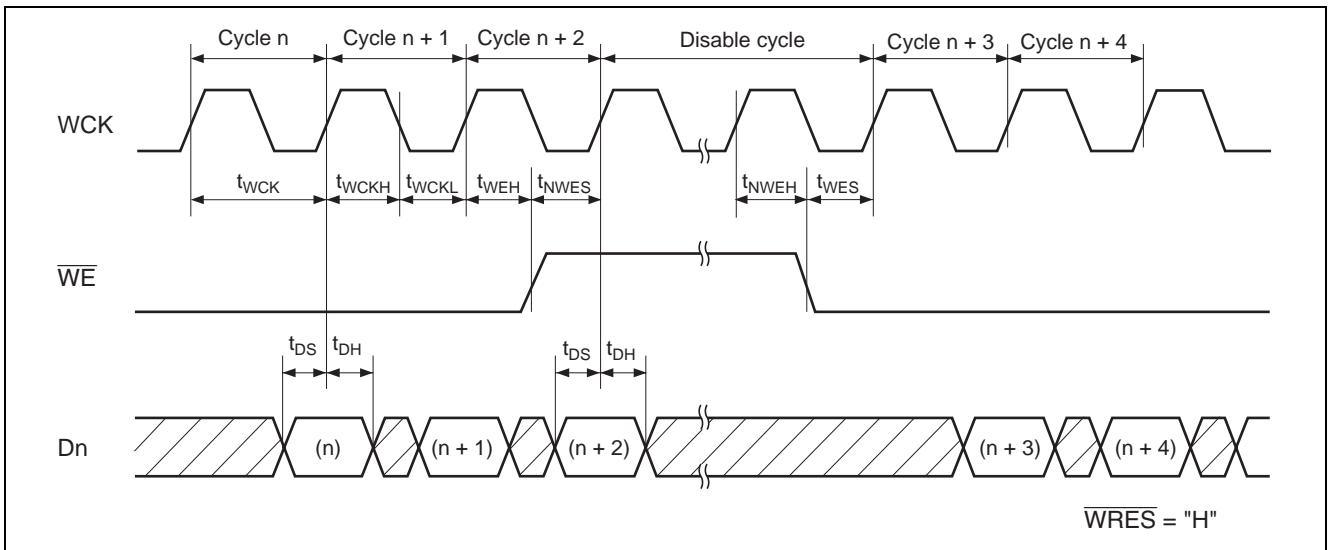
Parameter	SW1	SW2
$t_{ODIS(LZ)}$	Closed	Open
$t_{ODIS(HZ)}$	Open	Closed
$t_{OEN(ZL)}$	Closed	Open
$t_{OEN(ZH)}$	Open	Closed

t_{ODIS}/t_{OEN} Test Condition

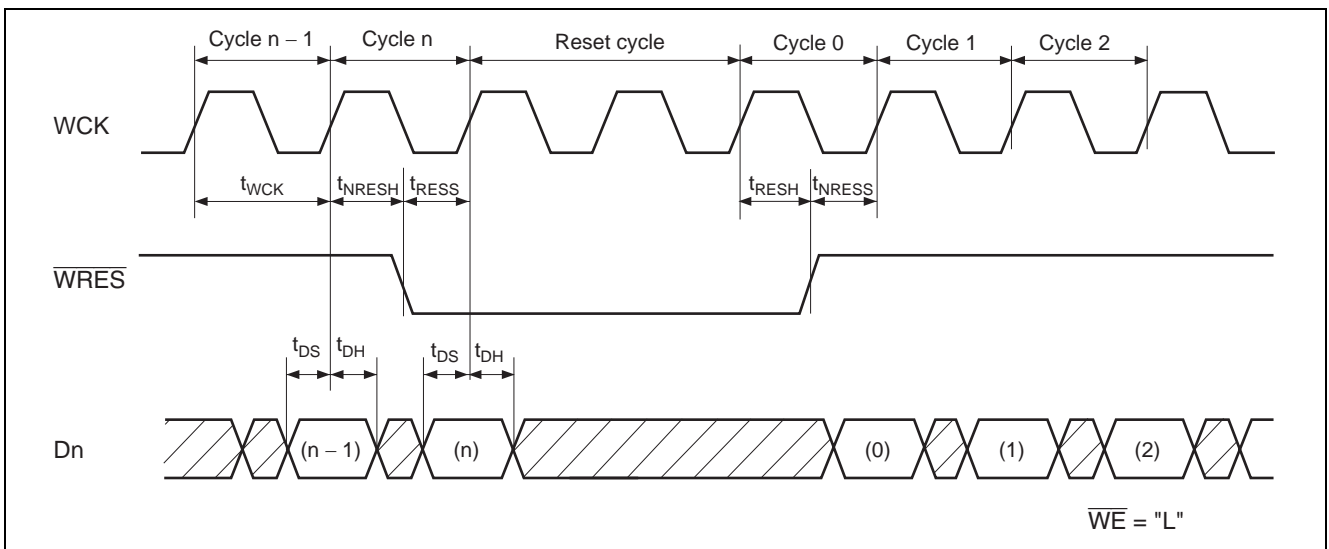


Operating Timing

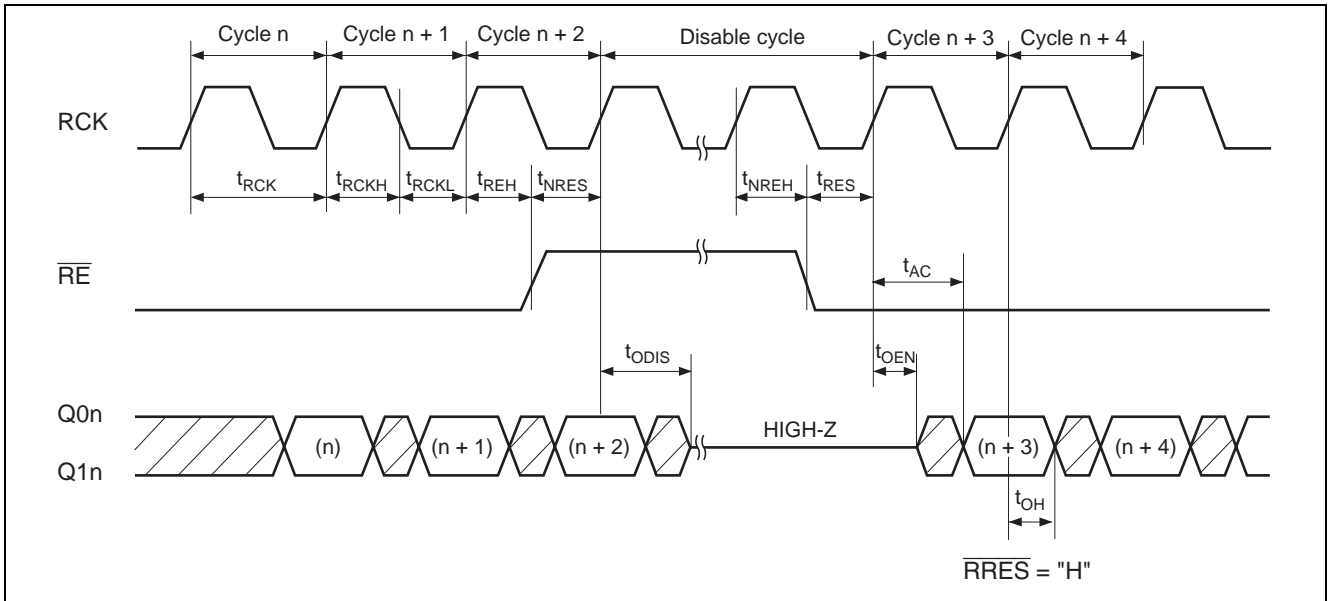
Write Cycle



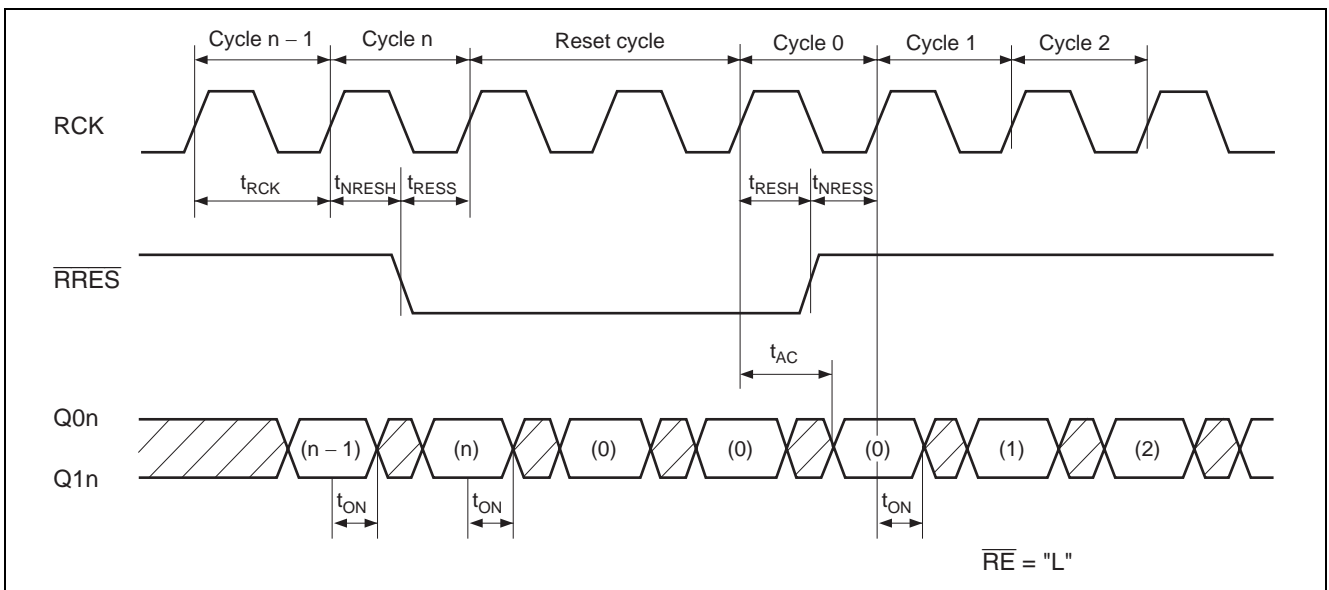
Write Reset Cycle



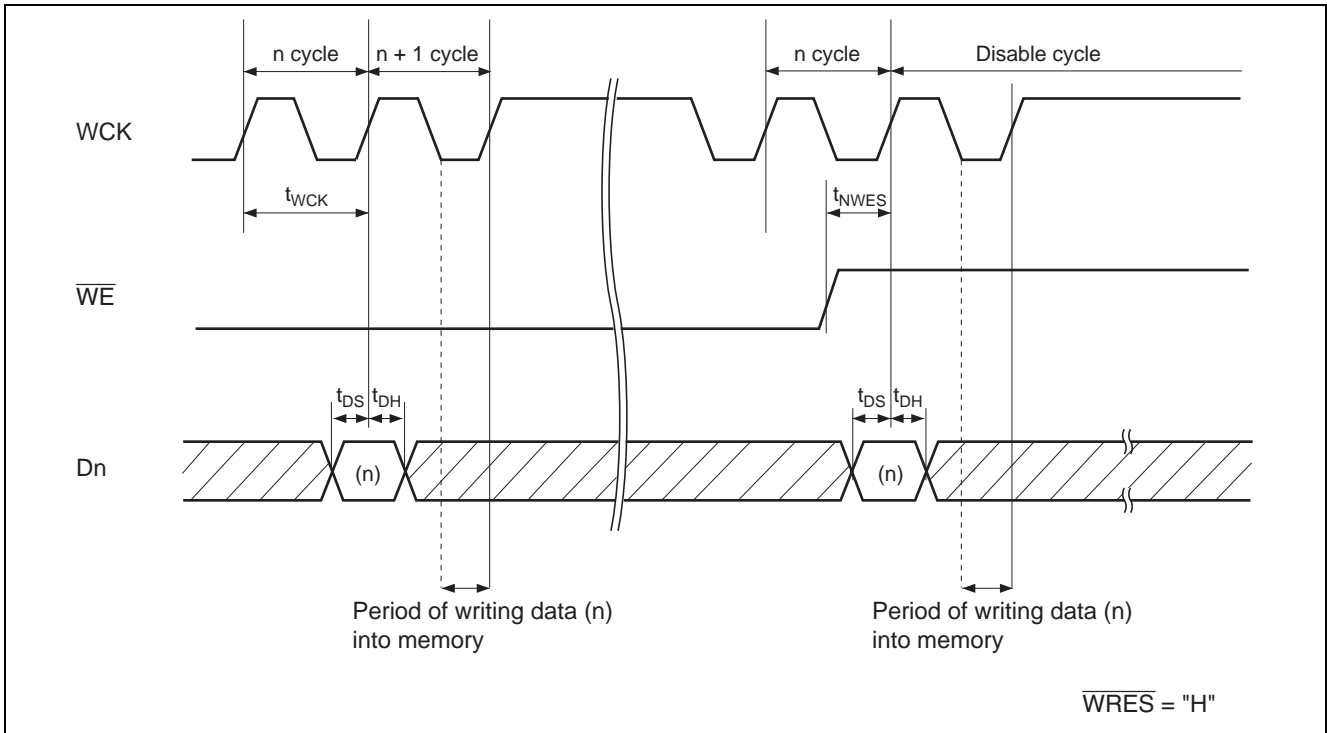
Read Cycle



Read Reset Cycle



Note at WCK Stop



Input data Dn of n cycle is read at the rising edge after WCK of n cycle. Writing operation starts in the "L" period of WCK of n + 1 cycle and ends at the rising edge after n + 1 cycle.

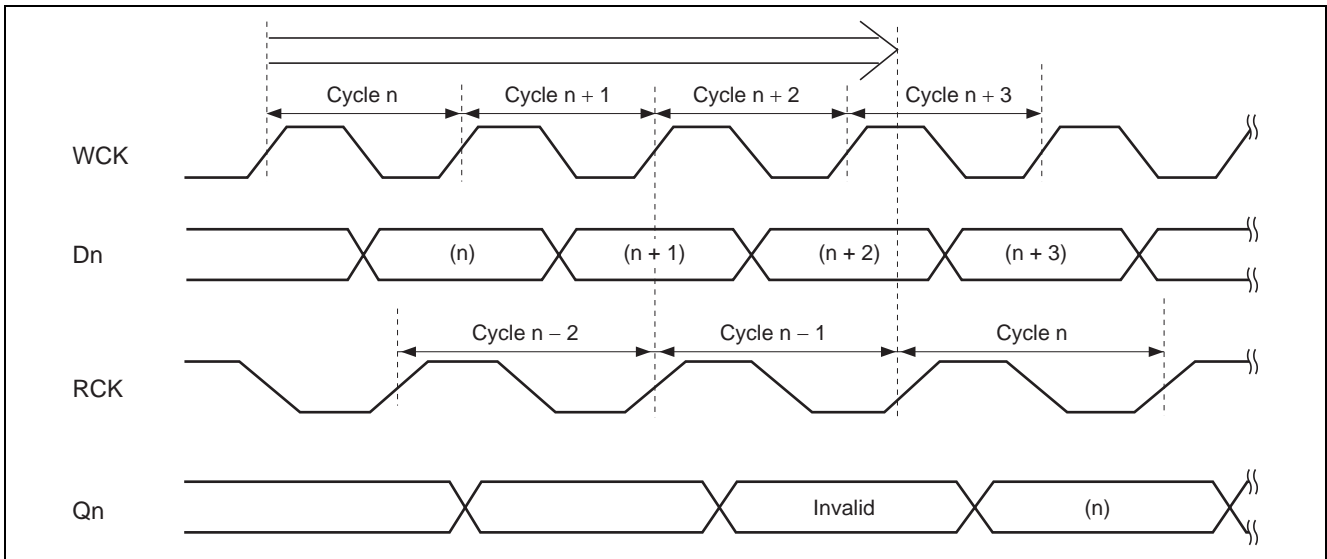
To stop reading write data at n cycle, input WCK for up to the rising edge of n + 1 cycle.

When the cycle next to n cycle is a disable cycle, input of WCK for a cycle is required after a disable cycle as well.

Shortest Read of Data "n" Written in Cycle n

(Cycle n - 1 on read side should be started after end of cycle n + 1 on write side)

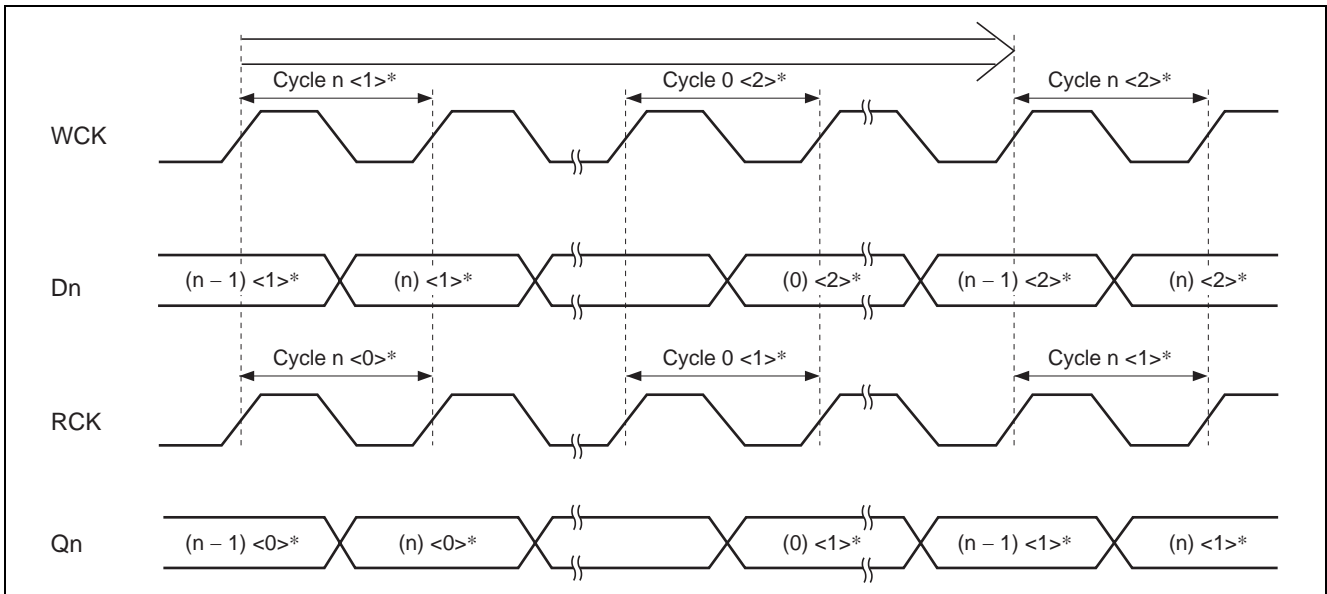
When the start of cycle n - 1 on read side is earlier than the end of cycle n + 1 on write side, output Qn of cycle n becomes invalid. In the figure shown below, the read of cycle n - 1 is invalid.



Longest Read of Data "n" Written in Cycle n: 1-line Delay

(Cycle n <1>* on read side should be started when cycle n <2>* on write is started)

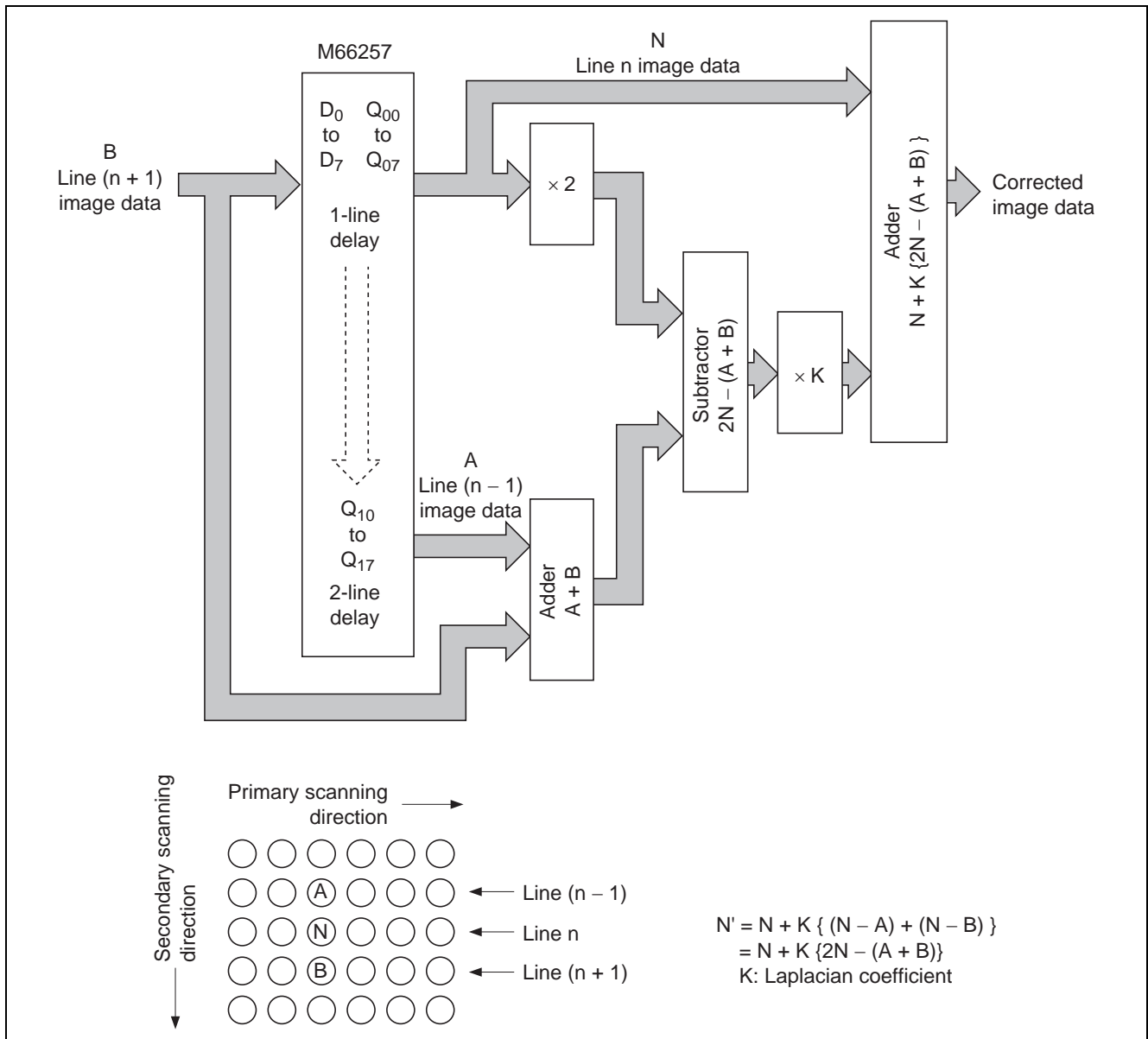
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.



Note: <0>*, <1>* and <2>* indicates a line value.

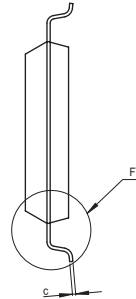
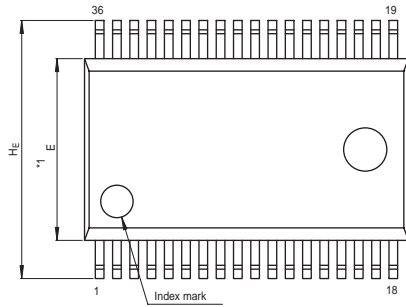
Application Example

Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction

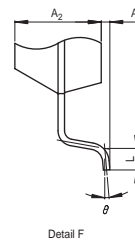
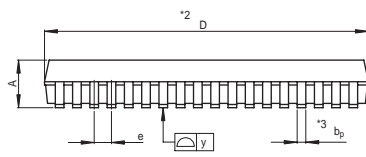


Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-A	36P2R-A	0.5g



NOTE)
 1. DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A ₂	—	2.0	—
A	—	—	2.4
A ₁	0.05	—	—
b _p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H _E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

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