To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

EOL announced Product

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EOL announced product

M66312P/FP

8-Bit LED Driver with Shift Register and Latched 3-State Outputs

REJ03F0178-0201
Rev.2.01
Mar 31, 2008

Description

M66312 is a LED array driver having a 8-bit serial input and parallel output shiftregister function with 3-state output latch.

This product guarantees the output electric current of 16 mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

EOL announced Product

Features

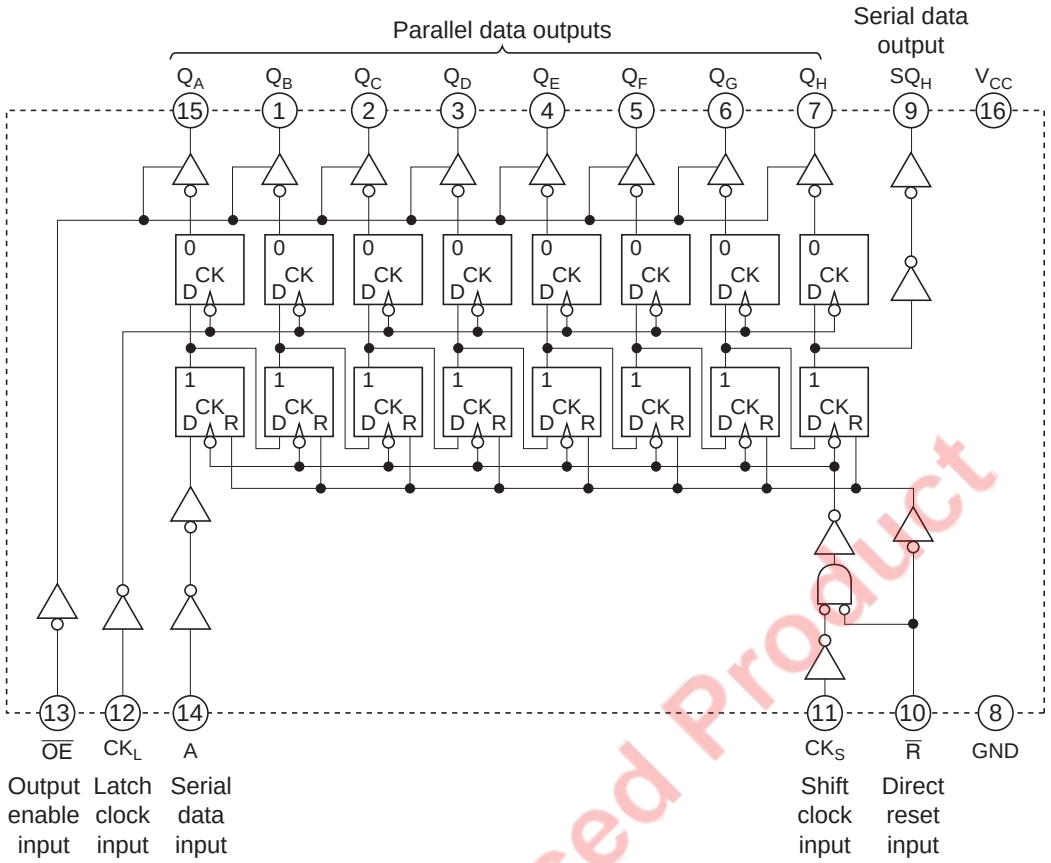
- High output current I_{OL} = 16 mA, I_{OH} = −16 mA
- High speed (clock frequency): 30 MHz (typ)
  (C_L = 50 pF, V_{CC} = 5 V)
- Low power dissipation: 20 µW/package (max)
  (V_{CC} = 5 V, Ta = 25°C, quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range: Ta = –40 to +85°C

Application

LED array drive of PRINTER

LED array drive of BUTTON TELEPHONE

Block Diagram



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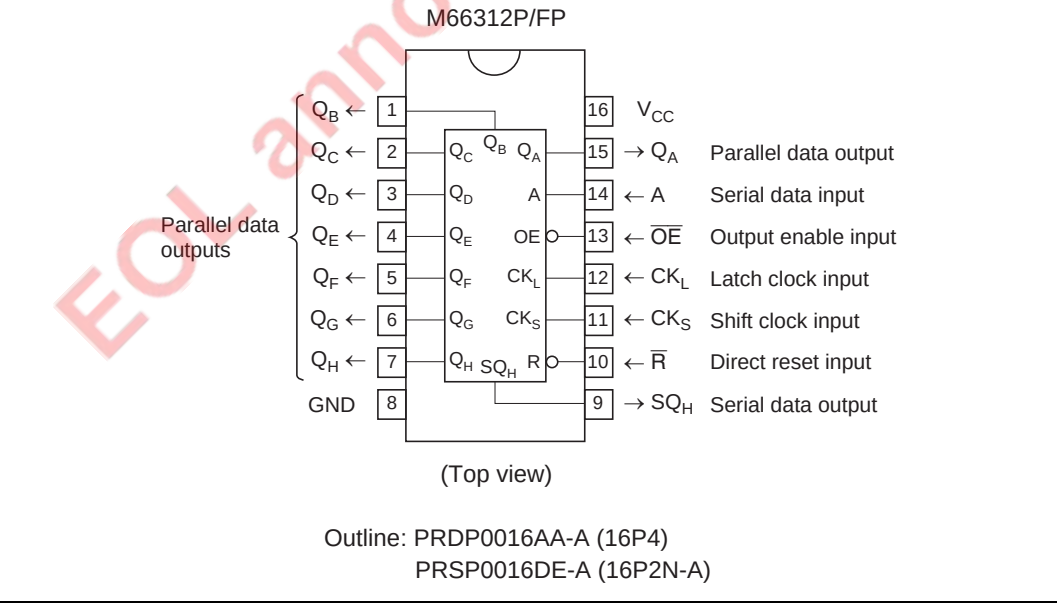
Pin Arrangement



Outline: PRDP0016AA-A (16P4)
PRSP0016DE-A (16P2N-A)

Functional Description

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when “L” changes to “H”.

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shiting registers one by one when a pulse is impressed to CK_S. When A is “H”, the signal of “H” shifts. When A is “L”, the signal of “L” shifts.

When the pulse is impressed to CK_L, the contents of the shifting register at that time are stored in a latching register, and they appear in the output from Q_A through Q_H are 3-state outputs.

To extend the number of bits, serial data output SQ_H is used to output the 8-bit of the shift register.

By connecting CK_S and CK_L, the shift register state delayed by 1 clock cycle is output at Q_A through Q_H.

When reset input $\overline{R}$ is low, shift register and SQ_H will be reset. To reset Q_A through Q_H to low-level, CK_L must be changed from low-level to high-level after the shift register is reset by $\overline{R}$.

When output-enable input $\overline{OE}$ is high, Q_A through Q_H will become high impedance state, but SQ_H is not changed.

Even if $\overline{OE}$ is changed, shift operation is not affected.

Function Table (Note)

Operation Mode		Input					Parallel Data Output								Serial Data Output SQ_H
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	
Reset	Shift t1	L	X	X	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	L
	Latch t2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift latch operation	Shift t1	H	↑	X	H	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t2	H	X	↑	X	L	H	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
	Shift t1	H	↑	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t2	H	X	↑	X	L	L	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
3 state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	q_H

Note ↑: Change from low-level to high-level
Q^0: Output state Q before CK_L changed
X: Irrelevant
q^0: Contents of shift register before CK_S changed
q: Contents of shift register
t_1, t_2: t_2 is set after t_1 is set
Z: High impedance

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Absolute Maximum Ratings

(Ta = −40 to +85°C, unless otherwise noted)

Item		Symbol	Ratings	Unit	Conditions
Supply voltage		V_{CC}	−0.5 to +7.0	V	
Input voltage		V_I	−0.5 to V_{CC} + 0.5	V	
Output voltage		V_O	−0.5 to V_{CC} + 0.5	V	
Input protection diode current		I_{IK}	−20	mA	V_I < 0 V
			20		V_I > V_{CC}
Output parasitic diode current		I_{OK}	−20	mA	V_O < 0 V
			20		V_O > V_{CC}
Output current per output pin	$\overline{Q}_A$ to $\overline{Q}_H$	I_O	±35	mA	
	SQ_H		±25		
Supply/GND current		I_{CC}	±132	mA	V_{CC}, GND
Power dissipation		Pd	500	mW	(Note)
Storage temperature range		Tstg	−65 to +150	°C	

Note: M66312FP; Ta = −40 to +70°C, Ta = 70 to 85°C are derated at −6 mW/°C.

Recommended Operating Conditions

(Ta = −40 to +85°C, unless otherwise noted)

Item		Symbol	Limits			Unit
			Min	Typ	Max	
Supply voltage		V_{CC}	4.5	5	5.5	V
Input voltage		V_I	0	—	V_{CC}	V
Output voltage		V_O	0	—	V_{CC}	V
Operating temperature range		Topr	−40	—	+85	°C
Input rising and falling time	V_{CC} = 4.5 V	tr, tf	0	—	500	ns
	V_{CC} = 5.5 V		0	—	400	

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Electrical Characteristics

(V_{CC} = 4.5 to 5.5V, unless otherwise noted)

Item	Symbol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = –40 to +85°C				
		Min	Typ	Max	Min	Max			
High-level input voltage	V_{IH}	0.70× V_{CC}	—	—	0.70×V_{CC}	—	V	V_O = 0.1 V, V_{CC}–0.1 V $\|I_O\|$ = 20 μA	
Low-level Input voltage	V_{IL}	—	—	0.30×V_{CC}	—	0.30×V_{CC}	V	V_O = 0.1 V, V_{CC}–0.1 V $\|I_O\|$ = 20 μA	
High-level output voltage Q_A to Q_H	V_{OH}	V_{CC}–0.1	—	—	V_{CC}–0.1	—	V	V_I = V_{IH}, V_{IL}	I_{OH} = –20 μA
		3.70(note)	—	—	3.55(note)	—		V_{CC} = 4.5 V	I_{OH} = –16 mA
High-level output voltage SQ_H	V_{OH}	V_{CC}–0.1	—	—	V_{CC}–0.1	—	V	V_I = V_{IH}, V_{IL}	I_{OH} = –20 μA
		4.0	—	—	3.9	—		V_{CC} = 4.5 V	I_{OH} = –4 mA
Low-level output voltage Q_A to Q_H	V_{OL}	—	—	0.1	—	0.1	V	V_I = V_{IH}, V_{IL}	I_{OL} = 20 μA
		—	—	0.7(note)	—	0.85(note)		V_{CC} = 4.5 V	I_{OL} = 16 mA
Low-level output voltage SQ_H	V_{OL}	—	—	0.1	—	0.1	V	V_I = V_{IH}, V_{IL}	I_{OL} = 20 μA
		—	—	0.4	—	0.5		V_{CC} = 4.5 V	I_{OL} = 4 mA
High-level input current	I_{IH}	—	—	0.1	—	1.0	μA	V_I = V_{CC}, V_{CC} = 5.5 V	
Low-level input current	I_{IL}	—	—	–0.1	—	–1.0	μA	V_I = GND, V_{CC} = 5.5 V	
Off state high-level output current Q_A to Q_H	I_{OZH}	—	—	1.0	—	10.0	μA	V_I = V_{IH}, V_{IL} V_{CC} = 5.5 V	V_O = V_{CC}
Off state low-level output current Q_A to Q_H	I_{OZL}	—	—	–1.0	—	–10.0	μA		V_O = GND
Quiescent supply current	I_{CC}	—	—	4.0	—	40.0	μA	V_I = V_{CC}, GND, V_{CC} = 5.5 V	

Note: Limits of single PIN operating state

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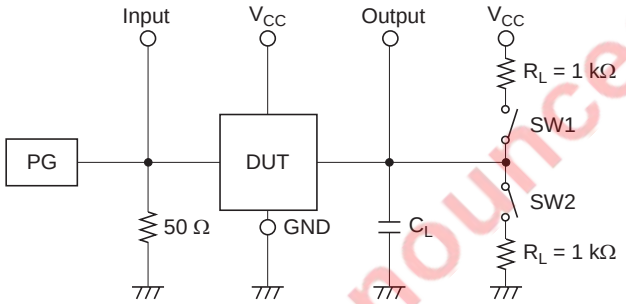
Switching Characteristics

(V_{CC} = 5 V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = –40 to +85°C			
		Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	15	—	—	12	—	MHz	C_L = 50 pF
Low-level to high-level and high-level to low-level output propagation time CK_S-SQ_H	t_{PLH}	—	—	70	—	88	ns	C_L = 15 pF (Note)
	t_{PHL}	—	—	70	—	88	ns	
High-level to low-level output propagation time $\overline{R}$-SQ_H	t_{PHL}	—	—	60	—	76	ns	
Low-level to high-level and high-level to low-level output propagation time CK_L-Q_A to Q_H	t_{PLH}	—	—	60	—	76	ns	C_L = 50 pF (Note)
	t_{PHL}	—	—	60	—	76	ns	
Output disable time from low-level and high-level $\overline{OE}$-Q_A to Q_H	t_{PLZ}	—	—	50	—	64	ns	C_L = 5 pF (Note)
	t_{PHZ}	—	—	50	—	64	ns	
Output enable time to low-level and high-level $\overline{OE}$-Q_A to Q_H	t_{PZL}	—	—	56	—	70	ns	C_L = 50 pF (Note)
	t_{PZH}	—	—	56	—	70	ns	

Note: Test Circuit



Item	SW1	SW2
t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10% to 90%): tr = 6 ns, tf = 6 ns

(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

Timing Requirements

(V_{CC} = 5 V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = –40 to +85°C			
		Min	Typ	Max	Min	Max		
CK_S, CK_L, $\overline{R}$ pulse width	t_w	32	—	—	40	—	ns	
A setup time with respect to CK_S	t_{su}	40	—	—	50	—	ns	
CK_S setup time with respect to CK_L	t_{su}	40	—	—	50	—	ns	
A hold time with respect to CK_S	t_h	10	—	—	10	—	ns	
$\overline{R}$ recovery time with respect to CK_S	t_{rec}	20	—	—	26	—	ns	

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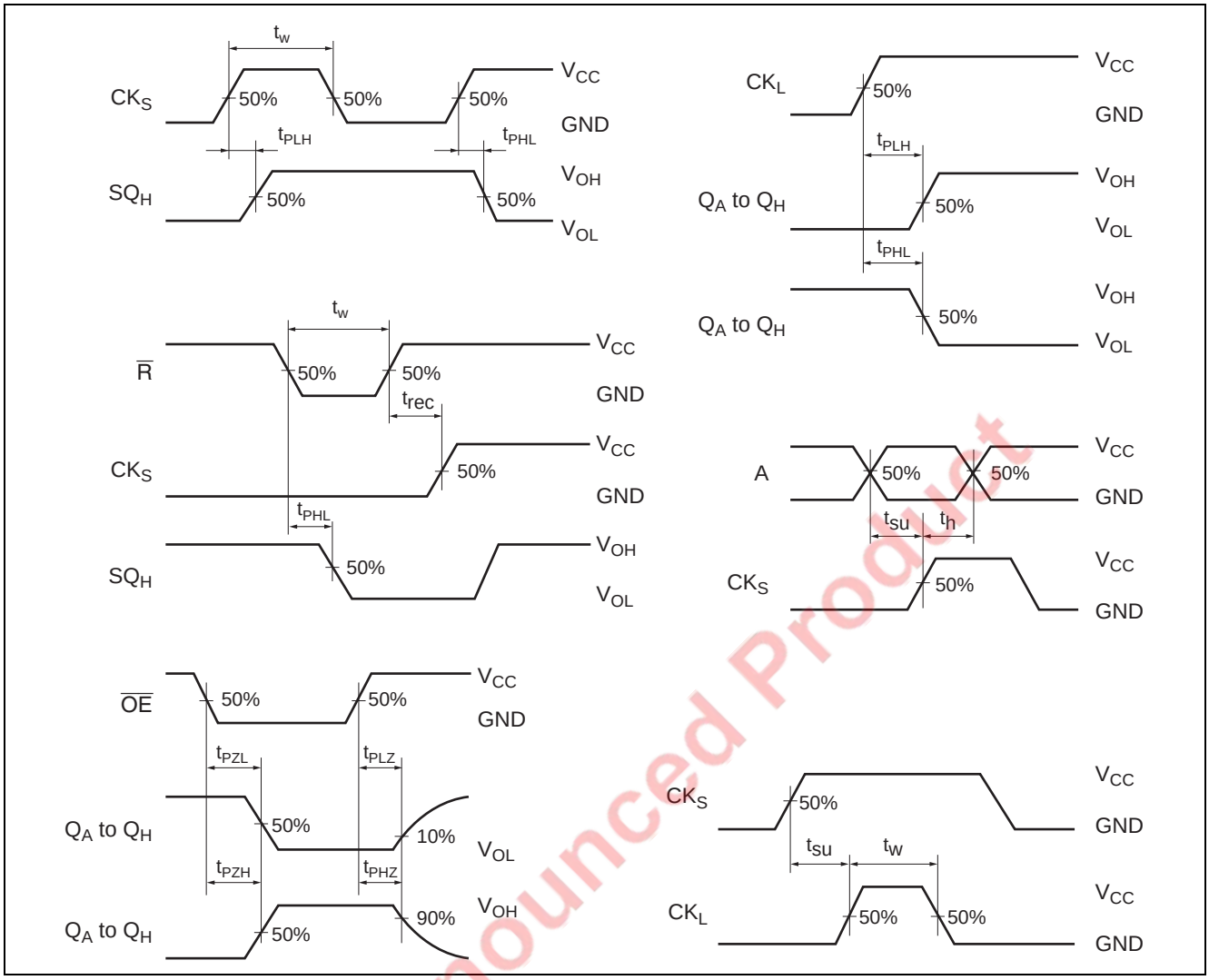
Timing Chart



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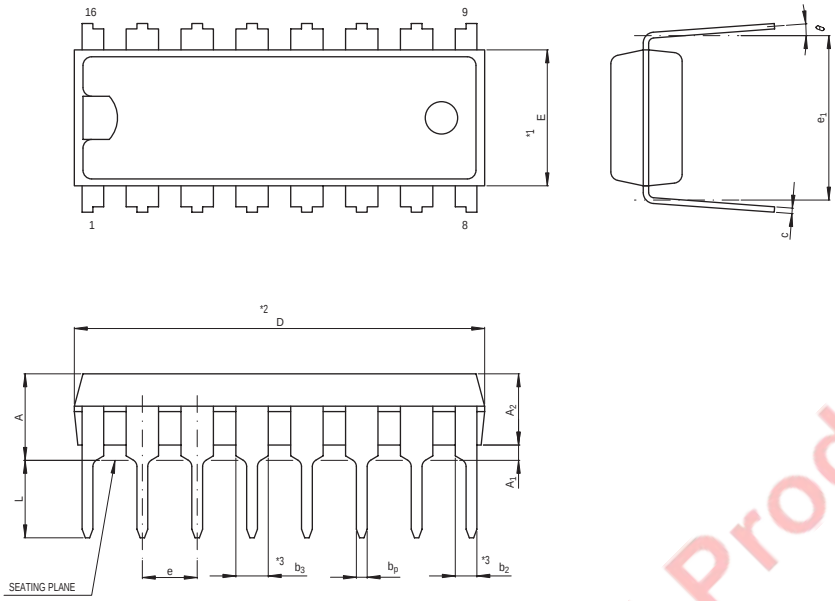
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19-2.54	PRDP0016AA-A	16P4	1.0g



NOTE)
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2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

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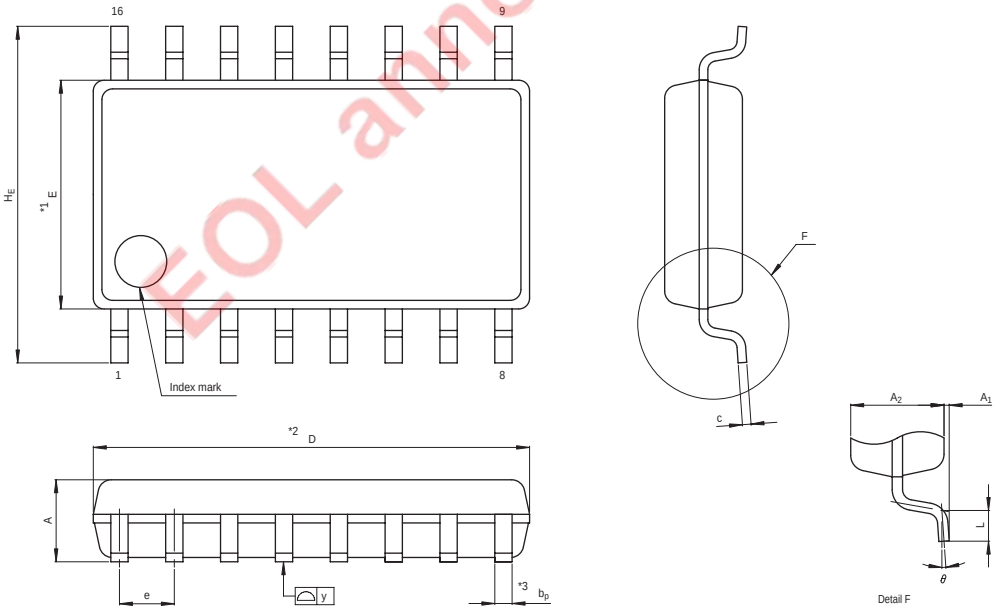
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.3x10.1-1.27	PRSP0016DE-A	16P2N-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

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