μPD5754T7A

R09DS0012EJ0100
Rev.1.00
Dec 22, 2010

SiGe/CMOS Integrated Circuit
4 × 2 IF Switch Matrix with Gain and Tone/Voltage Controller

FEATURES

- 4 independent IF channels, integral switching to channel input to either channel output
- 4 × 2 switch matrix with integrated IF amplifier and switch control - Tone/Voltage
  - Switch's Enable mode is linked V_{CC} external pins
- Mirror reversal logic pattern of μPD5739T7A
- Frequency range : f = 950 MHz to 2 150 MHz
- High isolation : $ISL_{D/U}$ = 30 dB TYP. @Worst mode
- Power gain : G_P = 18 dB TYP. @ $Z_S = Z_L$ = 50 Ω
- Power gain flatness : ΔG_P = 1.0 dB TYP.
- Surface mounting : 28-pin 5 × 5 mm square micro lead package (28-pin plastic QFN (0.5 mm pitch))

APPLICATIONS

- DBS IF switching
- Multiswitch, Switch box
- 4 × 2 switching application for microwave signal

ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Supplying Form
μPD5754T7A-E1	μPD5754T7A-E1-A	28-pin plastic QFN (0.5 mm pitch) (Pb-Free)	D5754	• Embossed tape 12 mm wide • Pin 8 to 14 face the perforation side of the tape • Qty 2.5 kpcs/reel • Dry packing specification (MSL 3 Equivalent)

Remark To order evaluation samples, please contact your nearby sales office.
Part number for sample order: μPD5754T7A

CAUTION

Observe precautions when handling because these devices are sensitive to electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}, $V_{CC}1$, $V_{CC}2$	+4.0	V
Power Dissipation Note	P_D	1.465	W
Storage Temperature	T_{stg}	–55 to +125	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Input Power	P_{in}	+5	dBm
POLA Control Input Voltage (POLA1 and POLA2)	V_{POLA}	+25	V
TONE Signal Input Voltage	V_{TONE}	1	V_{p-p}

Note: Mounted on double-sided copper-clad 50 × 50 × 0.51 mm laminates PWB, T_A = +85°C

RECOMMENDED OPERATING RANGE (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage Note	V_{DD}, $V_{CC}1$, $V_{CC}2$	+3.0	+3.3	+3.6	V
Operating Ambient Temperature	T_A	–40	+25	+85	°C
POLA Control Input Voltage	V_{POLA}	0	–	21	V
TONE Signal Frequency	f_{TONE}	18	22	26	kHz
TONE Signal Input Voltage	V_{TONE}	0.4	0.6	0.8	V_{p-p}

Note: $V_{CC}1 = V_{CC}2 = V_{DD}$

ELECTRICAL CHARACTERISTICS (T_A = +25°C, $V_{DD} = V_{CC}1 = V_{CC}2$ = +3.3 V, $Z_S = Z_L$ = 50 Ω for each port, worst mode, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Total Supply Current	I_{CC}	non–RF, 2 channels active total current of $I_{CC}1$, $I_{CC}2$, and I_{DD}	33	40	50	mA
Power Gain 1	G_P1	P_{in} = –30 dBm, f = 0.95 GHz	15	18	21	dB
Power Gain 2	G_P2	P_{in} = –30 dBm, f = 2.15 GHz	14.5	17.5	20.5	dB
Isolation D/U-ratio 2 Note	$ISL_{D/U}$ 2	P_{in} = –30 dBm, f = 2.15 GHz	25	30	–	dB
Gain 1 dB Compression Output Power 1	$P_{O\ (1\ dB)}$ 1	f = 0.95 GHz	5	8	–	dBm
Gain 1 dB Compression Output Power 2	$P_{O\ (1\ dB)}$ 2	f = 2.15 GHz	3	6	–	dBm
Output Return Loss 1	$RL_{out}1$	P_{in} = –30 dBm, f = 0.95 GHz	10	14	–	dB
Output Return Loss 2	$RL_{out}2$	P_{in} = –30 dBm, f = 2.15 GHz	10	12.5	–	dB
Noise Figure 1	NF1	f = 0.95 GHz	–	10.5	12.5	dB
Noise Figure 2	NF2	f = 2.15 GHz	–	11.5	13.5	dB
POLA Control Threshold Voltage, Channel Selection	V_{th_POLA}	OFF to ON	14	14.5	15.5	V
TONE Signal Threshold Voltage, Channel Selection	V_{th_TONE}	f_{TONE} = 22 kHz, Duty Cycle = 50%, pulse wave, OFF to ON	0.1	0.15	0.35	V_{p-p}

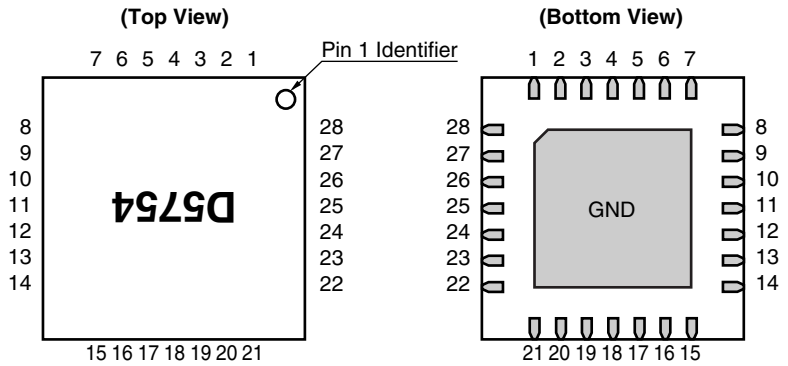
Note: Isolation D/U (Desire/Un-desire) ratio = |(Signal Leakage (off-state)) – (Power Gain (on-state))| at worst mode

STANDARD CHARACTERISTICS FOR REFERENCE
(T_A = +25°C, V_{DD} = V_{CC}1 = V_{CC}2 = +3.3 V, Z_S = Z_L = 50 Ω for each port, worst mode, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Supply Current of V_{CC}1, V_{CC}2	I_{CC}1, I_{CC}2		19	mA
Supply Current of V_{DD}	I_{DD}		2.0	mA
Gain Flatness	ΔG_P1	P_{in} = –30 dBm, f = 0.95 GHz to 2.15 GHz	1.0	dB
Differential Gain Between Active Channels	ΔG_P2		1.0	dB
Gain Change, selected channel	ΔG_P3		1.0	dB
Isolation D/U Ratio 1 Note	$ISL_{D/U}$ 1	P_{in} = –30 dBm, f = 0.95 GHz	30	dB
Input Return Loss 1	RL_{in}1	P_{in} = –30 dBm, f = 0.95 GHz	13	dB
Input Return Loss 2	RL_{in}2	P_{in} = –30 dBm, f = 2.15 GHz	10	dB
Output 3rd Order Intercept Point 1	$OIP_3$1	f1 = 950 MHz, f2 = 951 MHz	19	dBm
Output 3rd Order Intercept Point 2	$OIP_3$2	f1 = 2 150 MHz, f2 = 2 151 MHz	15	dBm
2nd Order Intermodulation Distortion	IM_2	f1 = 950 MHz, f2 = 951 MHz, P_{out} = –5 dBm/tone	44	dBc
2nd Harmonics	2f0	f0 = 1.0 GHz, P_{out} = –15 dBm	60	dBc
K factor 1	K1	P_{in} = –30 dBm, f = 0.95 GHz	2.5	–
K factor 2	K2	P_{in} = –30 dBm, f = 2.15 GHz	2.5	–
POLA Control Current	I_{POLA}	V_{POLA} = 21 V	50	μA
POLA Switching Time	T_{POLA}	V_{POLA} = 18 V, OFF to ON	1.0	μs
TONE Switching Time	T_{TONE}	f_{TONE} = 22 kHz, Duty Cycle = 50%, pulse wave, V_{TONE} = 600 mV_{p-p}, OFF to ON	250	μs

Note: Isolation D/U (Desire/Un-desire) ratio = |(Signal Leakage (off-state)) – (Power Gain (on-state))| at worst mode

PIN CONNECTIONS



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$V_{CC}1$	8	GND	15	IN-D	22	GND
2	OUT1	9	IN-B	16	GND	23	POLA2
3	GND	10	GND	17	GND	24	TONE2
4	GND	11	GND	18	GND	25	V_{DD}
5	GND	12	GND	19	GND	26	TONE1
6	GND	13	IN-C	20	OUT2	27	POLA1
7	IN-A	14	GND	21	$V_{CC}2$	28	GND

Remark Heat Sink (Bottom side) : GND

TRUTH TABLE OF SWITCHING BY CONDITION OF CONTROL VOLTAGE

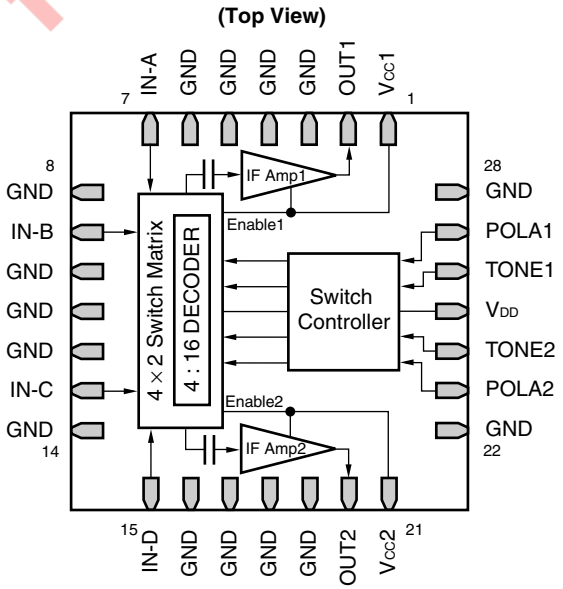
State			Output to Input State		Control Pins					
No.	Mode		OUT1	OUT2	TONE1	POLA1	TONE2	POLA2	$V_{CC}1$ (Enable1)	$V_{CC}2$ (Enable2)
1	Both OUTs Enabled	DD	IN-D	IN-D	22 kHz	Low	22 kHz	Low	3.3 V	3.3 V
2		DC		IN-C	22 kHz	Low	0	Low	3.3 V	3.3 V
3		DB		IN-B	22 kHz	Low	0	High	3.3 V	3.3 V
4		DA		IN-A	22 kHz	Low	22 kHz	High	3.3 V	3.3 V
5		CD	IN-C	IN-D	0	Low	22 kHz	Low	3.3 V	3.3 V
6		CC		IN-C	0	Low	0	Low	3.3 V	3.3 V
7		CB		IN-B	0	Low	0	High	3.3 V	3.3 V
8		CA		IN-A	0	Low	22 kHz	High	3.3 V	3.3 V
9		BD	IN-B	IN-D	0	High	22 kHz	Low	3.3 V	3.3 V
10		BC		IN-C	0	High	0	Low	3.3 V	3.3 V
11		BB		IN-B	0	High	0	High	3.3 V	3.3 V
12		BA		IN-A	0	High	22 kHz	High	3.3 V	3.3 V
13		AD	IN-A	IN-D	22 kHz	High	22 kHz	Low	3.3 V	3.3 V
14		AC		IN-C	22 kHz	High	0	Low	3.3 V	3.3 V
15		AB		IN-B	22 kHz	High	0	High	3.3 V	3.3 V
16		AA		IN-A	22 kHz	High	22 kHz	High	3.3 V	3.3 V
17	OUT1 Disabled	ND	None	IN-D	Any Note	Any Note	22 kHz	Low	0	3.3 V
18		NC		IN-C	Any Note	Any Note	0	Low	0	3.3 V
19		NB		IN-B	Any Note	Any Note	0	High	0	3.3 V
20		NA		IN-A	Any Note	Any Note	22 kHz	High	0	3.3 V
21	OUT2 Disabled	DN	IN-D	None	22 kHz	Low	Any Note	Any Note	3.3 V	0
22		CN	IN-C		0	Low	Any Note	Any Note	3.3 V	0
23		BN	IN-B		0	High	Any Note	Any Note	3.3 V	0
24		AN	IN-A		22 kHz	High	Any Note	Any Note	3.3 V	0
25	Both OUTs Disabled		None	None	Any Note	Any Note	Any Note	Any Note	0	0

Note: Any means High or Low, 22 kHz or 0.

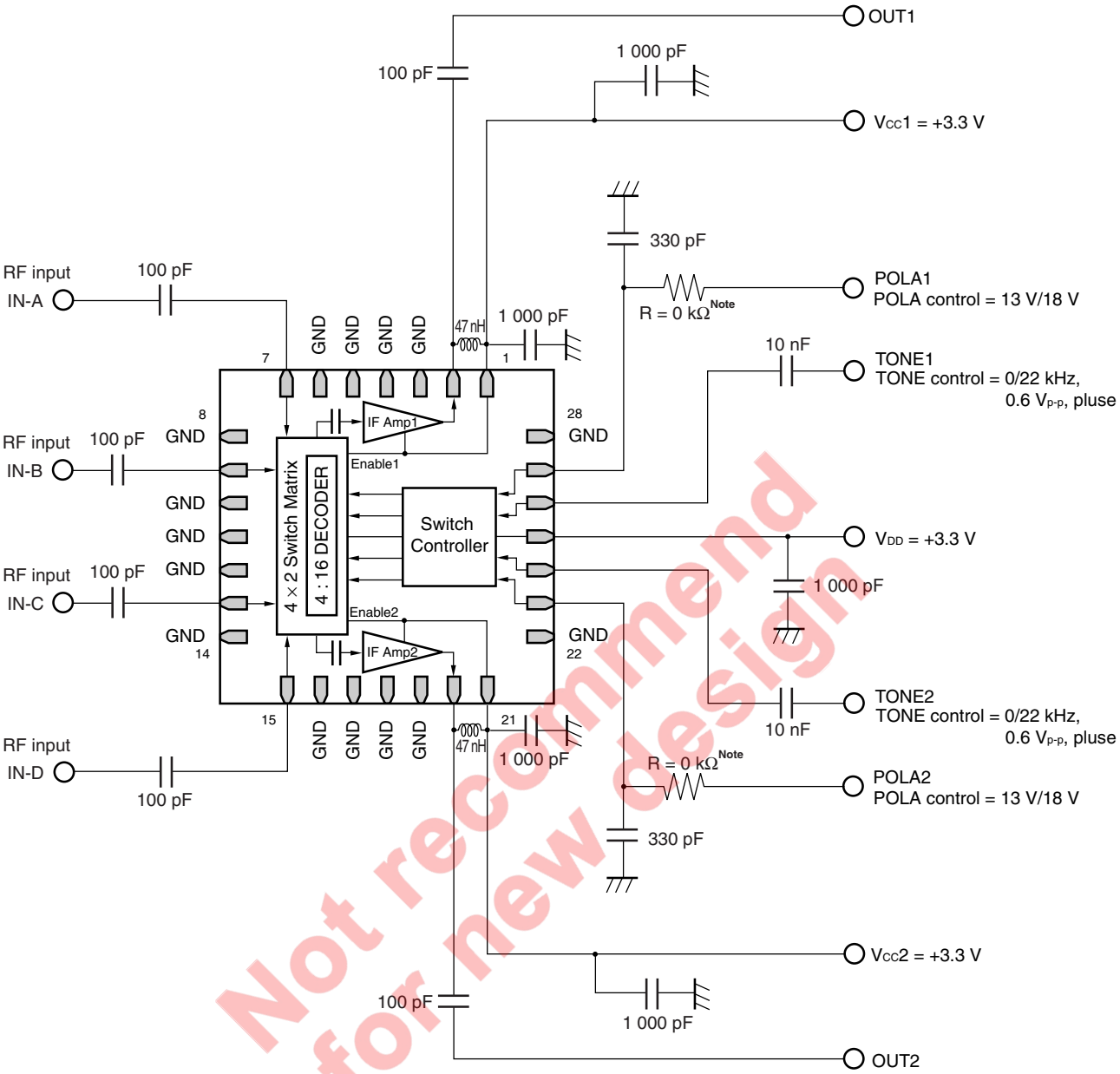
Remark Low : under +14 Vdc, High : +15.5 to +19.0 Vdc, V_{DD} = +3.3 Vdc

FUNCTIONAL DIAGRAM

(Top View)



EVALUATION CIRCUIT



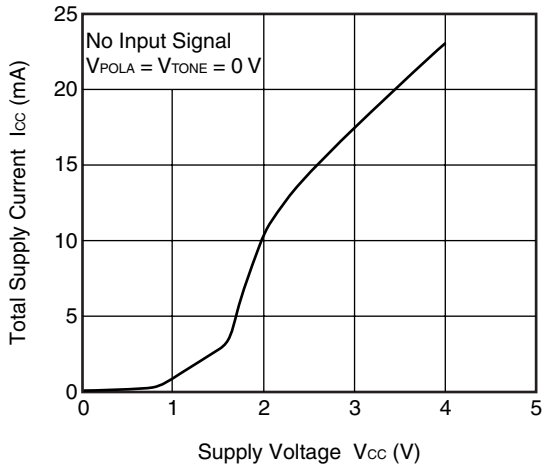
Note: R = 0 kΩ (at POLA control = 13 V/18 V)
= 5.6 kΩ (at POLA control = 14 V/18 V)

Remark Low : under +14 Vdc, High : +15.5 to +19.0 Vdc, V_{DD} = +3.3 Vdc

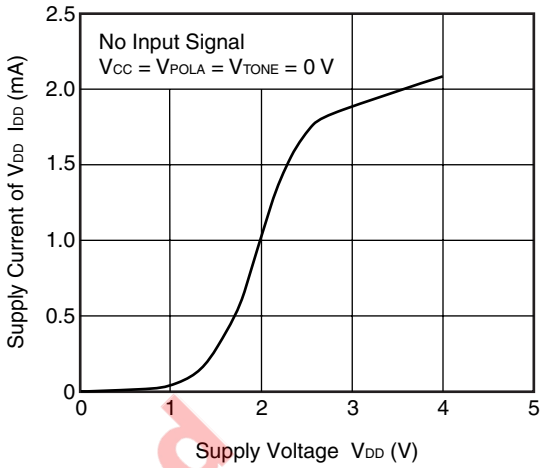
The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

TYPICAL CHARACTERISTICS
(T_A = +25°C, V_{DD} = V_{CC}1 = V_{CC}2 = +3.3 V, Z_S = Z_L = 50 Ω for each port, worst mode, unless otherwise specified)

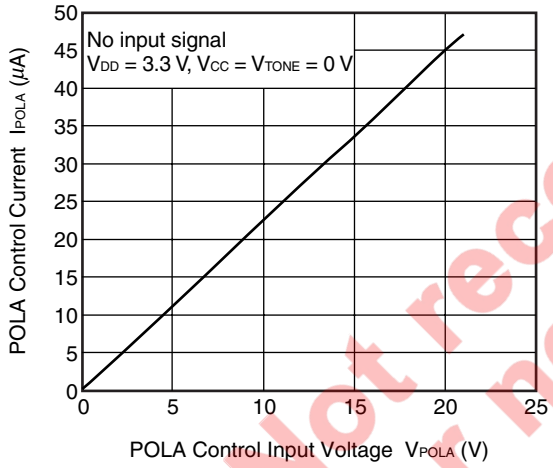
TOTAL SUPPLY CURRENT
vs. SUPPLY VOLTAGE (IF-Amplifier part)



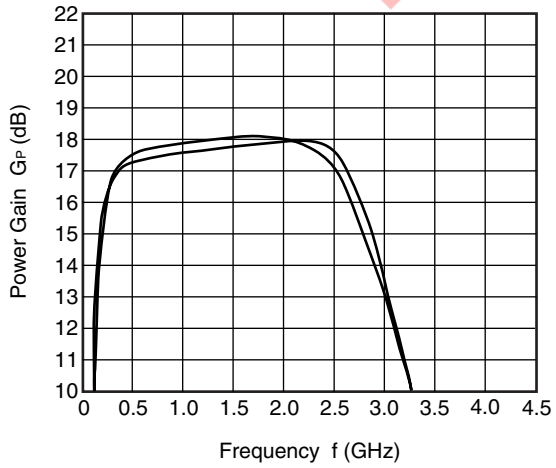
SUPPLY CURRENT OF V_{DD}
vs. SUPPLY VOLTAGE (Control part)



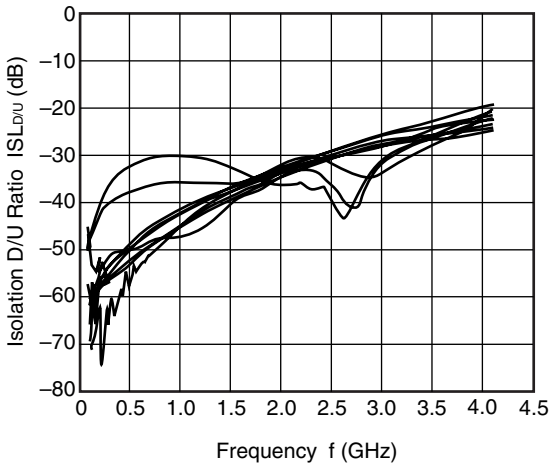
POLA CONTROL CURRENT vs.
POLA CONTROL INPUT VOLTAGE (Control part)



POWER GAIN vs. FREQUENCY

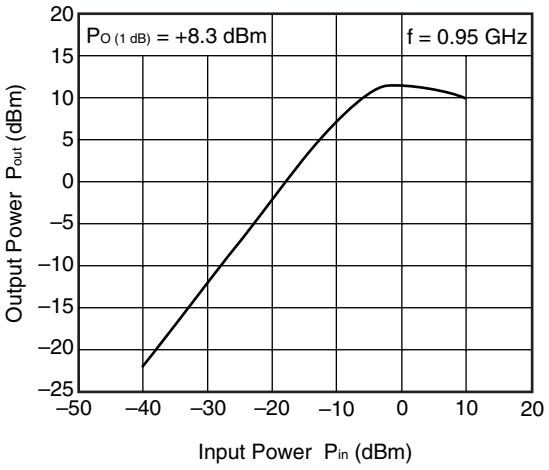


ISOLATION D/U RATIO vs. FREQUENCY

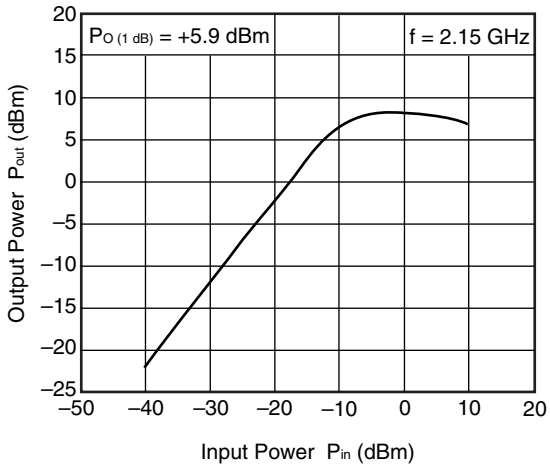


Remark The graphs indicate nominal characteristics.

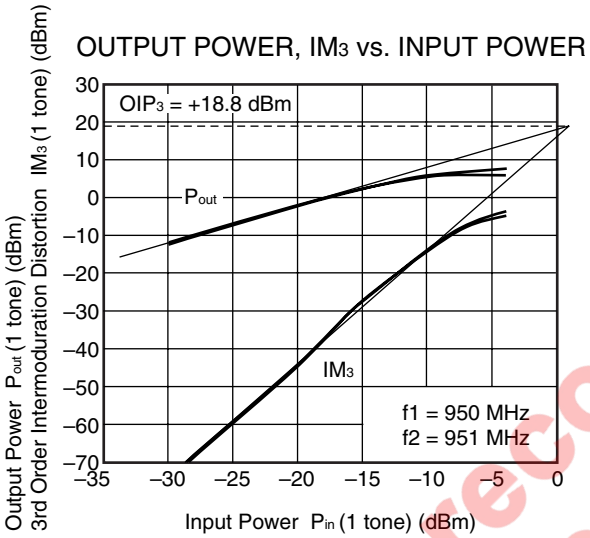
OUTPUT POWER vs. INPUT POWER



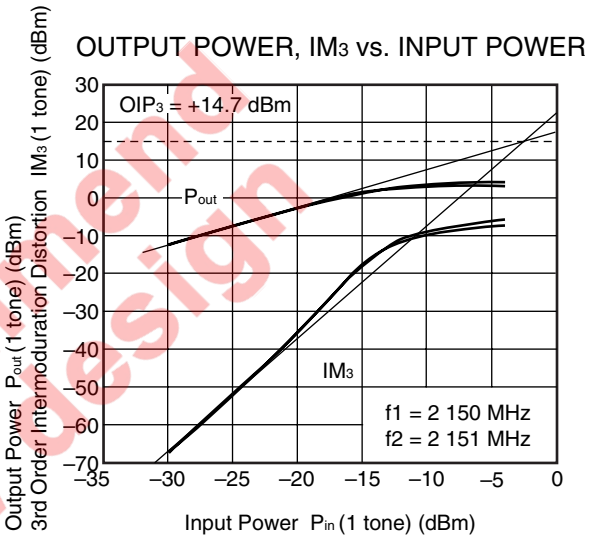
OUTPUT POWER vs. INPUT POWER



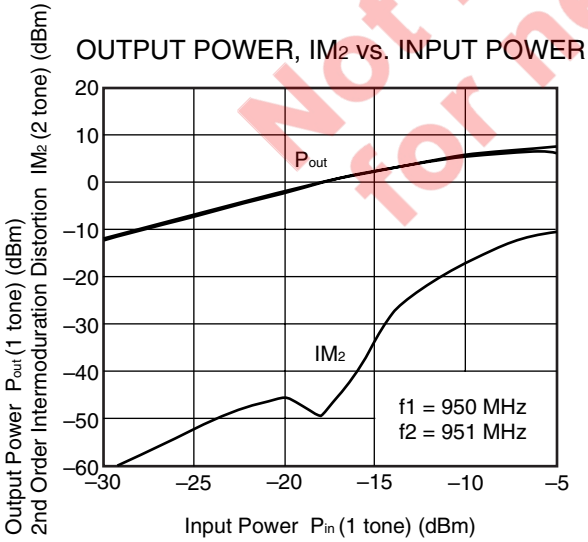
OUTPUT POWER, IM3 vs. INPUT POWER



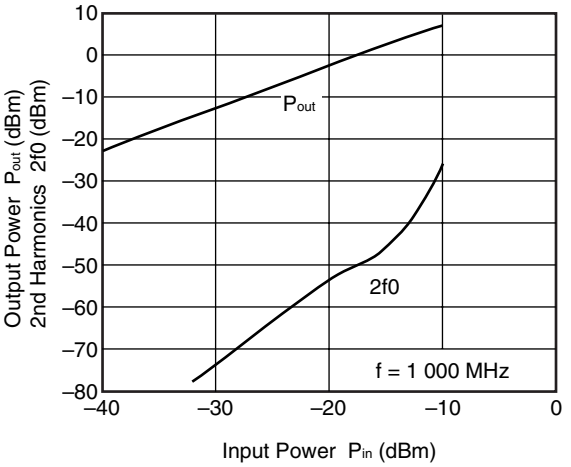
OUTPUT POWER, IM3 vs. INPUT POWER



OUTPUT POWER, IM2 vs. INPUT POWER

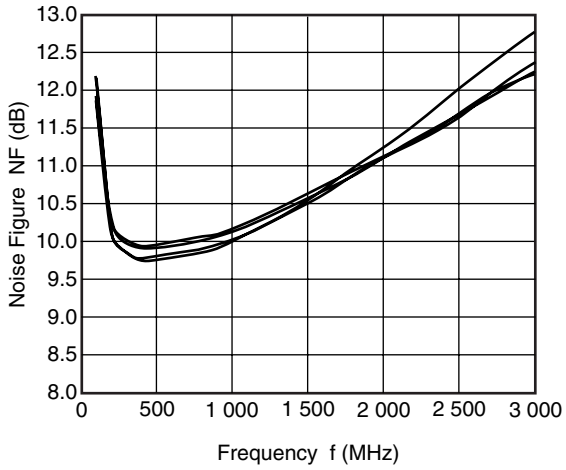


OUTPUT POWER, 2f0 vs. INPUT POWER

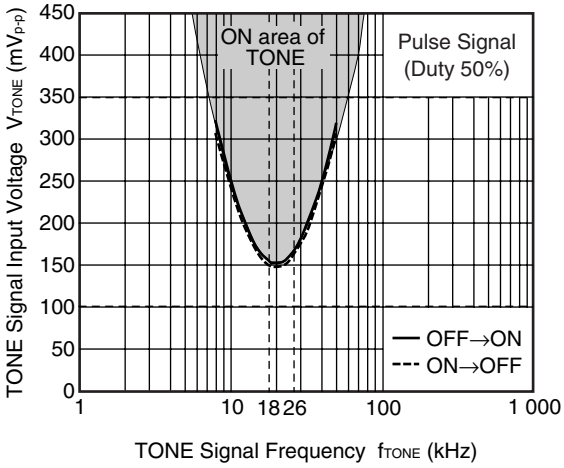


Remark The graphs indicate nominal characteristics.

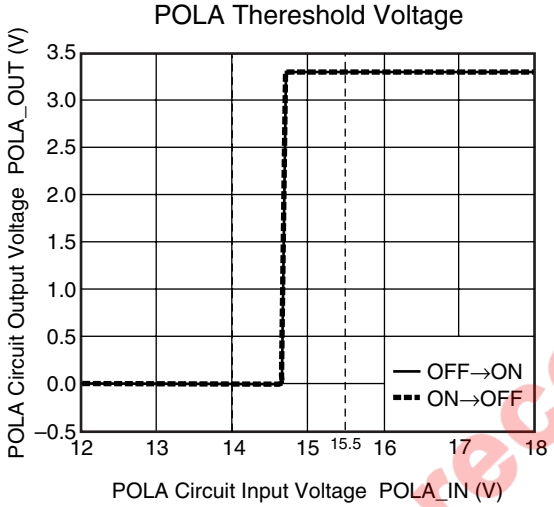
NOISE FIGURE vs. FREQUENCY



ON AREA OF TONE



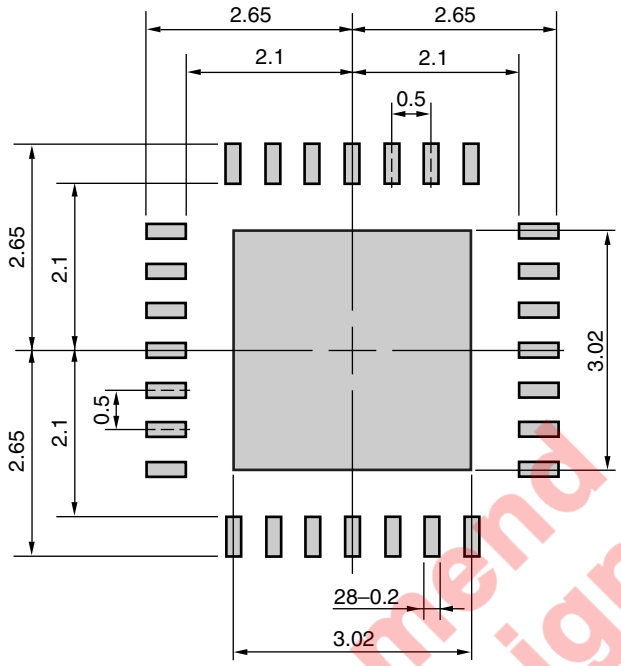
POLA Thereshold Voltage



Remark The graphs indicate nominal characteristics.

MOUNTING PAD LAYOUT DIMENSIONS

28-PIN 5 × 5 mm SQUARE MICRO LEAD PACKAGE (28-PIN PLASTIC QFN (0.5 mm pitch))
(UNIT: mm)



Remark The mounting pad layout in this document is for reference only.

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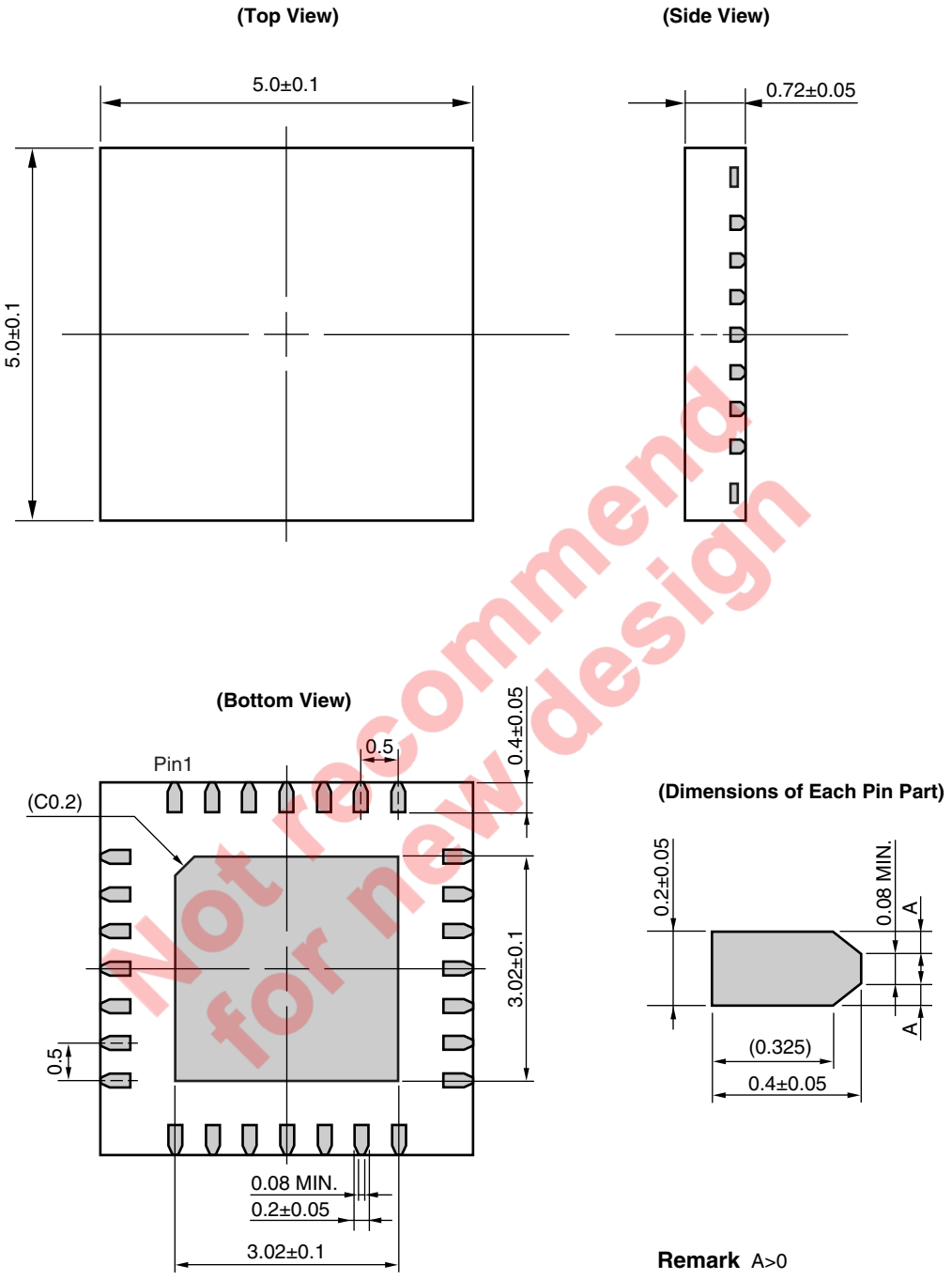
28-PIN 5 × 5 mm SQUARE MICRO LEAD PACKAGE (28-PIN PLASTIC QFN (0.5 mm pitch))
(UNIT: mm)



Remark A>0
( ) : Reference value

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
Partial Heating	Peak temperature (terminal temperature) : 350°C or below Soldering time (per side of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350

CAUTION

Do not use different soldering methods together (except for partial heating).

Revision History	μPD5754T7A Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec 22, 2010	–	First edition issued

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