Using the HI20201/03 Evaluation Kit

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Introduction

The HI20201 and HI20203 are 10-bit 160MHz and 8-bit 160MHz Digital to Analog Converters. These devices are ECL 10K and 100K logic compatible. These current out DACs are ideally suited for Signal Reconstruction and DDS (Direct Digital Synthesis) applications due to their inherent low noise design and low glitch area.

Architecture

The HI20201/03 DACs are designed with a split architecture to minimize glitch while maximizing linearity. Figure 1 shows the functional architecture of the device. The 6 least significant bits of the converter are derived by a traditional R2R network to binary weight the 1mA current sources. The upper 4, most significant bits are implemented as segmented or thermometer encoded current sources. The encoder converts the incoming 4 bits to 15 control lines to enable the most significant current sources. The thermometer encoder will convert binary to individual control lines.

As shown in Figure 2 the thermometer encoder translates the 4 bit binary input data into a decode that enables individual current sources. For example a binary code of 0110 on the data bits D6 thru D9 will enable current sources I1, I2, I3, I4, I5, and I6. The thermometer encoding architecture ensures good linearity without laser trimming. Also compared to an straight R/2R design the worst case glitch is greatly reduced since creating the MSB current is the sum of current sources I1 thru I8. This reduces the theoretical switching skew from current source to current source by using identically sized switches with identical gain, leakage and transient responses.

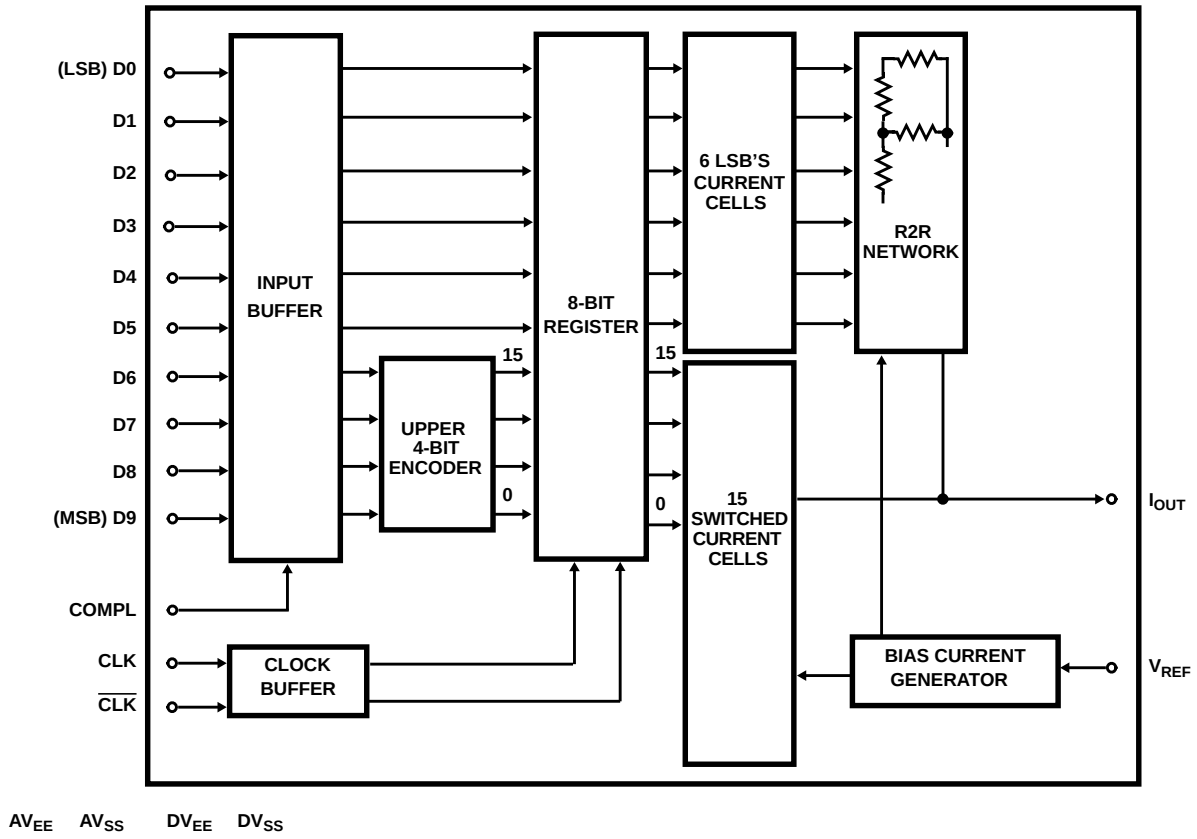


FIGURE 1. HI20201/03 FUNCTIONAL BLOCK DIAGRAM

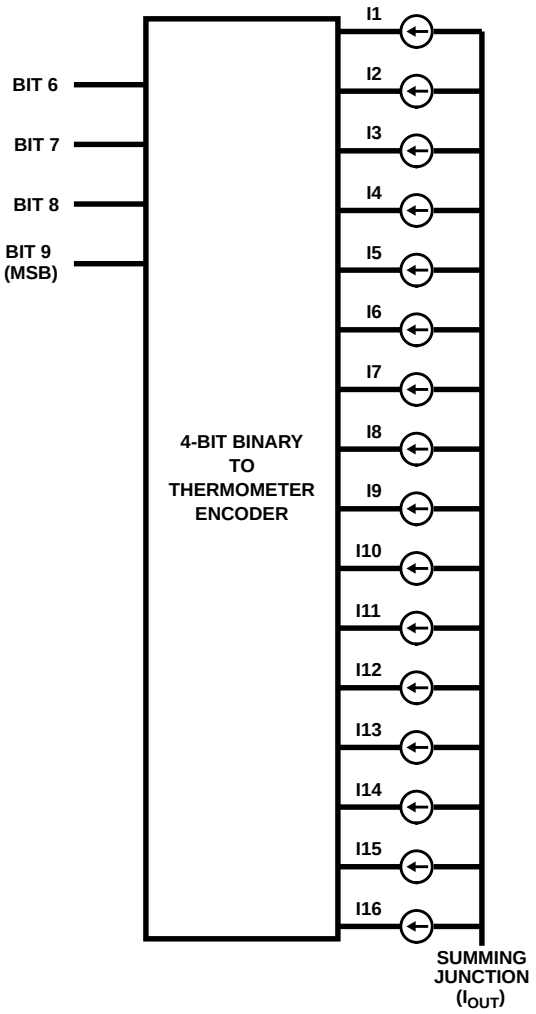


FIGURE 2. THERMOMETER ENCODER

Designing to Minimize Glitch

One cause of glitch is the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). In an ECL system where the logic levels switch from one non-saturated level to another, the switching times can be considered close to symmetrical. This helps to reduce glitch in the D/A. Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Intersil HI20201/03 employes an internal register, just prior to the current sources, that is updated on the clock edge. In traditional DACs the worst case glitch usually happens at the major transition i.e. 01 1111 1111 to 10 0000 0000. But in the HI20201/03 the worst case glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R2R/segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range.

Since the glitch is a transient event this leads designers to believe that a simple low pass filter can be used to eliminate or reduce the size of the glitch. In effect low pass filtering a glitch tends to “smear” the event and does little to remove the energy of the transient.

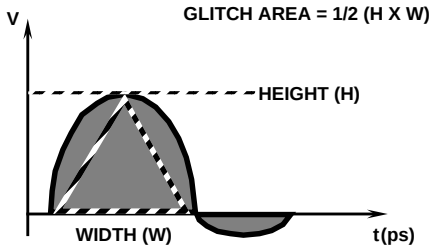
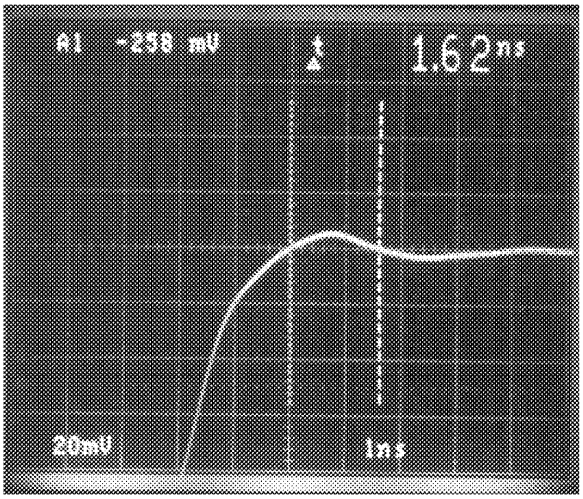


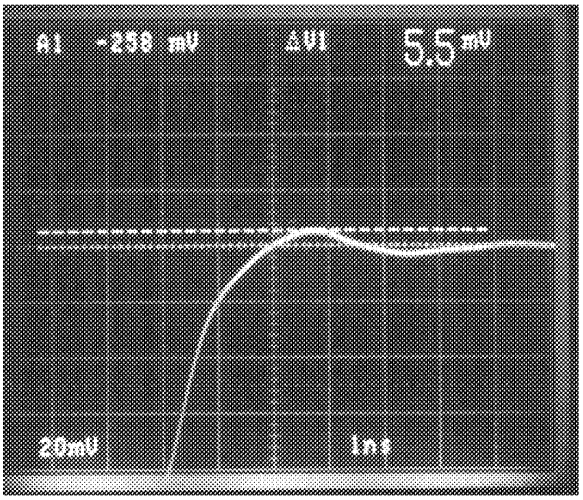
FIGURE 3. GLITCH AREA

Figure 4 and Figure 5 show a typical HI20201 glitch on a high speed Analog oscilloscope. The evaluation board from page 7 and page 8 was used, with the oscilloscope terminated 50Ω to ground.



G.A. = 1/2 (H x W)
= 1/2(5.5mV x 1.62ns)
= 4.4pV-Sec

FIGURE 4. GLITCH WIDTH



G.A. = 1/2 (H x W)
= 1/2(5.5mV x 1.62ns)
= 4.4pV-Sec

FIGURE 5. GLITCH HEIGHT

Integral Linearity

The HI20201 has a FSR range of 20mA. When driving an equivalent 75Ω load the full scale voltage swing is 0 to +1.5V. Most video and communication applications use a 1V pk-pk voltage swing which yields 13mA full scale current sink capability. With a 1V pk-pk voltage swing on the HI20201 output an LSB is

$$\text{LSB} = \text{Full Scale Range}/2^N$$

where N is the number of bits and the Full Scale Range is 1V.

The LSB size for this application is 977µV. To determine the Integral Linearity of the HI20201 the bit weights of each major transition is taken. Since the End Point method is used to calculate the overall INL the first measurements taken are Offset and then the Full Scale Voltage. Then the ideal LSB size for this given End Point line is used to calculate the INL error.

The worst case linearity of the HI20201 is specified to be less than 1 LSBs. The linearity of the HI20201 is worst in the segmented current sources in the thermometer encoded section. This is due to the errors of each current source being biased in one direction and being additive with increasing data values. The R/2R resistor matching needs be to a 6 bit level to ensure overall 10-bit linearity. Process control of resistor matching in the Bipolar process used is easily adequate to do the job. For the overall transfer function the typical INL performance is shown in Figure 6.

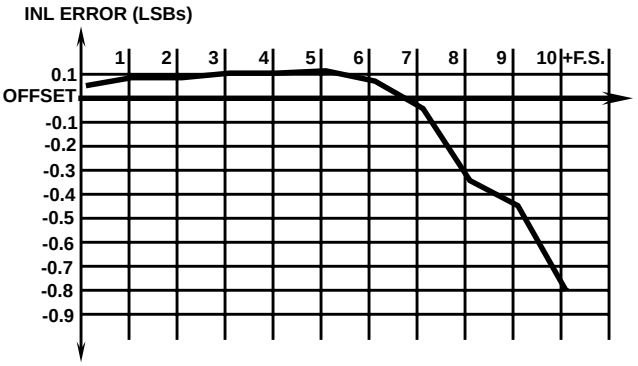


FIGURE 6. INL TYPICAL PERFORMANCE CURVE

Differential Linearity and Missing Codes

For a D/A Converter, the differential linearity is the step size difference throughout the entire code range. For the HI20201, the step to step maximum difference is 0.5 LSBs. For any given D/A converter, to guarantee no missing codes, the converter must be monotonic.

The definition of Monotonicity is that as the input code is increased the output should increase. When an input code is increased and the output of the DAC does not increase or reverses direction then this converter is assumed to be missing codes.

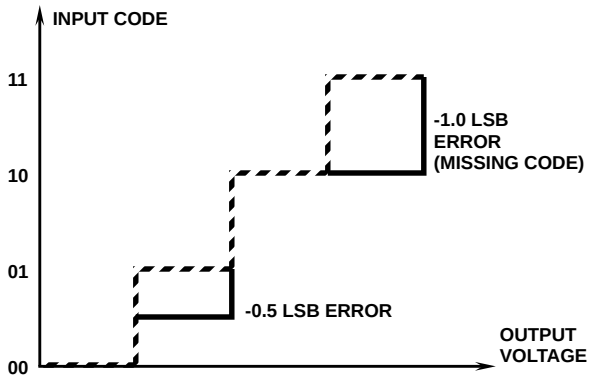


FIGURE 7. DNL EXAMPLE

As shown in Figure 7 as the input code increases the output voltage should increase. When an error of 1 LSB is incurred that bit can be assumed to be a missing code since the output did not increase, but, rather, remained the same.

Switching Noise

The HI20201/03 is an ECL compatible input device. Most systems today are TTL/CMOS where switching levels are typically 0 to +5V. (See Figure 8 for Logic Levels).

	TTL	CMOS	ECL (10K)
V_{IH} (Max/Min)	4.0V/2.0V	5.0/2.4	-0.81/-0.96
V_{IL} (Max/Min)	0.8V/0.0V	0.8V/0.0V	-1.65/-1.85
Noise Margin	1.2V	1.6V	0.125V
Rise/Fall Times	2.0ns	1.0ns	800ps
Maximum Clock Rates	~50MHz	~80MHz	~500MHz

FIGURE 8. LOGIC LEVEL COMPARISON

In an ECL system, logic signals must be properly terminated to ensure high speed operation. Typically a 50Ω resistor to a -2V supply is adequate. Board trace impedance should also have a characteristic Z_0 of 50Ω. In an ECL system, the logic swing runs a differential switching pair that operates in the linear region of the transistor or FET. The reduced logic swing and non-saturated logic makes an ECL converter have a lower noise floor due to the reduced clock and switching noise in the system.

The Evaluation Board

The HI20201/03 Evaluation board is a 1/2 size daughter board designed to interface to the HSP-EVAL board. The HSP-Eval is an Evaluation Platform for Intersil' Fast Function DSP ICs. These boards when used together create a flexible and powerful DDS system. The HSP45116 board is used to generate the high speed digital SINE wave patterns for the D/A module. The HI20201/03 board reconstructs the incoming digital data to an analog representation that can be analyzed on a spectrum analyzer or oscilloscope.

Plugging In

After opening the HSP45116 board and the HI20201/03 board, power should be applied to the banana jacks. A +5V, -5.2V and a -2.0V supply will be needed. To reduce noise the power supply leads should be twisted pairs.

The interface cable should be connected to an IBM PC or compatible parallel port. Power should be applied to the board and then the software can be started. The software can be run directly from floppy disk. To run the software place the floppy disk into drive A: and type:

A: NCOMCTRL

The HSP45116 Control Panel will be loaded. To exercise the board the following parameters should be set:

BINFMT# = 0

and then set the Center Frequency to:

CENTER FREQUENCY = 01000000_H

where the center frequency is in hex. At this point the output of the HI20201/03 DAC module should be converting a SINE wave at 48KHz. Connect the output of the HI20201/03 module to an oscilloscope. Adjust the potentiometer until the output waveform has an amplitude of $1V_{P-P}$. Adjusting the potentiometer Clockwise (CW) will reduce the amplitude and Counter-Clockwise (CCW) will increase the amplitude.

The HI20201/03 module has Jumper plug for selecting the complement feature of the HI20201. When J2 is installed, the DAC will invert the incoming data. When J3 is installed, the DAC will not invert the data.

The HI20201/03 is very sensitive to clock noise. Some TTL/CMOS oscillators have tremendous amounts of ringing and overshoot. To reduce this, R7 can be installed. A 50Ω resistor is recommended.

DDS Interface

The HSP45116 board is a TTL/CMOS compatible logic board. The HI20201/03 D/A is an ECL compatible logic converter. MC10H124's are use to convert the TTL/CMOS output of the Numerically Controlled Oscillator (NCO) to ECL logic inputs. The HI20201/03 also requires a complementary clock input which is also done in the MC10H124s. The design of the DAC module is to interface to the 10 Most Significant Bits (MSB's) of the NCO.

Spurious Free Dynamic Range

The Spurious Free Dynamic Range of the HI20201/03 DACs is the most important specification for communication applications. This specification shows how Integral Linearity, Glitch, and Switching noise affect the spectral purity of the output signal. Several important items must be noted first.

When a quantized signal is reconstructed, certain artifacts are created. Let's take the example of trying to recreate a 1MHz Sine wave with a $1V_{P-P}$ output. In the frequency domain, the fundamental should appear at 1MHz as shown in Figure 9.

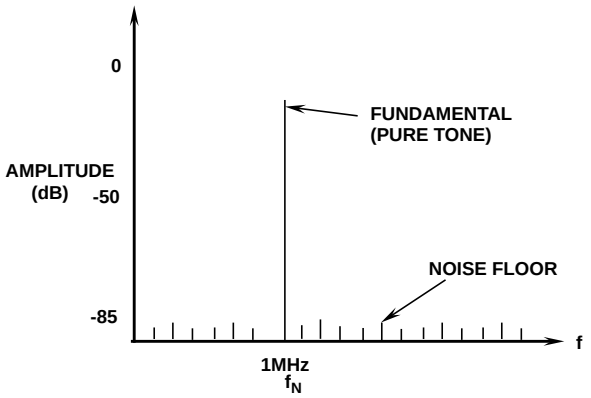


FIGURE 9. FREQUENCY PLOT OF 1MHZ TONE

The fundamental of a pure 1MHz tone should appear as an impulse in the frequency domain at 1MHz. In a sampled system noise terms are produced near the sampling frequencies called aliases. These aliases are related to the fundamental in that they are located f_N around the sampling frequency as shown in Figure 10.

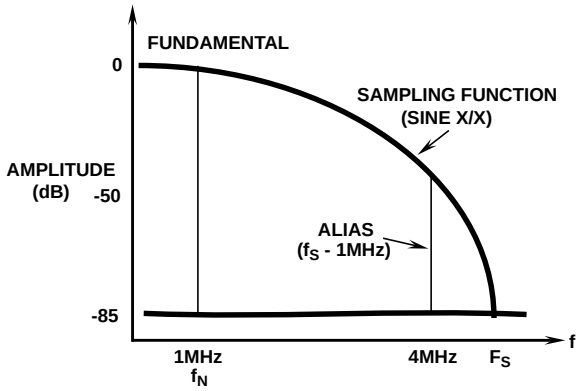


FIGURE 10. SAMPLING ALIAS PRODUCTS

So for a 1MHz fundamental and a 5MHz sampling rate an alias term is created at 4MHz. A SYNC2 function shaping is also induced by sampling a signal. Aliases continue up through the frequency spectrum repeating around the sampling frequency and its harmonics (i.e. $2f_S$, $3f_S$, $4f_S$...).

A reconstructed Sine wave out of the HI20201/03 is not ideal and as such, has harmonics of the fundamental. The difference between the magnitude of the fundamental and the highest noise spur, whether it is harmonically related to the fundamental or not, is the definition of Spurious Free Dynamic Range. Figure 11, Figure 12, Figure 13, and Figure 14 are sample plots taken from the HI20201 at various frequencies. Included are the oscilloscope plots.

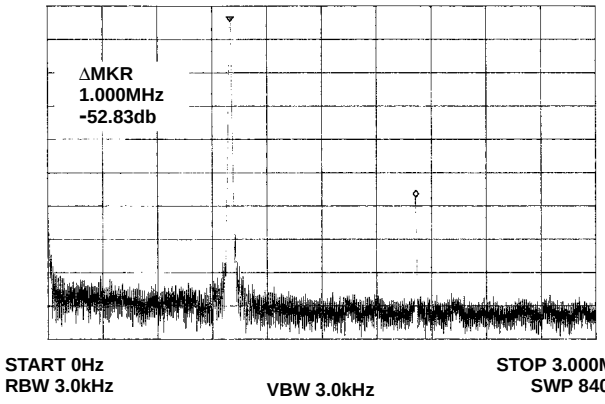


FIGURE 11A. SAMPLE PLOT

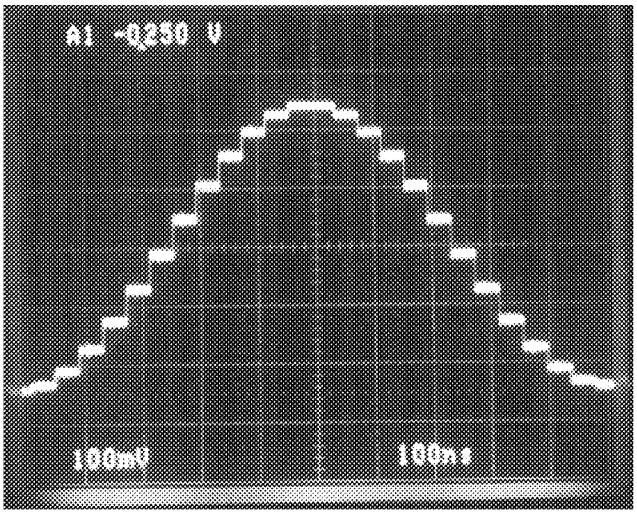


FIGURE 11B. OSCILLOSCOPE PLOT

FIGURE 11.

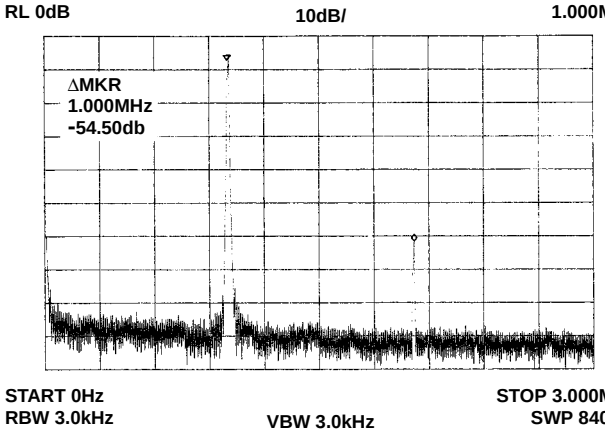


FIGURE 12A. SAMPLE PLOT

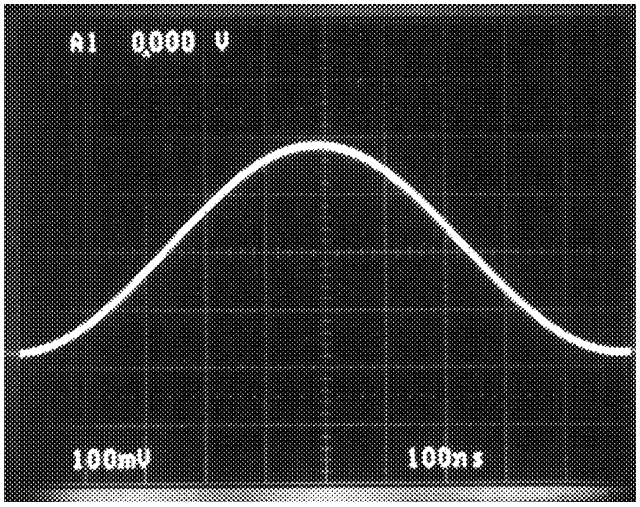


FIGURE 12B. OSCILLOSCOPE PLOT

FIGURE 12.

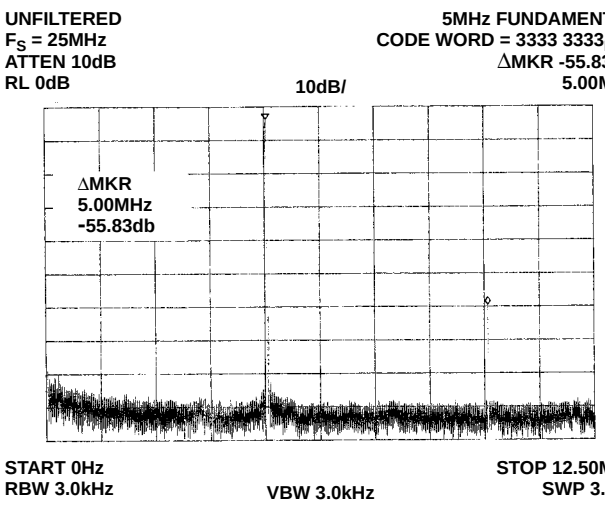


FIGURE 13A. SAMPLE PLOT

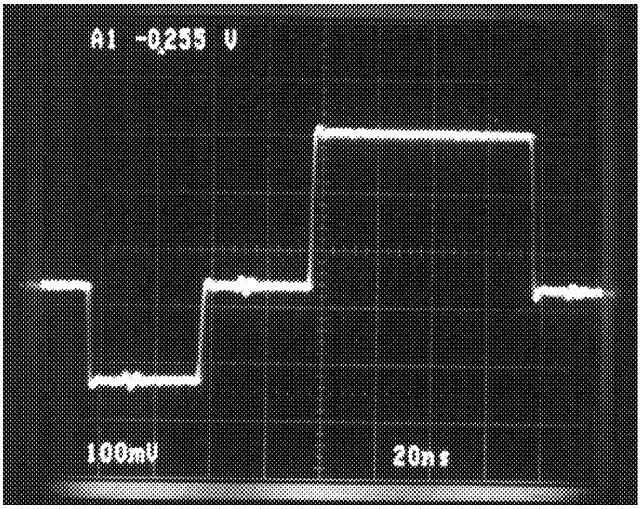


FIGURE 13B. OSCILLOSCOPE PLOT

FIGURE 13.

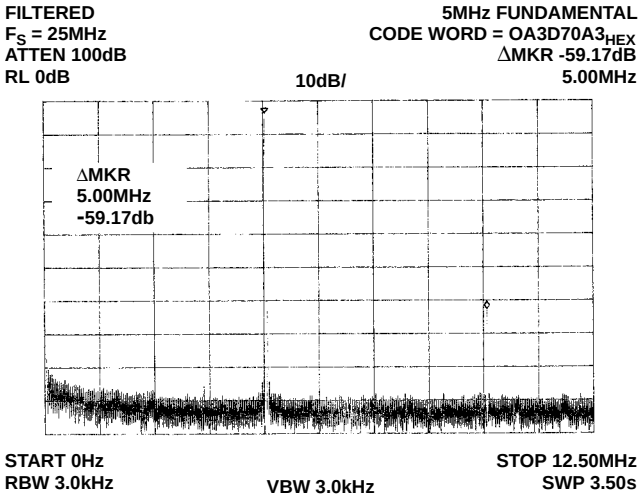


FIGURE 14A. SAMPLE PLOT

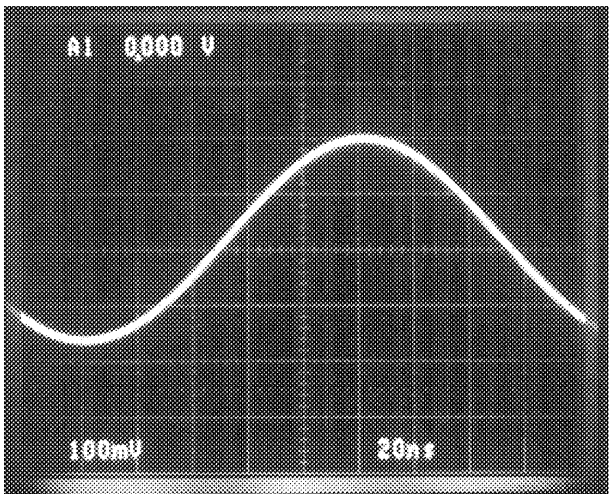


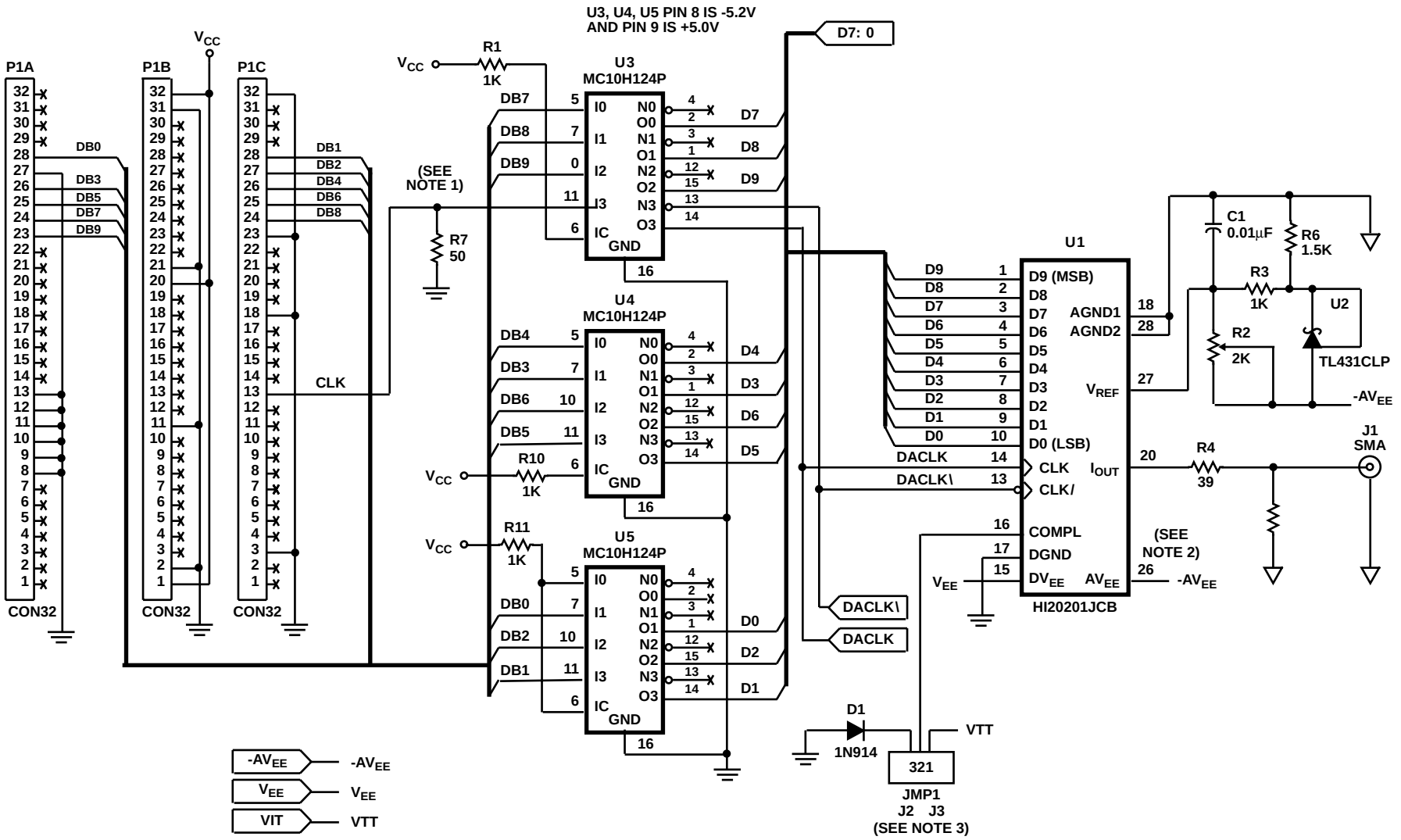
FIGURE 14B. OSCILLOSCOPE PLOT

FIGURE 14.

Schematic Materials List

NUMBER	DESCRIPTION	PART NUMBER	VENDOR	QUANITY	REFERENCE (DES)
1	96 Pin Female DIN	A1262-ND	Digi-Key	1	J1
2	3 Post Jumper Thru-Hole	518-1072	Allied	1	J2, 3
3	Banana Jacks	J147-ND	Digi-Key	4	BJ1, 2, 3, 4
4	Pin Sockets	2-220808-7	Amp	28	U1
5	Female SMA Connector	PE4117	Pasternack	1	J4
6	1KΩ Res. Thru-Hole	297-4356	Allied	4	R1, 3, 10, 11
7	1.5KΩ Res. Thru-Hole	297-4380	Allied	1	R6
8	39Ω Res. Thru-Hole	297-5140	Allied	1	R4
9	100Ω Res. Thru-Hole	297-4202	Allied	1	R5
10	2KΩ Pot Thru-Hole	754-3122	Allied	1	R2
11	8 Pin Resistor SIP 50Ω	4600X-101-510	Bourns	2	RN1, 2
11	10µH Ind. Thru-Hole	274300111	Dexter	4	L1, 2, 3, 4
10	0.1µF Cap CER Thru-Hole	CK05BX104K	Allied	11	C3, 5, 12, 13, 15, 16, 17, 18, 20, 21, 22
11	0.01µF Cap CER Thru-Hole	CK05BX103K	Allied	7	C1, 4, 6, 7, 8, 9, 10
12	10µF TANT Cap Thru-Hole	10µF TANT	Allied	5	C2, 11, 14, 19, 23
13	Shottky Diode	IN914	HP	1	D1
14	HI20201 D/A DIP Package	HI20201HIP	Intersil	1	U1
15	Quad TTL to ECL Drivers Dip	MC10H124P	Motorola	3	U3, 4, 5
16	+2.5V Reference TO-92	TL431CP	TI	1	U2
17	HI20201 Evaluation Board	HI20201.EVAL	Intersil	1	

Schematic Diagram (Part 1 of 2)



NOTES:

1. User installs 50Ω resistor for TTL clock termination if needed.
2. Connect pins 19, 21, 22, 23, 24 and 25 to analog ground.
3. Insert J2 to enable data complement, insert J3 to enable normal data.

FIGURE 15.

Schematic Diagram (Part 2 of 2)

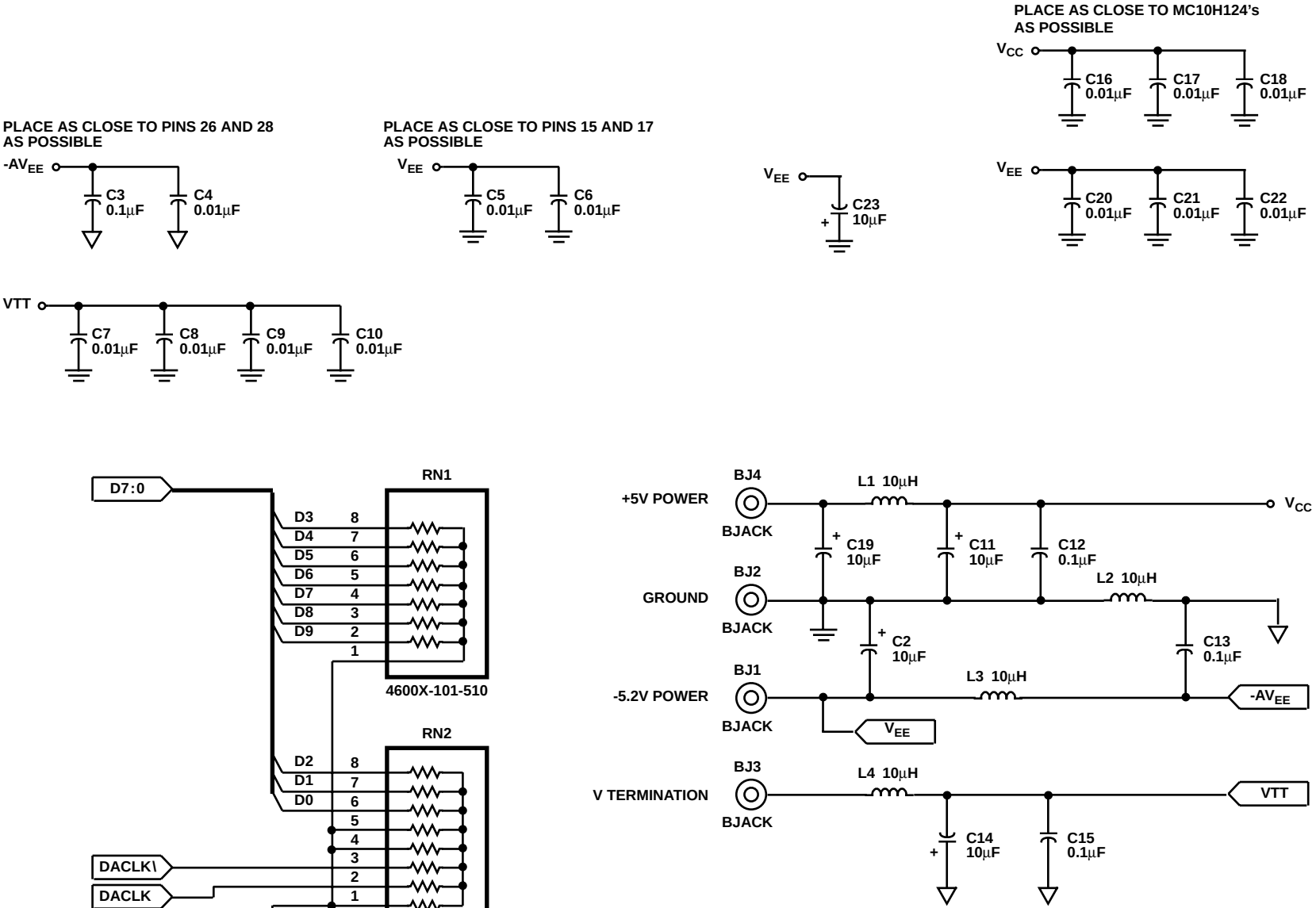


FIGURE 15. (Continued)

Evaluation Board Layers

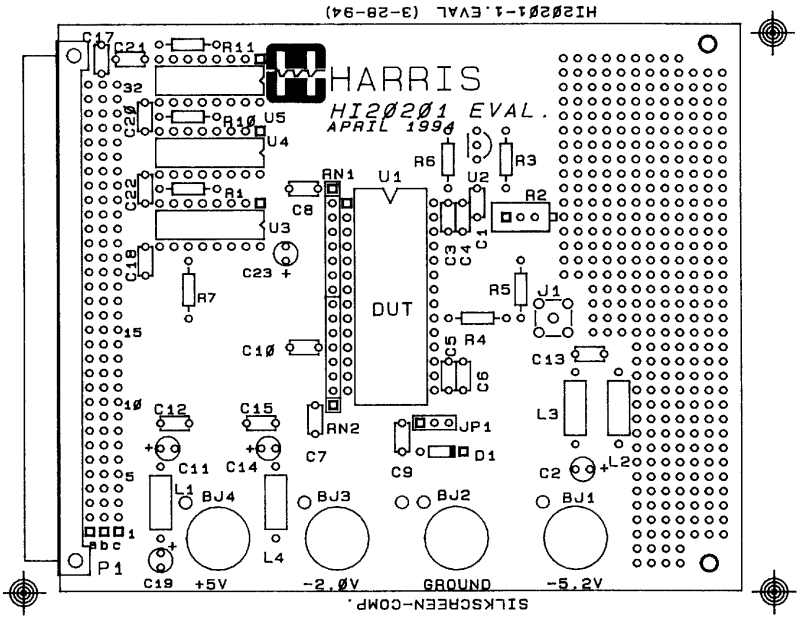


FIGURE 16A. HI20201 SILKSCREEN

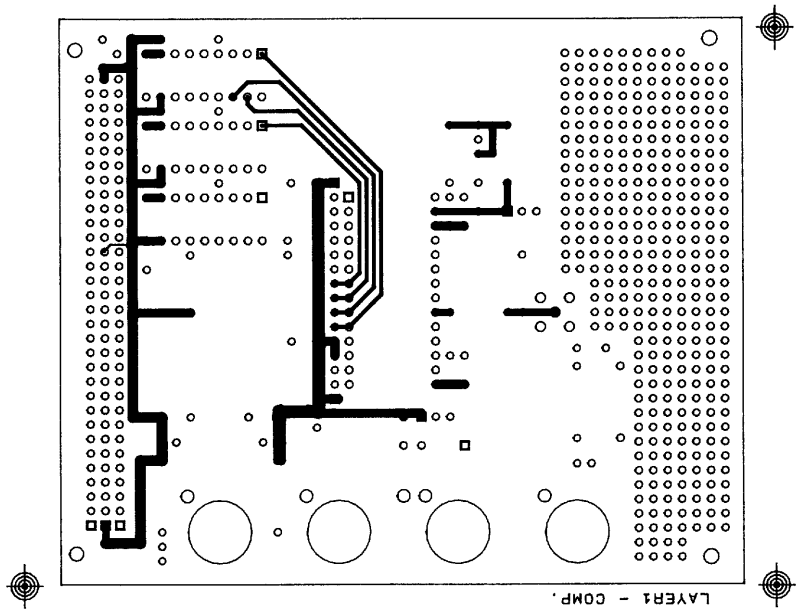


FIGURE 16B. HI20201 LAYER 1

Evaluation Board Layers (Continued)

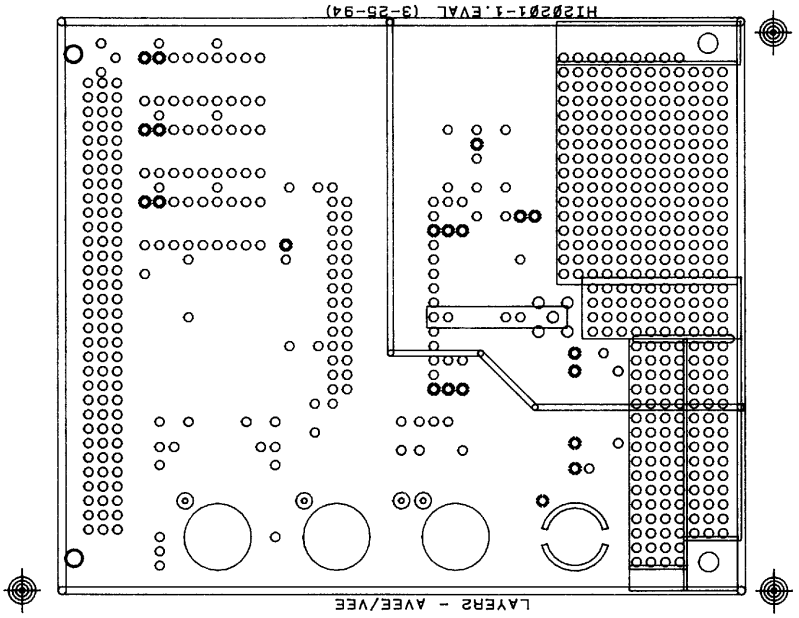


FIGURE 16C. HI20201 LAYER 2

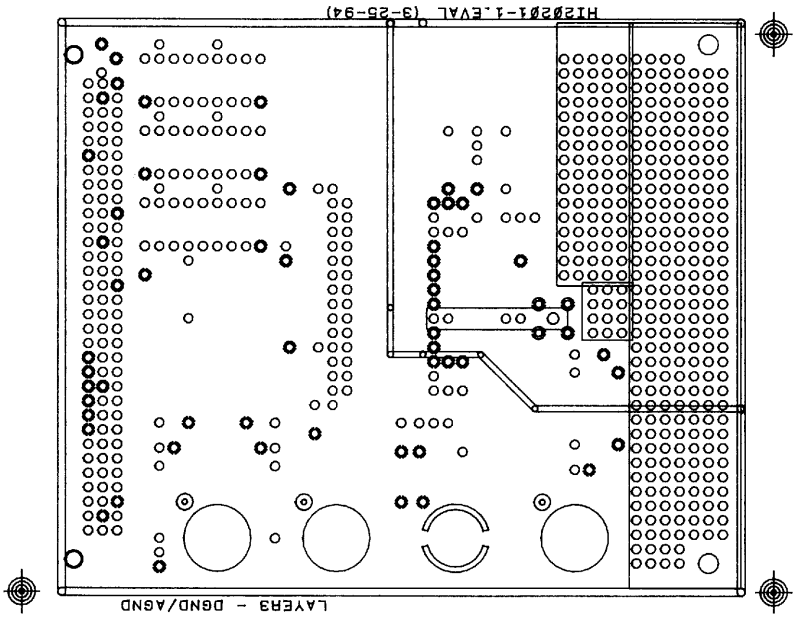


FIGURE 16D. HI20201 LAYER 3

Evaluation Board Layers (Continued)

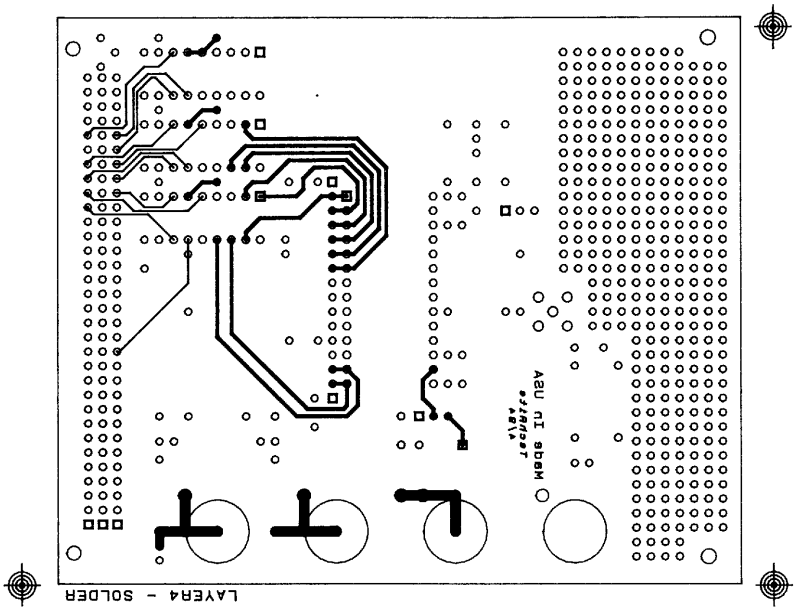


FIGURE 16E. HI20201 LAYER 4