An ACPI Controller for ICH2-Based Computer Systems (HIP6503EVAL1)

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Introduction

The Advanced Configuration and Power Interface specification (ACPI; [1]), written by a consortium representing Intel, Microsoft and Toshiba, attempts to evolve the current collection of power management methods and configuration interfaces into a well-specified and unified power management and configuration mechanism. The key objective in the ACPI specification is to transfer all control of power management and configuration functions to the operating system, thus enabling Operating System Directed Power Management (OSPM). ACPI-compliant systems will benefit from a robust interface for configuring motherboard devices, a versatile power management interface enabling a wide variety of solutions with full operating-system support, and not lastly, a realm of new, intelligent possibilities added to the already broad span of PC uses.

The HIP6503 IC was designed to be used in conjunction with a second integrated circuit to provide a complete ACPI-sanctioned motherboard power regulation solution for an ICH2-based computer system. The HIP6503/HIP6020 or HIP6503/HIP6021 chip sets produce the processor core, GTL bus, memory controller hub, and AGP bus voltages, as well as the 3.3V dual/standby, 1.8V standby, 2.5V clock, 2.5V or 3.3V SDRAM/RDRAM memory, and 5V dual plane necessary for a complete PIII-ICH2 (Camino 2, Solano 2, or equivalent) system implementation [2, 3, 5]. Regardless, the HIP6503 can also be used in differently power partitioned systems.

From a hardware perspective, and mentioned accordingly in this document, the ACPI functionality of a circuit can be simplified down to 3 major modes of operation:

- ‘S0’ or active state (in effect either S0, S1, or S2)

- ‘S3’ sleep state (suspend-to-RAM)

- ‘S5’ sleep state (in effect either S4 or S5; suspend-to-disk or soft-off)

Brief familiarity with the ACPI initiative and supporting documentation is needed to properly assimilate the content of this document.

Quick Start Evaluation

Important!

Given the specialized nature of the HIP6503, the HIP6503EVAL1 board is meant to be evaluated only with an ATX power supply. Furthermore, only an ACPI-ready ATX supply can be used to power-up the evaluation boards (720mA minimum capability on 5VSB output; ATX Specification v2.02, [4]). Standard laboratory power supplies are not suitable for powering up this evaluation board.

Circuit Setup

‰ **Set Up JP1, JP2, and JP2, JP3**

Before connecting the input ATX supply to the HIP6503EVAL1 board, consult the circuit schematic and data sheet and set the JP2 configuration jumper on the HIP6503EVAL1 according to the configuration you wish to emulate. This particular configuration is latched-in during certain times, but can be subsequently changed at certain times. See HIP6503 data sheet for information on the available configurations and how to set them.

‰ **Connect the Input Power Supply**

Ensuring that the supply is not plugged into the mains, or that the AC switch is off (if provided), connect the main ATX output connector to J1.

‰ **Connect the Output Loads**

Connect typical standby loads to all the evaluation board’s outputs. Consult Table 1 for maximum loads supported by the design of the HIP6503EVAL1 in the configuration received; consult the ‘HIP6503EVAL1 Modifications’ chapter for information on modifying the evaluation board to meet your special needs.

‰ **Set Start-Up State (Active Is Recommended)**

If start-up in active state (S0) is desired, ensure both ‘S3’ (SW2) and ‘S5’ (SW3) switches are in the off position (away from ‘S3’ or ‘S5’ marking). Ensure the ‘ATX ON’ switch is also in the off position.

Set either the ‘S3’ or the ‘S5’ standby switch for start-up in either of the standby states. IMPORTANT: only one switch needs to be actuated, so select the standby state by turning on the switch with that name - the signal conditioning circuitry ensures correct $\overline{S3}$ and $\overline{S5}$ pin stimulation.

Operation

‰ **Provide Bias Voltage to the Board**

Plug the ATX supply into the mains. If the supply has an AC switch, turn it on. The ‘5VSB’ (LP4) LED should light up, indicating the presence of 5V standby voltage on board.

‰ **Examine Start-Up Waveforms**

Sleep state start-up is immediate following application of bias voltage. Using an oscilloscope or other laboratory equipment, you may study the ramp-up and/or regulation of the controlled voltages, according to the specific JP2 configuration previously set and the specific standby state selected.

For start-up into an active state (standby switches set off prior to application of bias voltage), flip on the ‘ATX ON’ switch (SW1). This will turn on the main ATX outputs and the

HIP6503 will start up into active state. Once turned on, SW1 needs not be turned off until bias is removed from the board.

‰ **Examine Output Quality Under Varying Loads**

In either state (sleep or active) vary the output loads to simulate computer loads typical of the specific operating state the circuit is in.

‰ **Examine State Transitions**

For subsequent transitions into standby states, leave the main ATX outputs enabled (SW1 on); the circuit will automatically turn them off when entering a standby state. To enter a standby state, turn on the respective switch. The ‘S3’ LED will light up to indicate S3 standby state, while S5 state will illuminate both ‘S3’ and ‘S5’ LEDs. However, the HIP6503 will ignore any illegal transition requests, such as from S3 state to S5 state or vice versa, as shown in Figure 1.

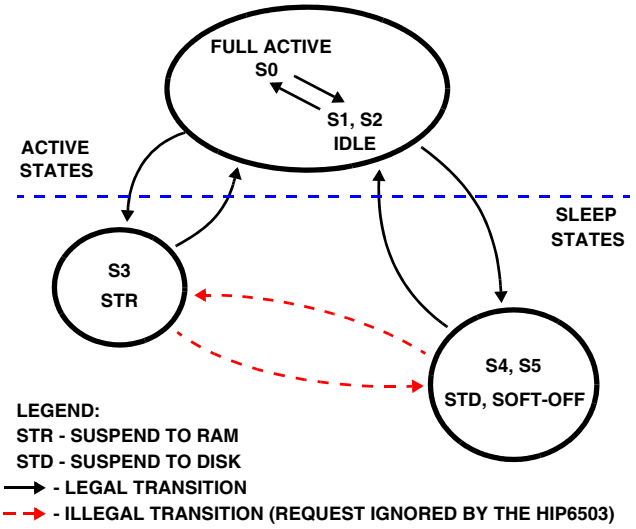


FIGURE 1. HIP6503 LEGAL/ILLEGAL STATE TRANSITIONS

Fault Handling

In case of a fault condition (output under-voltage), the FAULT pin asserts a logic ‘high’, shutting down the ATX supply’s main outputs through the on-board latch circuit. To recover from such a shutdown, press the ‘SHUTDOWN/CLEAR FAULT’ button (PB1). Depressing PB1 will reset the IC and initiate a soft-start sequence, thus clearing the FAULT latch, and enabling the main ATX outputs.

If jumper JP1 “FAULT LATCH” is removed, the FAULT output will not latch the circuit. The circuit may appear to latch off because the FAULT signal shuts down the ATX supply, cutting off the input supply to the faulting output, and thus keeping it from ever recovering from the fault condition. ***However, it is not recommended to test the circuit against output under-voltages (output short-circuits) with the fault latch jumper removed***. Due to the very slow response of the ATX supply in response to a shutdown request, the external N/P-MOS switches (Q4, Q5, and Q6) in use at the time of testing could fail as a result of sustained over-current through the drain-source channel and bond wires. The FAULT latch circuit acts on the SS pin directly, shutting down the IC quickly. To protect the external switches it is strongly recommended that JP1 ‘FAULT LATCH’ jumper is shunted throughout the operation of the evaluation board.

Configuring Sleep State Support

Sleep state support on the $5V_{DUAL}$ output of the HIP6503EVAL1 is user-configurable through jumper JP2. The configuration can be changed prior to 5VSB application, during active state operation, as well as during chip shutdown (PB1 pressed). During all other times, the configuration is internally latched and any changes in the EN5VDL pin’s logic status is ignored.

HIP6503EVAL1 Reference Design

General

The evaluation design is implemented on 2-ounce, 4-layer, printed circuit board (see last three pages of this application note for layout plots). Most of the components specific to the evaluation board alone, which are not needed in a real computer application, are placed on the bottom side of the board. ***Assuming the input supplies and the controlled output planes have their own on-board filtering (capacitors), the only components required to implement this ACPI 5-voltage controller/regulator solution are contained within the white rectangle surrounding the HIP6503 on the top side of the board***. All the additional circuitry contained on board has the role of duplicating the computer environment the chip would operate in. Since this additional circuitry would clutter and detract from the readability of the schematic, most of it was grouped in two blocks, named ‘SIGNAL CONDITIONING’ and ‘FAULT LATCH’ (see evaluation board schematics).

The board also contains a serpentine resistor which occupies about 1/3 of both top and bottom sides of the board. The ATX supply requires some minimum loading on the +5V output in order to stay active; lack of this minimum loading causes the ATX to shut down all its outputs, except +5VSB. This minimum load is specified as 1A, but most supplies will stay active with as little as 400-500mA. The embedded resistor is designed to draw a current of about 1A (typical). If the current draw is insufficient to keep the power supply active, try reducing the value of the embedded resistor. Shorting out the W1 footprint, on the back side of the board, effectively shorts out 1/4 of the resistive trace, increasing the current draw by 30%. Similarly, shorting out W2 reduces the trace by 50%, thus doubling the current draw from the +5V output. If either W1 or W2 are shorted, it is advised that active state operation time be reduced as to avoid severe overheating of the board (in case the 5V

current draw exceeds 1A). For most, if not all cases, neither W1 nor W2 need be shorted.

Design Envelope

Although different computer systems might have different requirements, the HIP6503EVAL1 board was designed to meet the maximum output loading described in Tables 1. Note the fact that the addition of all the sleep state output currents exceeds the typical ATX power supply 5VSB output capability (725mA). Real-life sleep state current requirement on each of the outputs could be lower, and their maximums should rarely all occur simultaneously. Output tolerances and current ratings (with the exception of the $2.5V_{CLK}$, $1.8V_{SB}$, and $3.3V_{DUAL}/3.3V_{SB}$, $2.5/3.3V_{MEM}$ when operating on internal pass transistors) can be adjusted by properly selecting the components external to the HIP6503.

TABLE 1. HIP6503EVAL1 MAXIMUM OUTPUT LOADING

OUTPUT VOLTAGE	ACTIVE STATES		SLEEP STATES		TOL. (STATIC/ DYNAMIC)
	I_{OUT}	dI_{OUT}/dt	I_{OUT}	dI_{OUT}/dt	
$2.5V_{CLK}$	500mA	0.1A/µs	0	0	5%/5%
$2.5/3.3V_{MEM}$	4A	1A/µs	200mA (Note)	1A/µs (Note)	5%/9%
$1.8V_{SB}$	150mA	0.1A/µs	50mA	0.1A/µs	5%/5%
$3.3V_{DUAL}$/ $3.3V_{SB}$	3A	0.2A/µs	600mA	0.2A/µs	9%/9%
$5V_{DUAL}$	2.5A	0.1A/µs	200mA	0.1A/µs	9%/9%

NOTE: S3 State Only.

The maximum current supported on the $2.5V_{MEM}$ output (systems employing RDRAM memory) is as high as 7-8A. To be safe from a thermal performance perspective, do not operate the evaluation board for extended periods of time at output current levels exceeding the design envelope, as detailed in Table 1.

HIP6503EVAL1 Performance

Figures 2 through 6 depict the evaluation board's performance during a few typical operational situations. To simulate minimum loading conditions, unless otherwise specified, the outputs were loaded with 65Ω resistive loads.

Sleep-State Start-Up

Figure 2 shows a typical HIP6503EVAL1 start-up into S3 sleep state with the $5V_{DUAL}$ output enabled (EN5VDL = 1). As 5VSB is applied to the board, SW1 and SW3 are off, while SW2 is on. At time T0 the input supply exceeds the power-on-reset (POR) threshold. Approximately three milliseconds afterwards, at time T1, the soft-start clamp is removed, the $1.8V_{SB}$ and $3.3V_{DUAL/SB}$ outputs starting to ramp up toward their target values, which they reach at time T2. As its ramping ends shortly after bringing up these two outputs, the soft-start voltage is quickly brought down and prepared for a second soft-start designed to bring up the remainder of the controlled voltages that are supported in this configuration and state. This second ramp-up begins at time T3 and ends at time T4. The $5V_{DUAL}$ output has a slightly different ramp-up than the remainder of the output voltages. The $5V_{DUAL}$ output is not actively regulated, as is the case with the $2.5V_{MEM}$, $1.8V_{SB}$ and $3.3V_{DUAL/SB}$ (in S3) outputs, but rather switched on through a P-MOS or PNP switch. An error amplifier is thus provided for the $5V_{DUAL}$ output just for the purpose of providing a smooth, controlled output voltage rise. This error amplifier uses a different, soft-start derived ramp signal to achieve the controlled rise of the output.

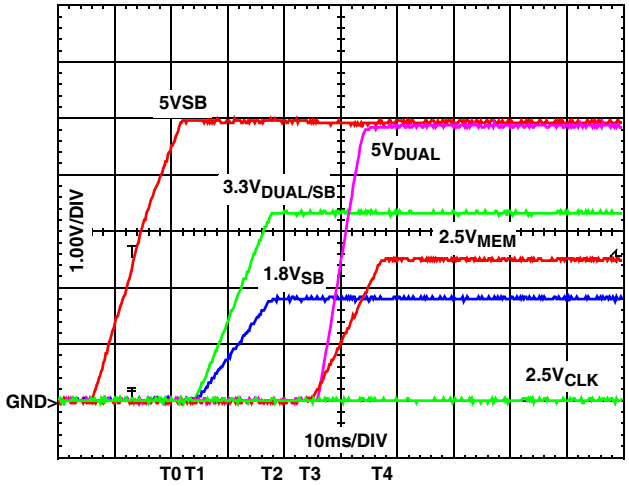


FIGURE 2. HIP6503EVAL1 START-UP IN SLEEP STATE (S3) WITH ALL OUTPUTS ENABLED

Active-State Start-Up

Figure 3 also shows a start-up sequence, but this time into an active state (S0, S1). As the enable pin only configures the sleep state $5V_{DUAL}$ support, this start-up sequence will be the same, regardless of EN5VDL status. In Figure 3, SW1, SW2 and SW3 are all off and 5VSB is applied to the HIP6503EVAL1 board. Active state operation is enabled by switching on SW1, a few milliseconds before T0. Invariably, the $3.3V_{DUAL/SB}$ and $1.8V_{SB}$ outputs are brought up shortly after 5VSB is applied to the IC, and they can be seen present at the time the main ATX outputs are coming up (T0). At time T0, the input voltages (3.3V, 5V, 12V) exceed the under-voltage thresholds (12V shown, only) and the internal 25ms (typical) timer is initiated. Note the typically poor regulation of the ATX supply resulting in a start-up overshoot. During start-up, the $5V_{DUAL}$ output undergoes a quasi soft-start, due to conduction through the body diode of the active N-MOS switch (Q6). At time T1, the timer expires and the two active-state N-MOS transistors (Q4 and Q6) are turned on; simultaneously, the $2.5V_{MEM}$ and $2.5V_{CLK}$ outputs begin a soft-start cycle, reaching regulation limits at time T2.

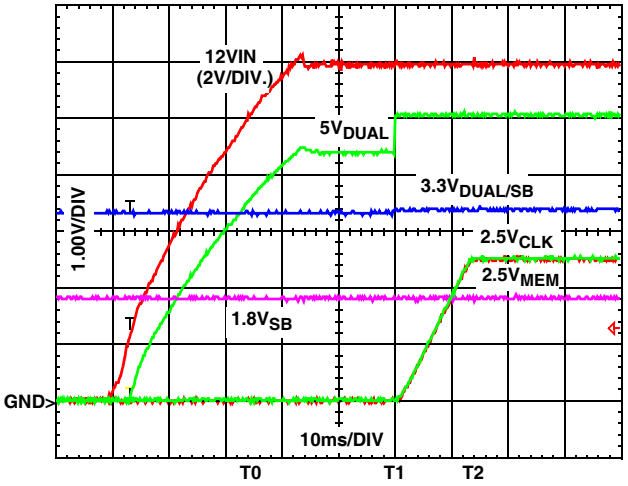


FIGURE 3. HIP6503/EVAL1 START-UP IN ACTIVE STATE (S0, S1) WITH ALL OUTPUTS ENABLED

State Transitions

Figure 4 shows the transition from active state (S0, S1) to S3 sleep state on the HIP6503EVAL1 board. Prior to time T0, the evaluation board was operating in active mode, with SW1 on and SW2 and SW3 off. At time T0, SW2 is switched on, triggering the turn-off of the ATX and the switch-over of the output regulation from the active ATX output rails to the 5VSB supply. Very shortly after time T0, the ATX responds to the turn-off request, and the 5V input starts to ramp down under the current drawn by the embedded 5Ω serpentine resistor. As it can be noticed in the scope capture, the transitions are devoid of any perturbations. These smooth transitions are desirable in a computer system, power glitches being the leading cause of power-related system crashes.

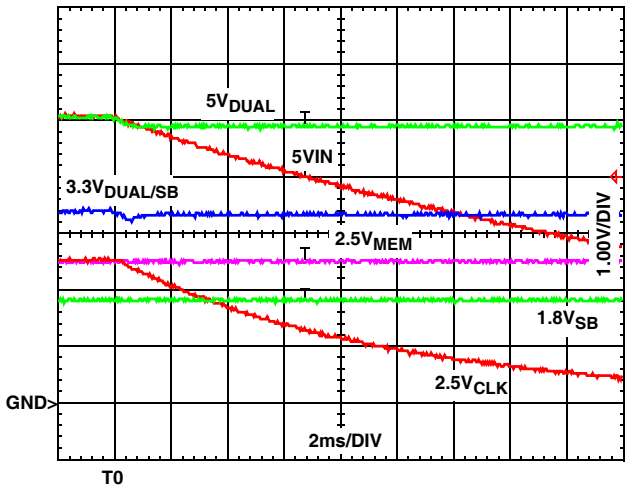


FIGURE 4. HIP6503EVAL1 ACTIVE STATE (S0, S1) TO STANDBY STATE (S3) TRANSITION WITH ALL OUTPUTS ENABLED

Figure 5 highlights the transition back from S3 sleep state to active state with all outputs enabled, as captured on the HIP6503EVAL1 board. Prior to time T0, the evaluation board was operating in S3 sleep state, with SW1 and SW2 on and SW3 off. At time T0, SW2 is switched off, enabling the main ATX outputs. As 3.3VIN, 5VIN, and 12VIN exceed their undervoltage thresholds, the 25ms timer internal to the HIP6503 is initiated. At T1 the time-out expires, conduction on the 3.3V$_{DUAL}$ and 5V$_{DUAL}$ outputs is transferred to the N-MOS switches and the 2.5V$_{CLK}$ output begins its ramp-up. At time T2, all the outputs are functional and ready for active state operation. The 2.5V$_{MEM}$ output is maintained glitch-free throughout the input voltage transition from the standby to the main ATX outputs.

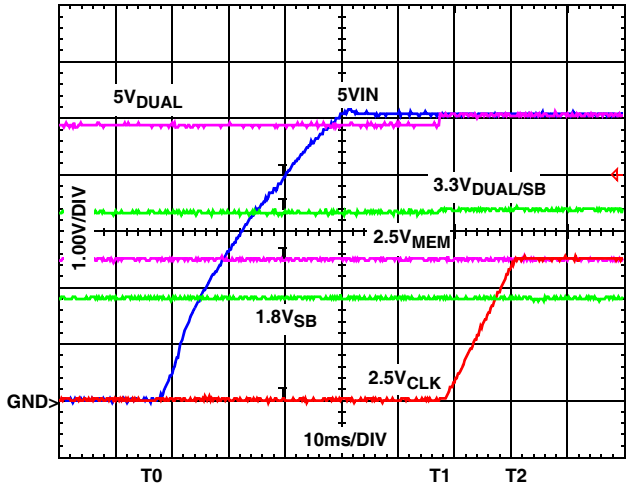


FIGURE 5. HIP6503EVAL1 STANDBY STATE (S3) TO ACTIVE STATE (S0, S1) TRANSITION WITH ALL OUTPUTS ENABLED

Figure 6 highlights the transition from S5 sleep state to active state (S0, S1) with all outputs enabled, as captured on the HIP6503EVAL1 board. Prior to time T0, the evaluation board was operating in S5 sleep state, with SW1 and SW3 on and SW2 off. At time T0, SW3 is switched off, enabling the main ATX outputs. As 3.3VIN, 5VIN, and 12VIN exceed their undervoltage thresholds (5VIN shown, only), the 25ms timer internal to the HIP6503 is initiated and, similar to the start-up shown in Figure 8, the 5V$_{DUAL}$ output undergoes a quasi-soft-start as conduction takes place through the body diode of the pass NMOS switch. At T1 the time-out expires, conduction on the 3.3V$_{DUAL/SB}$ and 5V$_{DUAL}$ outputs is transferred to the N-MOS switches, and the 2.5V$_{CLK}$ and 2.5V$_{MEM}$ outputs begin their ramp-up. At time T2, all the outputs are functional and ready for active state operation.

The 25ms time-out employed by the HIP6503 is necessary in order to insure that the main ATX outputs are allowed to stabilize and reach regulation limits before any circuits are connected to, or are allowed to derive their voltages from

them. This technique insures glitch-free operation, compatible with virtually any ATX power supply.

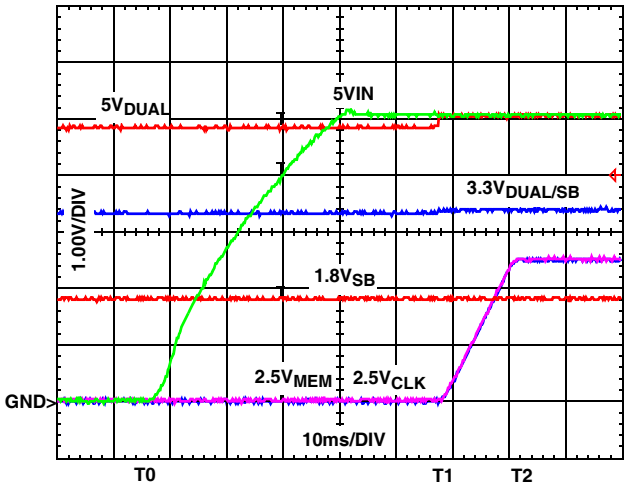


FIGURE 6. HIP6503EVAL1 STANDBY STATE (S5) TO ACTIVE STATE (S0, S1) TRANSITION WITH ALL OUTPUTS ENABLED

Transient Response

All outputs shown in the oscilloscope captures are DC offset by their nominal value and are DC coupled. The current waveforms underneath each of the output voltage waveforms show the (transient) current drawn from the respective output.

In Figure 7, the outputs shown are separately subjected to load transients while operating in active state (S0, S1). Transient loading of the outputs is as follows:
- 2.5V_{MEM}: 500mA to 3.2A at 1A/µs
- 2.5V_{CLK}: 180mA to 700mA at 0.2A/µs

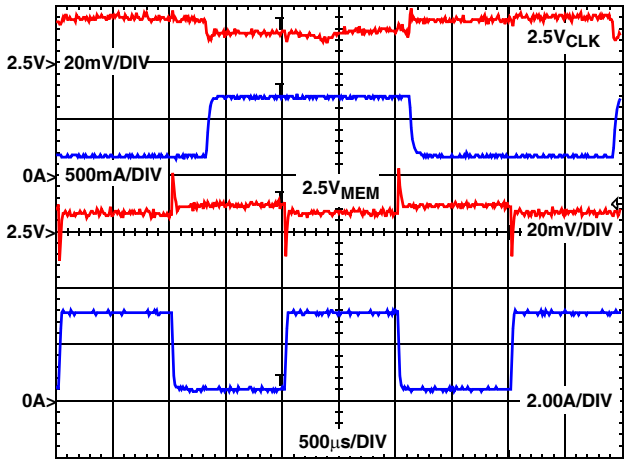


FIGURE 7. HIP6503EVAL1 ACTIVE STATE (S0, S1) OUTPUT TRANSIENT RESPONSE

In Figure 8, the outputs shown are separately subjected to load transients while operating in active state (S0, S1). Transient loading of the outputs is as follows:
- 3.3V_{DUAL}: 500mA to 3.2A at 0.5A/µs
- 5V_{DUAL}: 200mA to 2.5A at 0.5A/µs

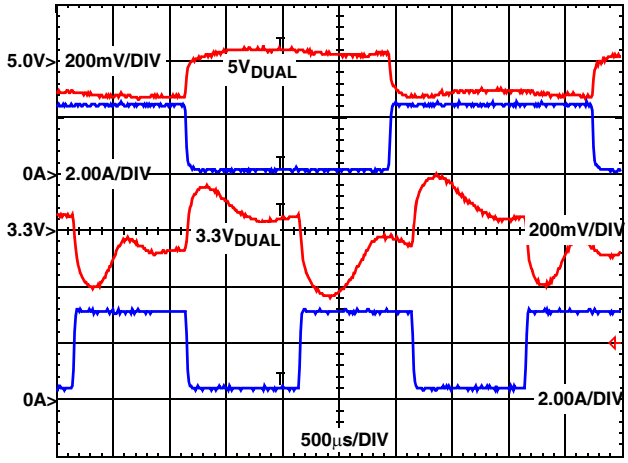


FIGURE 8. HIP6503EVAL1 ACTIVE STATE (S0, S1) OUTPUT TRANSIENT RESPONSE

The 3.3V_{DUAL} and 5V_{DUAL} outputs closely follow the AC meandering of the ATX 3.3V and 5V outputs, being separated only by the $r_{DS(ON)}$ of the N-MOS switches (Q4 and Q6). During the transient loading, the 3.3V_{DUAL} output develops a DC offset (compared to the ATX 3.3V), due to the voltage droop across Q4. Specific to this circuit and the particular circuit loading, the offset can easily be identified as the product of the $r_{DS(ON)}$ of the pass transistor and the output current. A similar explanation accompanies the 5V_{DUAL} output waveform.

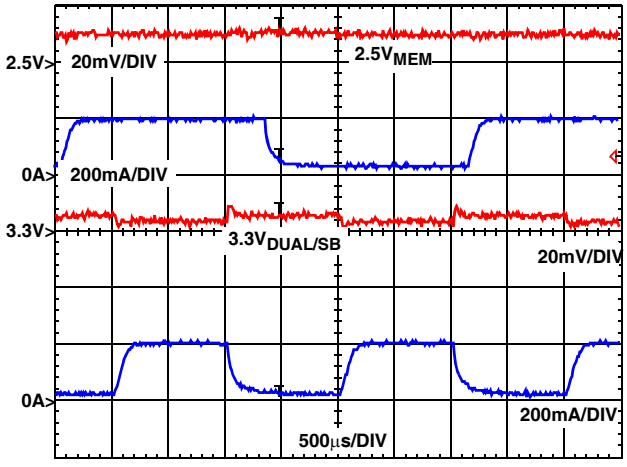


FIGURE 9. HIP6503EVAL1 SLEEP STATE (S3) OUTPUT TRANSIENT RESPONSE

In Figure 9, the outputs shown are separately subjected to load transients while operating in sleep state (S3). Transient loading of the outputs is as follows:

- 2.5V_{MEM}: 50mA to 200mA at 0.1A/µs
- 3.3$V_{DUAL/SB}$: 30mA to 200mA at 0.1A/µs

Output Short-Circuit Protection

Figure 10 depicts the circuit's behavior in response to a sudden output short-circuit (output under-voltage), applied, in this scope capture, on the 2.5V_{MEM} output, while operating in active state. At time T0 a short-circuit is applied using an electronic load - as a result, the 2.5V output starts to rapidly discharge, followed by the ATX 3.3V powering the collector of Q2. The ATX 3.3V output crosses the falling under-voltage threshold at time T1. To avoid false triggers, all UV detectors are equipped with 10µs filters. As the ATX

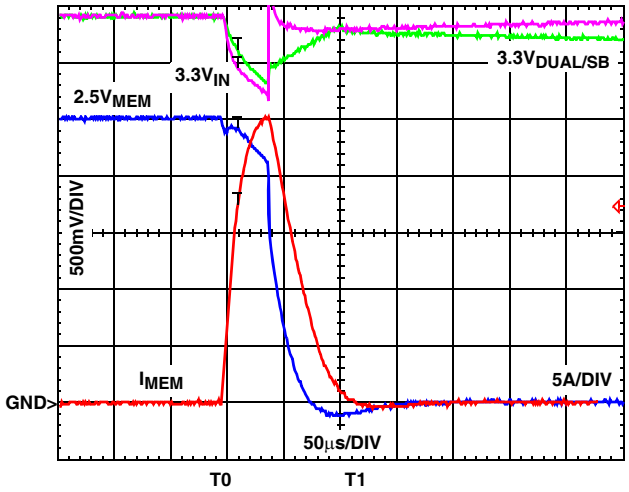


FIGURE 10. HIP6503EVAL1 2.5V_{MEM} OUTPUT UNDERVOLTAGE RESPONSE WHILE IN ACTIVE STATE (S0, S1)

3.3V voltage remains below the undervoltage (UV) threshold for more than 10µs, the HIP6503 triggers an automatic switch-over to S5 sleep state. As a result, the 2.5V_{MEM} output shuts down, and the ATX 3.3V output bounces back up. The 3.3$V_{DUAL/SB}$ also switches to the sleep state regulation path, regulating the output from the 5V_{SB} input.

If the ATX 3.3V output would not have been tripped below UV level (which is possible with a different supply and/or with more capacitance present on this line), a logic high output on the FAULT pin would have set the external fault latch circuitry, shutting down the ATX supply and quickly discharging the SS capacitor below the chip shutdown level. The chip reset disables the fault reporting and the latch maintains the circuit in a reset state. The latch is necessary to compensate for the slow response of the ATX supply, by shutting down the controller IC, along with the pass elements. Depressing the CLEAR FAULT button resets the latch and releases the circuit for operation.

Automatic State Switch-over During Loss of Main ATX Outputs

This feature allows the HIP6503 (as well as HIP6500B and HIP6502B) to maintain power delivery to some parts of the circuit, allowing the computer system to recover/re-boot following a momentary AC power loss. To achieve this task, the HIP6503 monitors all the active ATX outputs (3.3V, 5V, 12V) during active state operation to detect an UV event. If any of the three power rails fall below the UV threshold (typically 85%) while the $\overline{S3}$ and $\overline{S5}$ pins are held high (indicating active state operation request), the HIP6503 bypasses the active state request and switches over to S5 sleep state operation. Recovery from this operational mode is automatic upon restoration of the input power.

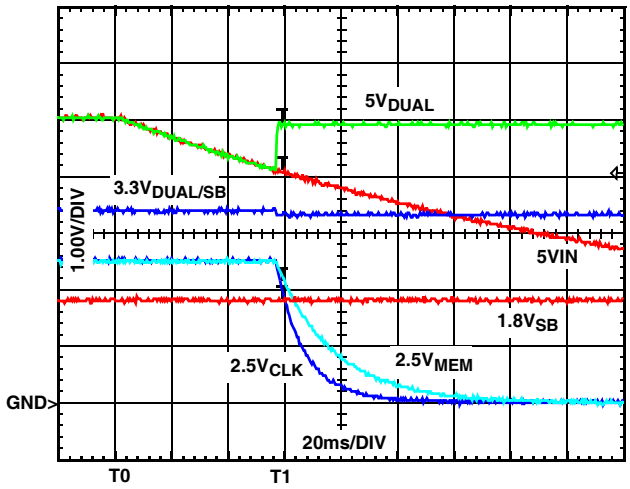


FIGURE 11. HIP6503EVAL1 AUTOMATIC SWITCHOVER TO S5 DUE TO LOSS OF MAIN ATX OUTPUTS

Figure 11 depicts such an automatic switch-over. Prior to time T0, the evaluation board was operating in active state, with SW1 on and SW2, SW3 off. Shortly before time T0, SW1 is switched off, shutting down the main ATX outputs; at time T0, the 5V_{IN} rail starts to slew down, under the current draw of the embedded serpentine resistor. At time T1, one of the main ATX outputs (3.3V, 5V, or 12V) discharges below the falling UV threshold, triggering the automatic switch-over to an S5 sleep state. As a result, the 2.5V_{CLK} and 2.5V_{MEM} outputs are turned off, and the 3.3$V_{DUAL/SB}$ and 5V_{DUAL} outputs switch to the sleep state regulation paths. The 1.8V_{SB} output remains undisturbed throughout the event.

Similarly, Figure 12 depicts the reversal switch-over into active mode. Prior to time T0, the evaluation board was operating in forced-S5 sleep state. Just before time T0, SW1 is switched on, restoring the main ATX outputs - at time T0, the 5V_{IN} rail starts to slew up. At time T1, the internal timer releases the chip from the forced-S5 state. As a result, the 2.5V_{CLK} and 2.5V_{MEM} outputs are soft-started back on, and the 3.3$V_{DUAL/SB}$ and 5V_{DUAL} outputs switch to the active

state regulation paths. The $1.8V_{SB}$ output remains, again, undisturbed throughout the event.

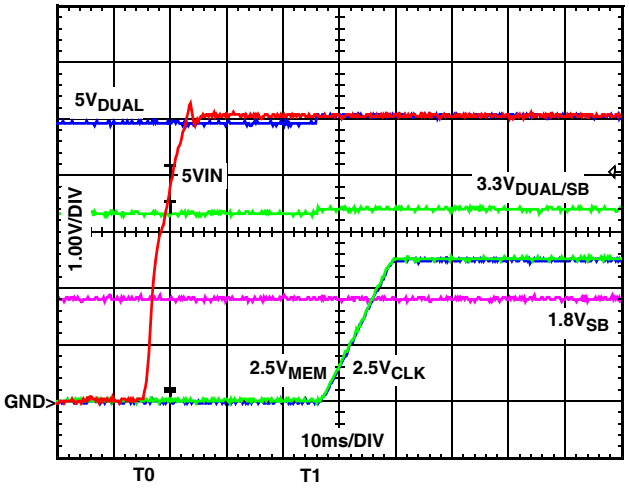


FIGURE 12. HIP6503EVAL1 AUTOMATIC SWITCHOVER FROM FORCED-S5 TO S0 STATE UPON RESTORATION OF MAIN ATX OUTPUTS

HIP6503EVAL1 Modifications

Setting the 2.5/3.3V_{MEM} Output to 3.3V

The HIP6503EVAL1 evaluation board ships populated to demonstrate support for RDRAM or some double data rate (DDR) SDRAM memory, with the memory output set for 2.5V. The HIP6503, however, is designed for either 2.5V or 3.3V memory output voltage. To change the memory output voltage on the evaluation board perform the following steps:

- Replace R5 with a 15kΩ resistor
- Remove Q2, and install an N-MOS transistor in its place (HUF76113 or equivalent recommended). Please note the connection diagram and insure the correct connections are established (N-MOS might not fit the provided footprint)

With the above modifications, the memory output will be set to 3.3V. In this configuration, the output voltage obtainable in active state is directly related to the ATX 3.3V output, the memory output current, and the $r_{(DS)ON}$ of Q2, according to the following equation:

$$V_{MEM} = V_{IN} - I_{MEM} \times r_{(DS)ON}$$

Improving Output Voltage Tolerance

The key to improving the output voltage tolerance is identifying the parameters which affect it, and then taking steps toward improving them.

The output DC voltage droop on the $3.3V_{DUAL/SB}$ (active state only) and $5V_{DUAL}$ outputs under applied load is due to the resistive losses across the N-MOS switch's own $r_{DS(ON)}$, thus decreasing the $r_{DS(ON)}$ results in reduced load-dependent voltage drooping.

High dV/dt spikes present in the output voltage waveform under highly dynamic load application (high dI/dt) are due to the ESR and the ESL of the output capacitance. These spikes coincide with the transient load's rising and falling edges, and decreasing their amplitude can be achieved by using lower ESR/ESL output capacitors (such as surface-mount tantalum capacitors), and/or the addition of more ceramic capacitors, which have inherently low ESR/ESL.

The addition of more input-side capacitance and decreasing the input-side capacitor banks' ESR can also help in situations where the input-side ripple is affecting the output regulation. Such an example is excessive ATX 3.3V ripple reducing the collector-to-emitter voltage available for Q2 (2.5V setting), and thus inducing an output droop component - in such instance, the addition of input-side capacitance and reduction of the ESR component can reduce the output excursion.

Conclusion

The HIP6503 is a sophisticated integrated circuit that embodies all the required circuitry for ACPI implementation in computer motherboards and computer systems. The circuit employs intelligent switching methods for smooth power plane transitions, noise immunity circuits for nuisance trip avoidance, and a direct interface to the south bridge and logical circuitry for simplified control and configuration.

References

For Intersil documents available on the internet, see web site www.intersil.com/

[1] Advanced Configuration and Power Interface Specification, Revision 1.0, December 1996, Intel/Microsoft/Toshiba. (http://www.teleport.com/~acpi/).

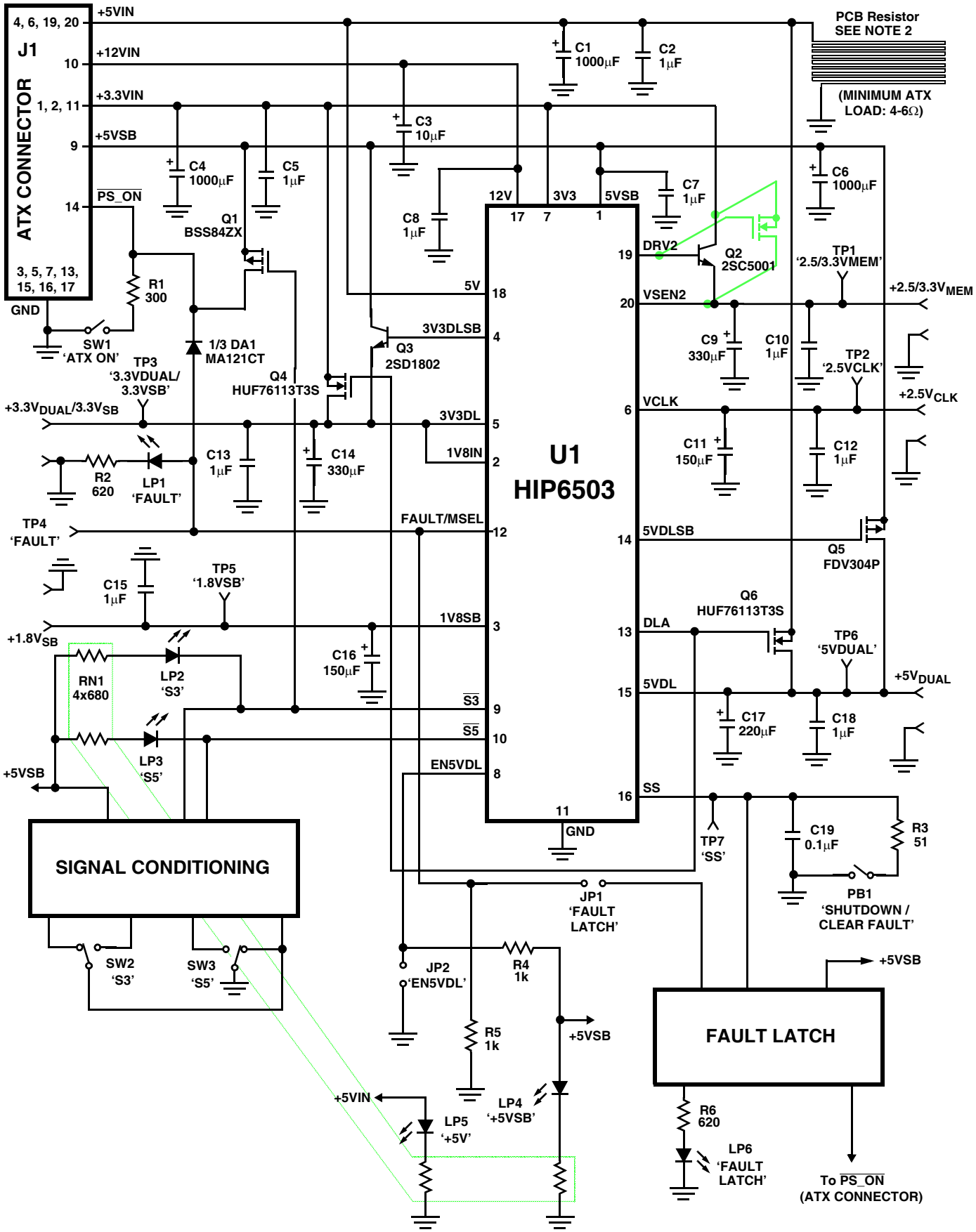
[2] *HIP6020 Data Sheet,* Intersil Corporation, Power Management Products Division, FN4683. (http://www.intersil.com/).

[3] *HIP6021 Data Sheet,* Intersil Corporation, Power Management Products Division, FN4684.

[4] ATX Specification, Version 2.02, October 1998, Intel Corporation (http://www.teleport.com/~atx/).

[5] *HIP6503 Data Sheet,* 2000, Intersil Corporation, Power Management Products Division, FN4882.

HIP6503EVAL1 Schematic



Signal Conditioning and Fault Latch Circuits

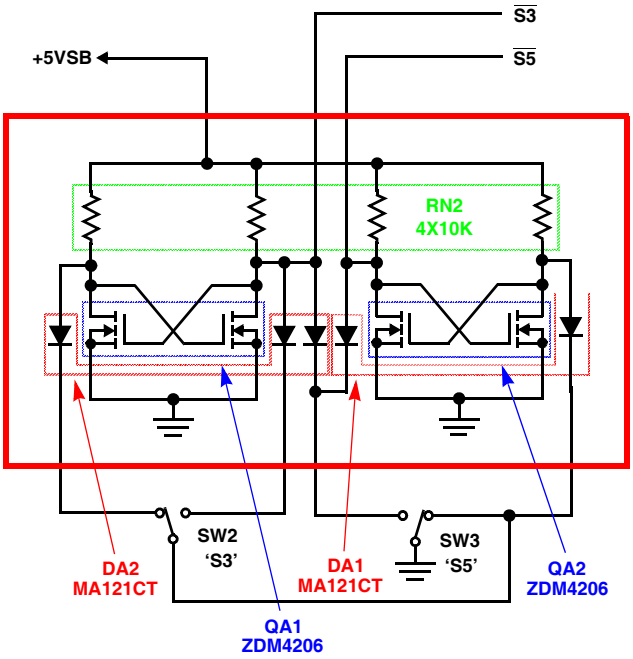


FIGURE 13. SIGNAL CONDITIONING BLOCK

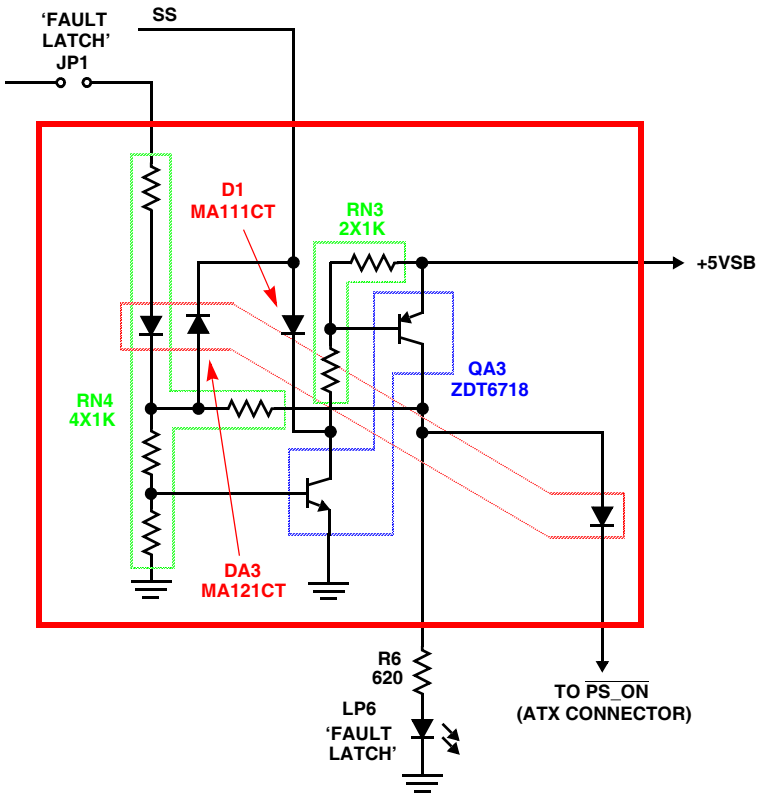


FIGURE 14. FAULT LATCHING BLOCK

Bill of Materials for HIP6503EVAL1

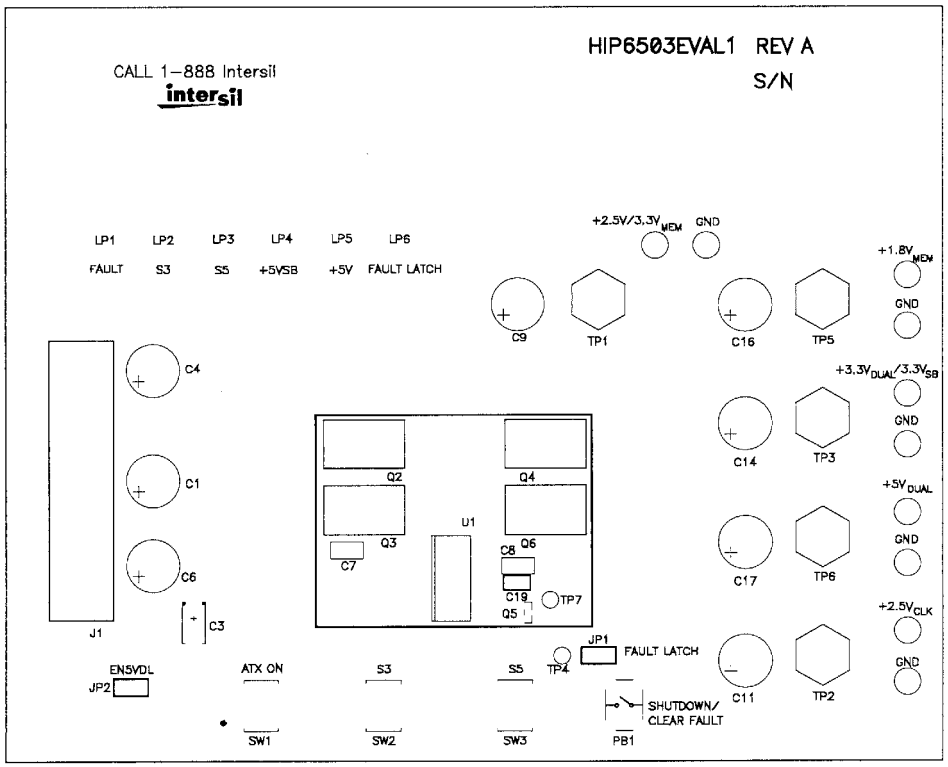
REF	PART NO.	DESCRIPTION	PACKAGE	VENDOR	QTY
C1,4,6	6MV1000CA	Al. Electrolytic Capacitor, 6.3V, 1000µF	8 x 11.5	Sanyo	3
C2,5,7,8,10,12,13,15,18	1µF Ceramic	Ceramic Capacitor, Y5V, 16V, 1.0µF	0805	Any	9
C3	TAJC106M020R	Tantalum Capacitor, 20V, 10µF	3.2 x 6.0	AVX	1
C9,14	6.3ZA330	Al. Electrolytic Capacitor, 6.3V, 330µF	8 x 11.5	Rubycon	2
C11,16	EEUFC1V151	Al. Electrolytic Capacitor, 35V, 150µF	8 x 11.5	Panasonic	2
C17	EEUFC1E221	Al. Electrolytic Capacitor, 25V, 220µF	8 x 11.5	Panasonic	1
C19	0603YC104MAT2A	Ceramic Capacitor, X7R, 16V, 0.1µF	0603	AVX	1
D1	MA111CT-ND	Switching Diode, 80V, 100mA	Mini 2P	Digikey	1
DA1-3	MA121CT-ND	Diode Array, 80V, 100mA	Mini 6P	Digikey	3
J1	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		Molex	1
JP1,2	68000-236	Jumper header	0.1” spacing	Berg	4/36
	71363-102	Jumper shunt	0.1” spacing	Berg	2
LP1-6	L63111CT-ND	Miniature LED, through-board indicator		Digikey	6
PB1	P8007S-ND	Push-button, miniature		Digikey	1
Q1	BSS84ZXCT-ND	Logic P-MOSFET, 50V, 10Ω	SOT-23	Digikey	1
Q2	2SC5001	NPN Bipolar, 20V,10A	TO-252AA	Rohm	1
Q3	2SD1802	NPN Bipolar, 50V, 3A	TO-252AA	Sanyo	1
Q4,6	HUF76113T3S	UltraFET™ MOSFET, 30V, 31mΩ	SOT-223	Intersil	2
Q5	FDV304P	Logic P-MOSFET, 25V, 1.5Ω	SOT-23	Fairchild	1
QA1,2	ZDM4206NCT-ND	Small-signal Dual MOSFET, 60V, 1Ω	SM-8	Digikey	2
QA3	ZDT6718CT-ND	Small-signal Bipolar Pair, 20V, 1.5A	SM-8	Digikey	1
R1	300Ω	Resistor, 5%, 0.1W	0603	Any	1
R2,6	620Ω	Resistor, 5%, 0.1W	0603	Any	2
R3	51Ω	Resistor, 5%, 0.1W	0603	Any	1
R4,5	1kΩ	Resistor, 5%, 0.1W	0603	Any	2
RN1	Y9681CT-ND	4-Resistor Network, 680Ω, 5%, 0.1W	3.2 x 1.6	Digikey	1
RN2	Y9103CT-ND	4-Resistor Network, 10kΩ, 5%, 0.1W	3.2 x 1.6	Digikey	1
RN3	Y8102CT-ND	2-Resistor Network, 1kΩ, 5%, 0.1W	1.6 x 1.6	Digikey	1
RN4	Y9102CT-ND	4-Resistor Network, 1kΩ, 5%, 0.1W	3.2 x 1.6	Digikey	1
SW1	GT12MSCKE	Miniature Switch, Single Pole, Single Throw		C&K	1
SW2,3	GT11MSCKE	Miniature Switch, Single Pole, Double Throw		C&K	2
TP1-3,5,6	1314353-00	Test Point, Scope Probe		Tektronics	5
TP4,7	SPCJ-123-01	Test Point		Jolo	2
U1	HIP6503CB	ACPI Multiple Linear Controller	SOIC-20	Intersil	1
+2.5/3.3V_{MEM}, +2.5V_{CLK}, +3.3V_{DUAL}/3.3V_{SB}, +1.8V_{SB}, +5V_{DUAL}, GND	1514-2	Terminal Post		Keystone	10

NOTES:

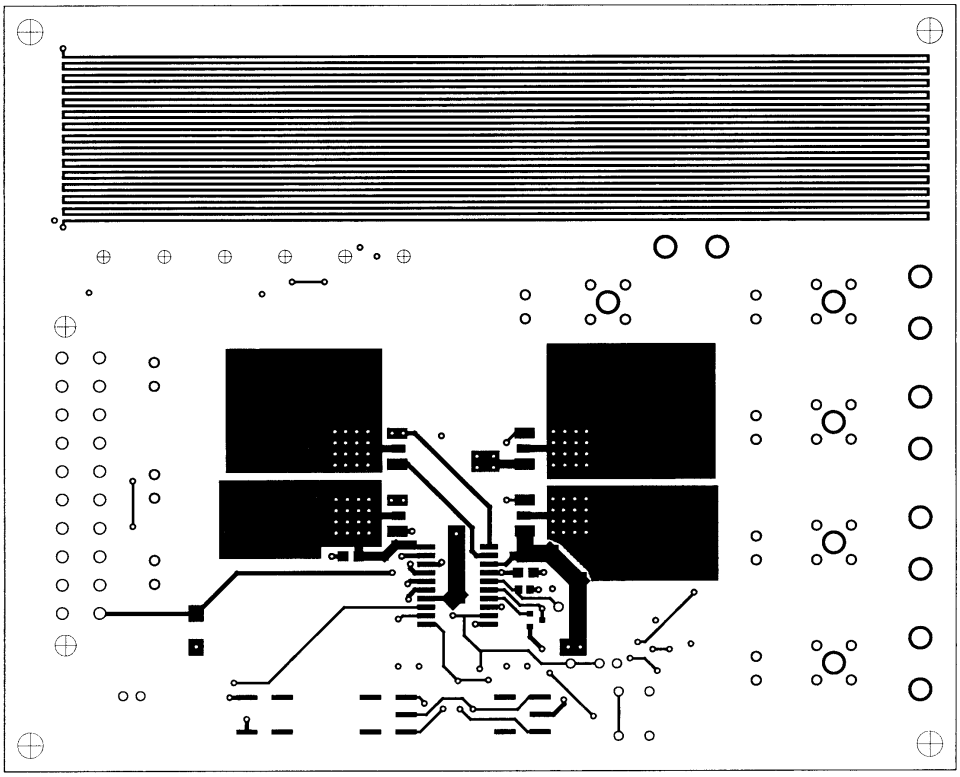
1. Q2 has to be replaced by an NMOS transistor when 3.3V V_{MEM} output is desired (see circuit diagram for proper connection).
2. R3 has to be replaced by a 15kΩ resistor when 3.3V V_{MEM} output is desired.

HIP6503EVAL1 Layout

TOP SILK SCREEN

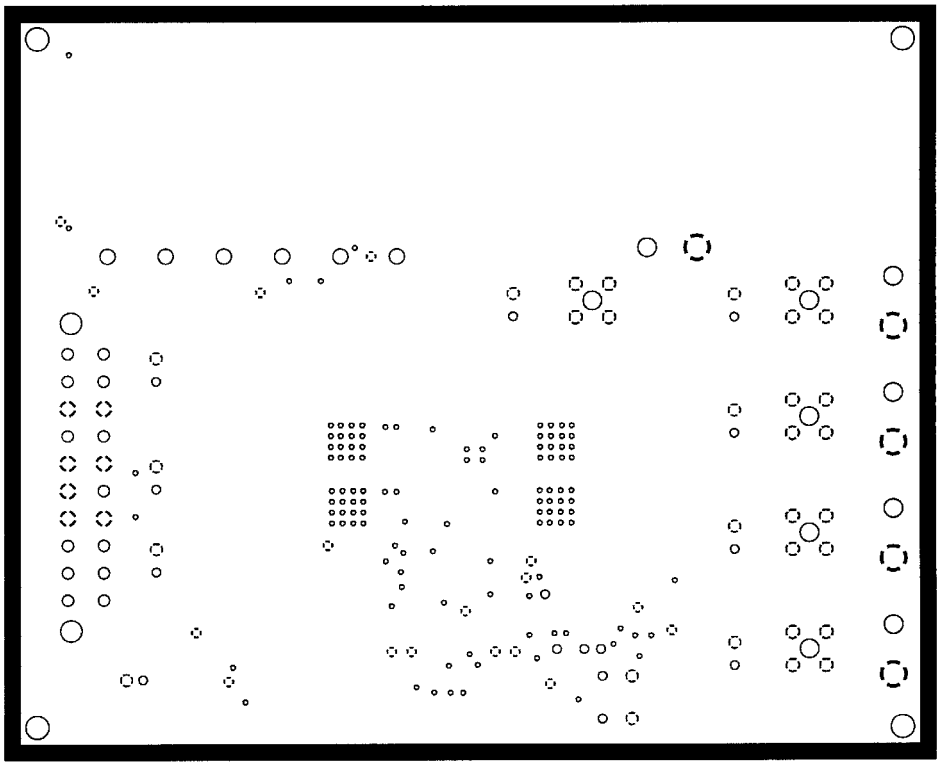


TOP LAYER

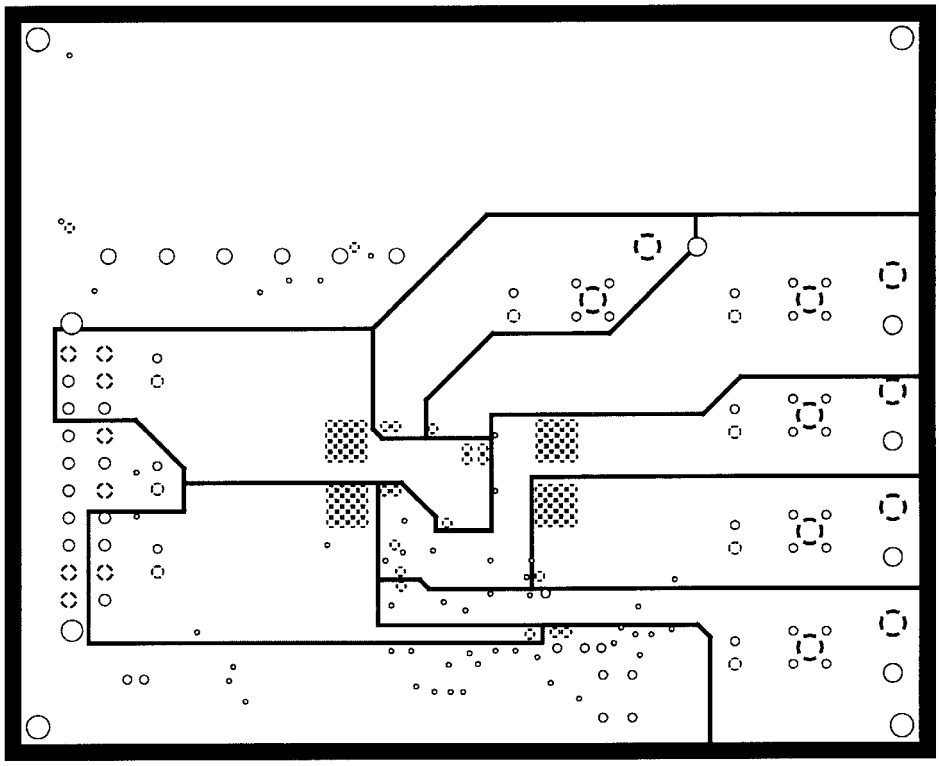


HIP6503EVAL1 Layout (Continued)

GROUND LAYER

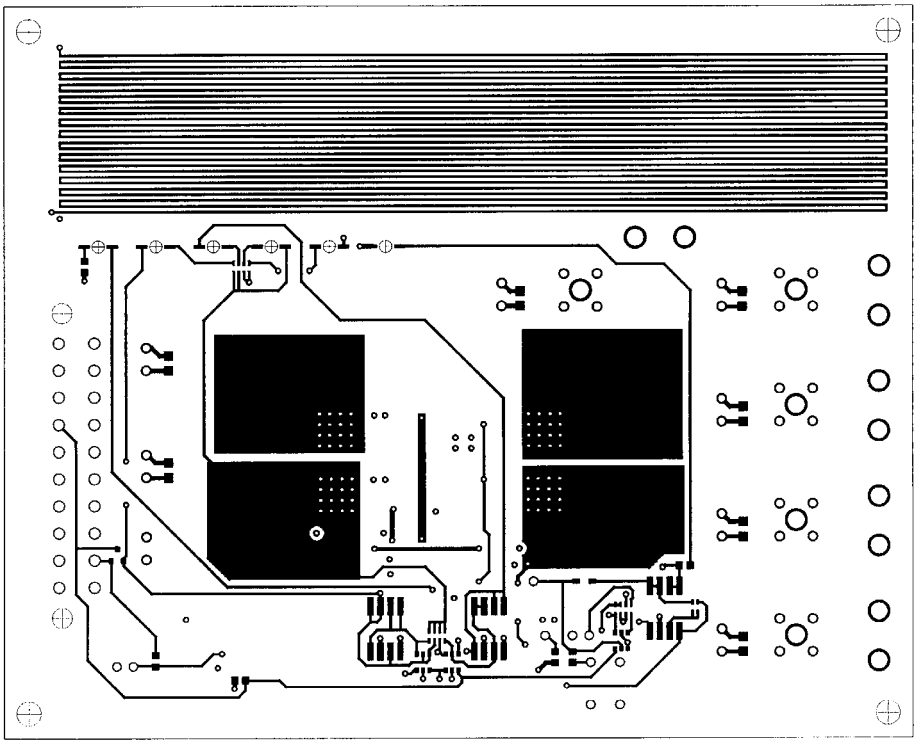


POWER LAYER



HIP6503EVAL1 Layout (Continued)

BOTTOM LAYER



BOTTOM SILK SCREEN