ISL8103EVAL1: Three Phase Buck Converter with Integrated High Current 5-12V Drivers

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Introduction

The progress in many parts of modern power systems such as DDR/Chipset core voltage regulators, high current low voltage DC/DC converters, FPGA/ASIC DC/DC converters and many other general purpose applications keeps challenging the power management IC makers to come up with innovative products and new solutions to meet the increase in power, reduction in size and increase in the DC/DC converter's efficiency targets. The interleaved multiphase synchronous buck topology proves again to be the topology of choice for such high current low voltage applications.

The ISL8103 is a space-saving, cost-effective solution for such applications. The ISL8103 is a three-phase PWM control IC with integrated high current MOSFET drivers. The integration of 5-12V high current MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multi-phase product families. By reducing the number of external parts, this integration allows for a cost and space saving power management solution.

Output voltage can be programmed using the on-chip DAC or an external precision reference. A two bit code programs the DAC reference to one of 4 possible values (0.6V, 0.9V,1.2V and 1.5V). A unity gain, differential amplifier is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be offset through the use of single external resistor. An optional droop function is also implemented and can be disabled for applications having less stringent output voltage variation requirements or experiencing less severe step loads.

A unique feature of the ISL8103 is the combined use of both DCR and $r_{DS(ON)}$ current sensing. Load line voltage positioning and overcurrent protection are accomplished through continuous inductor DCR current sensing, while $r_{DS(ON)}$ current sensing is used for accurate channel-current balance. Using both methods of current sampling utilizes the best advantages of each technique.

Protection features of this controller IC include a set of sophisticated overvoltage and overcurrent protection. Overvoltage results in the converter turning the lower MOSFETs ON to clamp the rising output voltage and protect the load. An OVP output is also provided to drive an optional crowbar device. The overcurrent protection level is set through a single external resistor. Other protection features include protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the output load.

The ISL8103EVAL1 evaluation board embodies a 85-90A regulator solution targeted at supplying power to the designated load. The physical board design is optimized for 3 phase operation and ships out configured to provide one of the following four output voltages (0.6V, 0.9V, 1.2V and 1.5V) depending on choice of the REF1, REF0 combination set by DIP switch U2, but can be easily modified to provide any output voltage values in the range of 0.6-2.3V by means of resistor divider composed of R90 and R81.

For further details on the ISL8103, consult the data sheet [1].

The Intersil multi-phase family controller and driver portfolio continues to expand with new selections to better fit our customer needs. Refer to our web site for updated information: **www.intersil.com**.

ISL8103EVAL Board Design

The evaluation kit consists of the ISL8103EVAL1 evaluation board, the ISL8103 datasheet, and this application note. The evaluation board is optimized for three phase operation without droop, the nominal output voltage is 1.5V (with DIP switch U2 set to 11 position) and the maximum output current is 90A.

The evaluation board provides convenient test points, a DIP switch for DAC (REF) voltage selection from four possible values (0.6V, 0.9V, 1.2V and 1.5V), footprint for a resistor divider for output voltage adjustment up to 2.3V, and an on-board transient load generator to facilitate the evaluation process. An on board LED is present to indicate the status of the PGOOD signal. The board is configured for down conversion from 5-12V to the REF setting.

The printed circuit board is implemented in 6-layer, 2-ounce copper. Layout plots and part lists are provided at the end of this application note for this design.

Quick Start Evaluation

The ISL8103EVAL1 is designed for quick evaluation after following only a few simple steps. All that is required is two bench power supplies, Oscilloscope and Load. To begin evaluating the ISL8103EVAL1 follow the steps below.

1. Before doing anything to the evaluation board, make sure that the "Enable" switch (S1) is in the Disable position and the "Transient Load Generator" switch (S2) is in the Load Off position.
2. Connect a 12V, 15A Lab power supply between J7 and J8, this power supply provides VIN and PVCC (with original board configuration).
3. Connect a 5V, 1A Lab power supply between J23 and GND, this power supply provides VCC bias (and PVCC bias if the board is configured for 5V PVCC).

4. Set the “REF Selection” DIP switch (U2) to 11 corresponding to DAC = REF = 1.5V. Figure 1 details the typical default configuration for U2 when the board is shipped. In this default setting, the evaluation board is set for a reference voltage of 1.5V.

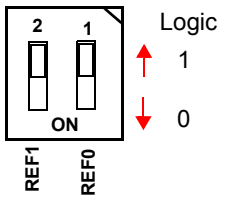


FIGURE 1. TYPICAL U2 DEFAULT SETTING 11 (1.500V)

5. Connect a load (either resistive or electronic) between VOUT terminal (J1, J2) and GND terminal (J3, J4).
6. Move the “Enable” switch (S1) to the Enable position releasing the IC ENLL pin to rise to begin regulation.

After step 6, the ISL8103EVAL1 should be regulating the output voltage, at the “VOUT+” and “VOUT-” test points (P20, P21) and J5 to the REF voltage. The “PGOOD Indicator” LED (D1) should be green to indicate the regulator is operating correctly.

ISL8103EVAL1 Board Features

Input Power Connections

The ISL8103EVAL1 allows for the use of standard bench power supplies for powering up the board. Two female-banana jacks are provided for connection of bench power supplies. Connect the +5V terminal to P23, +12V terminal to J7, and the common ground to terminal J8. Voltage sequencing is not required when powering the evaluation board.

Once power is applied to the board, the PGOOD LED indicator will begin to illuminate red. With S1 in the Disable position, the ENLL pin of the ISL8103 is held low and the startup sequence is inhibited.

Output Power Connections

The ISL8103EVAL1 output can be exercised using either resistive or electronic loads. Copper alloy terminal lugs provide connection points for loading. Tie the positive load connection to VOUT, terminals J1 and J2, and the negative to ground, terminals J3 and J4. A shielded scope probe test point, J5, allows for inspection of the output voltage, VOUT.

REF and VOUT Setup

The REF DIP switch would be preset to 11 (1.500V). Also 1.2V, 0.9V and 0.6V outputs can be selected using different codes on the DIP switch. If an output voltage different than the 4 possible REF values is desired, the output resistor divider composed of R90 (initially 0Ω) and R81 (initially open) can be used (consult Data sheet and the section entitled **Adjusting the Output Voltage** at the end of this application note for resistor value calculations). Note that the ISL8103 is usable for output voltages up to 2.3V when the REF voltage is set to 1.5V. See Table 1 below for the maximum possible output voltage with different REF setting.

TABLE 1. MAXIMUM OUTPUT VOLTAGE WITH DIFFERENT REF SETTING WITH THE USE OF A RESISTOR DIVIDER ON VSEN

REF1	REF0	REF=DAC	VOUT MAX
0	0	0.6V	1.4V
0	1	0.9V	1.7V
1	0	1.2V	2V
1	1	1.5V	2.3V

PVCC Power Options

One unique feature of the ISL8103 is the variable gate drive bias for the integrated drivers. The gate drive voltage for the internal drivers can be any voltage from +5V to +12V by simply connecting the desired voltage to the PVCC pin of the controller. To accommodate the flexibility of the drivers, the ISL8103EVAL1 has been designed to support a multitude of options for the PVCC voltage.

Switching between the different PVCC voltages available on the evaluation board is as simple as populating and depopulating certain resistors. The eval board has three on board voltages available: +5V, +12V, and +8V (from an onboard linear regulator). Refer to Table 2 for what resistors to populate for each voltage option.

TABLE 2. GATE DRIVE VOLTAGE OPTIONS AND RESISTOR SETTINGS

UGATE VOLTAGE	LGATE VOLTAGE	R48	R68	R71	R72
12.0V	12.0V	OPEN	OPEN	OPEN	0Ω
8.0V	8.0V	OPEN	OPEN	0Ω	OPEN
5.0V	5.0V	0Ω	OPEN	OPEN	OPEN
12.0V	5.0V	0Ω	0Ω	OPEN	OPEN

Enabling the Controller

In order to enable the controller, the board must be powered, a REF (DAC) code must be set, and the PVCC and VCC voltages must be set. If these steps have been properly followed, the regulator is enabled by toggling the “ENABLE” switch (S1) to the Enable position, which allows the voltage on the ENLL pin of the ISL8103 to rise above the ENLL threshold of 0.66V and the controller will begin its digital soft start sequence. The output voltage ramps up to the programmed setting, at which time the PGOOD indicator will switch from red to green.

On-Board Load Transient Generator

Most bench-top electronic loads are not capable of producing the current slew rates required to emulate most modern loads. For this reason, a discrete transient load

generator is provided on the evaluation board, see Figure 2. The generator produces a load pulse of 550µs in duration with a period of 70ms. The pulse magnitude is approximately 30A with rise and fall slew rates of approximately 50A/µs as configured. The short load current pulse and long duty cycle is required to limit the power dissipation in the load resistors (R38-R42) and MOSFETs (Q20, Q21). To engage the load generator simply place switch S2, in the “OFF” position.

If the DAC code is changed from 11(1.500V), the transient generator dynamics must be adjusted relative to the new output voltage level. Place a scope probe in J10 to measure the voltage across the load resistors and the dV/dt across them as well. Adjust the load resistors, R38-R40, to achieve the correct load current level. Change resistors R34-R37 to increase or decrease the dV/dt as required to match the desired dI/dt profile.

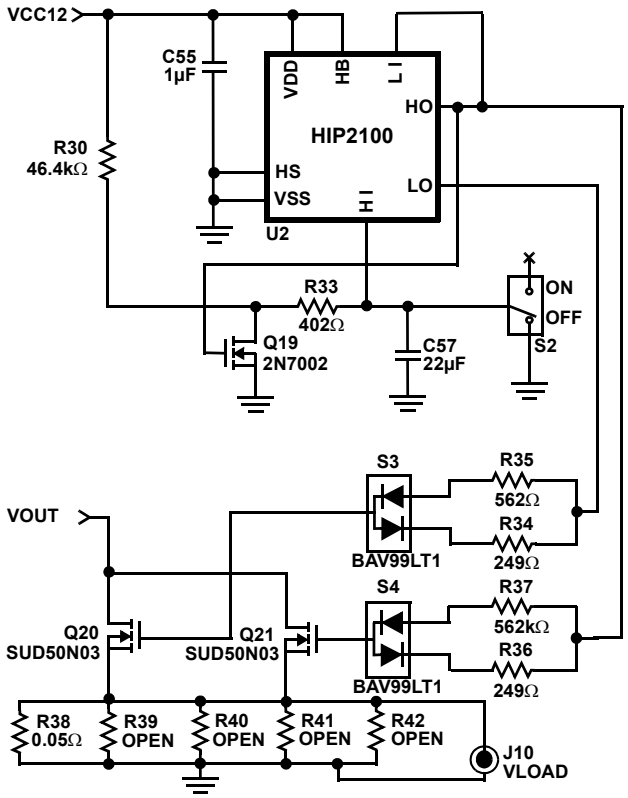


FIGURE 2. LOAD TRANSIENT GENERATOR

Inductor DCR Static Current Sense Points

A unique feature of the ISL8103EVAL1 is the ability to measure the voltage drop across the DCR of each channel’s inductor by multimeter. This is accomplished with the use of a capacitor and resistor series circuit which is placed in parallel across each inductor as illustrated in Figure 3. When current, I_L, flows through the inductor, the voltage drop developed across the DCR will be sensed by the R-C circuit, and an equivalent voltage will be developed across the capacitor C.

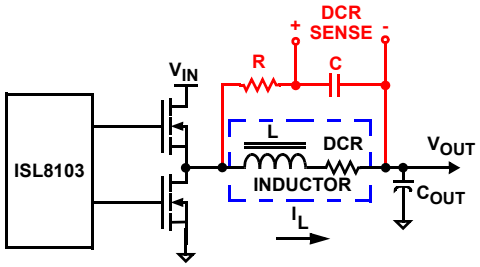


FIGURE 3. DCR STATIC CURRENT SENSE CIRCUIT

In order to not affect the rest of the regulator, the time constant of this R-C circuit is very large, so it can only be used to measure static current, and not transient currents. To calculate the current through each inductor measure the voltage across the “DCR SENSE” points on the ISL8103EVAL1 and then divide that number by the DCR of the inductor. This should give you an accurate reading of the current through each channel during static loads.

Modifying the ISL8103EVAL1 Design

Current Balance Resistors

The ISL8103 uses lower MOSFET $r_{DS(ON)}$ current sensing to measure the current through each channel and balance them accordingly. If the lower MOSFETs on the ISL8103EVAL1 are changed, the current balance resistors, R18-R20, should also be changed to adjust for the change in $r_{DS(ON)}$. Refer to page 19 in the ISL8103 datasheet to choose new current sense resistors. R18 adjusts the current in channel 1, R19 adjusts the currents in channel 3 and R20 adjusts the currents in channel 2. These resistors can also be changed to adjust for any current imbalance due to layout, which is also explained on page 19 of the ISL8103 datasheet.

Load Line (Droop) Regulation

The ISL8103 has an optional Droop function, the ISL8103EVAL1 board design is optimized for no Droop case. For Droop option selection follow Table 3.

TABLE 3. SELECTION OF DROOP OPTION

DROOP	R86	R85
Disabled (Droop connected to IREF)	0Ω	OPEN
Enabled (Droop connected to ICOMP)	OPEN	0Ω

If Droop is implemented, the compensation network will need to be recalculated for optimal loop response and stability.

To create an output voltage change proportional to the total current in all the active channels (droop), the ISL8103 uses an inductor DCR sensing R-C network. This network, shown in Figure 4, is designed not only to precisely control the load line of the regulator, but also to thermally compensate for any changes in DCR that may skew the load line as a result of increases in temperature.

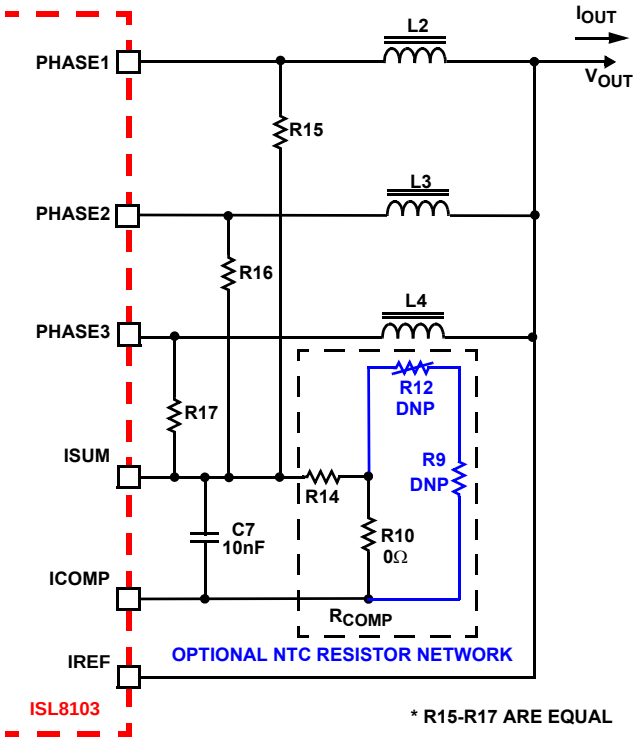


FIGURE 4. DCR SENSING CONFIGURATION WITH OPTIONAL FOOTPRINTS FOR NTC LOAD-LINE COMPENSATION

This sensing technique works off the principle that if the R-C time constant of C7 * Rcomp (Rcomp = R14) is equal to the L/DCR time constant of the inductor, the load line impedance will be equal to Rcomp*DCR/R15 (R15, R16 and R17 are equal).

If the load line impedance needs to be changed, all that is required is adjusting the values of R15-R17 as explained on page 20 of the ISL8103 datasheet. If the Inductor is changed though, the resistance of time constant matching network will need to be changed. The NTC resistor network must first be adjusted so that the new L/DCR time constant is precisely matched. Refer to page 19 and 20 of the ISL8103 datasheet to design the entire R-C sense network.

An Optional NTC resistor network consisting of 3 resistors (R9, R10, and R14) and a single NTC thermistor (R12), which is placed close the output inductors. This network is designed to compensate for any change in DCR that occurs due to temperature when the Droop option is used and a tight load-line regulation is required, and keep the time constant of the R-C network equal to that of the inductor L/DCR time constant.

Overcurrent Protection Level

The ISL8103 utilizes a single resistor to set the maximum current level for the IC's overcurrent protection circuitry. Please refer to page 17 of the ISL8103 datasheet, and adjust resistor R11 accordingly to set the desired overcurrent trip level.

Output Voltage Offset

The ISL8103 allows a designer to accurately offset the output voltage both negatively and positively. All that is required is a single resistor between the OFS and VCC pins, or the OFS pin and GND. The ISL8103EVAL1 has both of these resistor options available on the board. To positively offset the output voltage populate resistor R5. To negatively offset the output voltage populate resistor R7. Please refer to page 13 of the ISL8103 datasheet to accurately calculate these resistor values.

Switching Frequency

The switching frequency of the ISL8103EVAL1 board is set to an optimal value of 325kHz giving the best efficiency and performance for the given design with R13 = 75kΩ. However, the switching frequency can be adjusted anywhere from 80kHz to 1.5MHz per phase. In practice many factors affect the choice of switching frequency among which are efficiency, and gate drive losses (which depend on the MOSFET choice and Gate Driver Voltage). Since the ISL8103 has integrated MOSFET drivers, the driver losses must be taken into account when the switching frequency is chosen. To change the switching frequency refer to page 24 of the ISL8103 datasheet and adjust the value of frequency set resistor, R13, accordingly.

MOSFET Gate Drive Voltage (PVCC)

The gate drive bias voltage of the integrated drivers in the ISL8103 can be any voltage between +5V and +12V. This bias voltage is set by connecting the desired voltage to the PVCC pins of the IC. Please refer to the *PVCC Power Options* section to set the desired gate drive voltage.

Number of Active Phases

The ISL8103 has the option of 1, 2 or 2-phase operation. The ISL8103EVAL1 is designed to change the number of active phases by simply populating or depopulating few resistors, R62 - R65. Refer to Table 4 for which resistors to populate for 1, 2 or 3-phase operation.

TABLE 4. SETTINGS FOR NUMBER OF ACTIVE PHASES

# OF ACTIVE PHASES	R62	R63	R64	R65
3	0Ω	0Ω	OPEN	OPEN
2	OPEN	0Ω	0Ω	OPEN
1	OPEN	OPEN	0Ω	0Ω

ISL8103 Performance

Soft-Start Interval

The typical start-up waveforms for the ISL8103EVAL1 are shown in Figure 5. The waveforms represented in this image show the soft-start sequence of the regulator with the DAC set to 1.50V. Before the soft-start interval begins, VCC and PVCC are above POR and the DAC inputs are set to logic 11. With these two conditions met, throwing the ENABLE

switch into the Enable position causes the voltage on the ENLL pin to rise above the ISL8103's enable threshold, beginning the soft-start sequence. For a delay time of 0.85ms, VOUT does not move due to the manner in which soft-start is implemented within the controller. After this delay (which is approximately equal to 240 switching cycles), VOUT begins to ramp linearly toward the DAC voltage. With the converter running at 325kHz, this ramp takes approximately 5.2ms, during which time the input current, ICC12, also ramps slowly due to the controlled building of the output voltage.

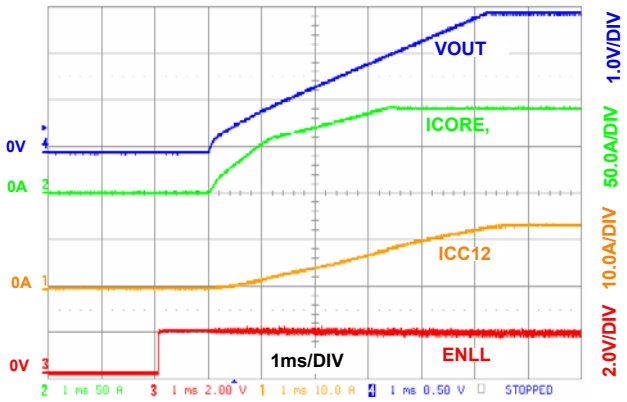


FIGURE 5. SOFT-START INTERVAL WAVEFORMS

Once VOUT reaches the DAC set point, the internal pull-down on the PGOOD pin is released. This allows a resistor from PGOOD to VCC to pull PGOOD high and the PGOOD LED indicator changes from red to green.

Special consideration is given to start-up into a pre-charged output (where the output is not 0V at the time the SS cycle is initiated). Under such circumstances, the ISL8103 keeps off both sets of output MOSFETs until the internal ramp starts to exceed the output voltage sensed at the FB pin. This special scenario is detailed in Figure 6. The circuit is enabled at time T0. As the internal ramp exceeds the magnitude of the output voltage at time T1, the MOSFETs drivers are enabled and the output voltage ramps up in a seamless fashion from the pre-existent level to the DAC-set level, reached at time T2.

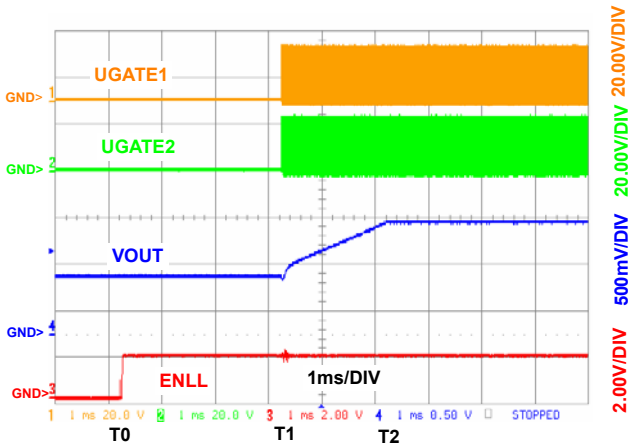


FIGURE 6. ISL8103EVAL1 START-UP INTO A PARTIALLY CHARGED OUTPUT (V_{DAC} = 1.200V)

A second scenario can be encountered with a pre-charged output: output being pre-charged above the DAC-set point, as shown in Figure 7. In this situation, the ISL8103 behaves in a way similar to that of Figure 6, keeping the MOSFETs off until the end of the SS ramp. However, once the end of the ramp has been reached, at time T1, the output drivers are enabled for operation, and the output is quickly drained down to set-point level.

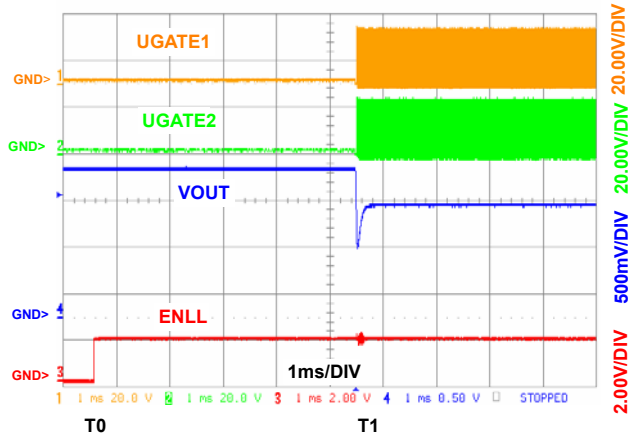


FIGURE 7. ISL8103EVAL1 START-UP INTO AN OVERCHARGED OUTPUT (V_{DAC} = 1.200V)

An OV condition during start-up will take precedence over this normal start-up behavior, but will allow reversal back to normal behavior as soon as the condition is removed or brought under control.

Transient Response

The ISL8103EVAL1 is designed without droop for a maximum output load current of 90A. The Load step is approximately 30A and the output voltage variation during the transient is kept below 100mV peak to peak. This load step have a maximum slew rate of approximately 50A/µs on both the rising and falling edges. The on-board load transient generator is designed to provide the specified load step, different load steps and current slew rates can be accommodated with the on Board Transient Load Generator.

The rising edge transient response of the ISL8103EVAL1, is shown in Figure 8. In order to obtain the load current waveform shown, the bench-top load is turned off, while the on-board transient generator is pulsing a 30A step for 550µs. When the load step occurs, the output capacitors provide the initial output current, causing VOUT to drop suddenly due to the ESR and ESL voltage drops in the capacitors. The controller immediately responds to this drop by increasing the PWM duty cycles to as much as 66%. The duty cycles then decrease to stabilize VOUT.

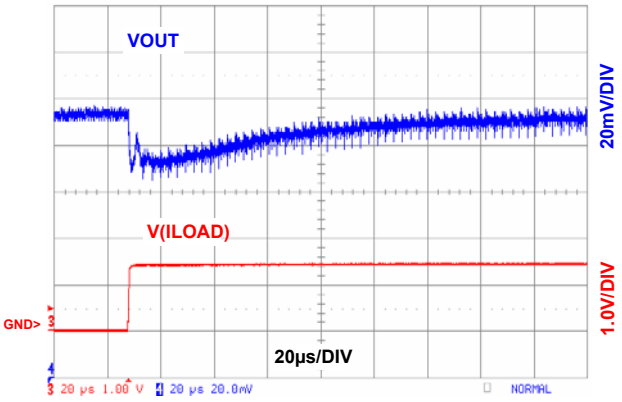


FIGURE 8. ISL8103EVAL1 RISING EDGE TRANSIENT LOAD RESPONSE

At the end of the 550µs load pulse, the load current returns to 0A. The transient response to this falling edge of the load is shown in Figure 9. When the falling load step occurs, the output capacitors must absorb the inductor current which can not fall at the same rate of the load step. This causes VOUT to rise suddenly due to the ESR and ESL voltage drops in the capacitors. The controller immediately responds to this rise by decreasing the PWM duty cycles to zero, and then increasing them accordingly to regulate VCORE to the programmed 1.5V level.

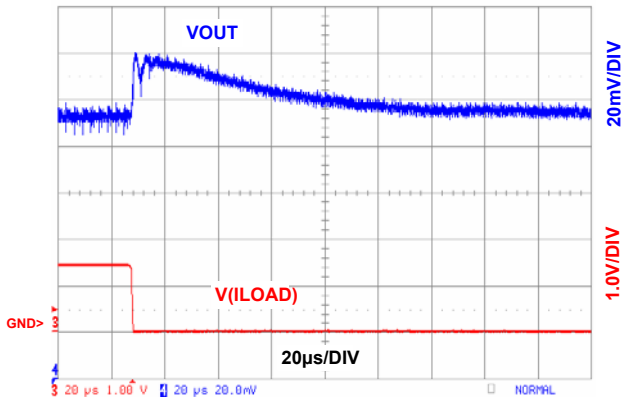


FIGURE 9. ISL8103EVAL1 FALLING EDGE TRANSIENT RESPONSE

Figure 10 shows both the rising and falling edges.

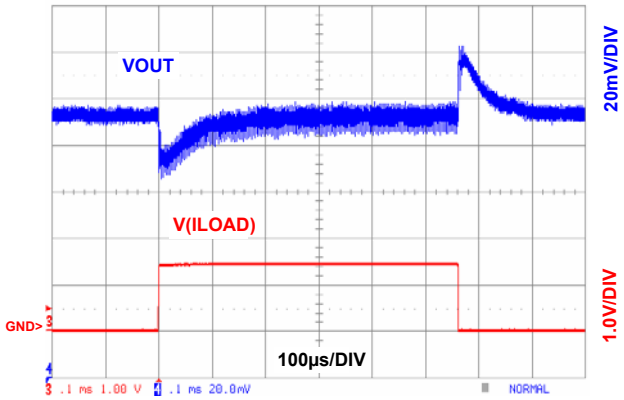


FIGURE 10. ISL8103EVAL1 TRANSIENT RESPONSE

Overcurrent Protection

The ISL8103 is designed to stop all regulation and protect the sensitive Load if an overcurrent event occurs. This is done by continuously monitoring the total output current and comparing it to an overcurrent trip level set by the OCSET resistor, R11. If the output current ever exceeds the trip level as shown in Figure 11 (at time T1), the ISL8103 immediately turns the upper and lower MOSFETs off, causing VOUT to fall to 0V. The controller holds the UGATE and LGATE signals in this state for a period of 4096 switching cycles, which at 325kHz is 13.65ms. The controller then re-initializes the soft-start cycle (at time T2). If the load that caused the overcurrent trip remains, another overcurrent trip will occur before the soft-start cycle completes. The controller will continue to try to cycle soft-start indefinitely until the load current is reduced, or the controller is disabled. This operation is shown in Figure 11.

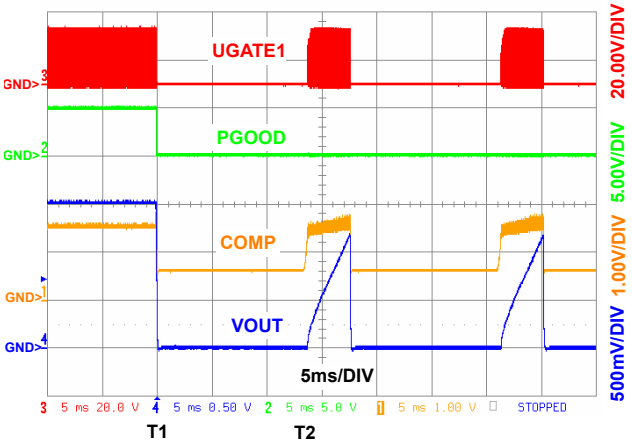


FIGURE 11. ISL8103EVAL1 OVERCURRENT PROTECTION

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL8103 is designed to protect the load from any overvoltage events that may occur (such an overvoltage may occur if for example one of the upper MOSFETs was shorted at assembly due to manufacturing defects). This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the input power supply current limits itself and cuts off. In Figure 12, an artificial pre-POR overvoltage event has been created by shorting the positive 12V input plane to the PHASE plane. This same 12V input is connected to PVCC pins of the ISL8103. Figure 12 illustrates how the controller protects the load from a high output voltage spike, when the 12V input turns on, by tying LGATE to PHASE.

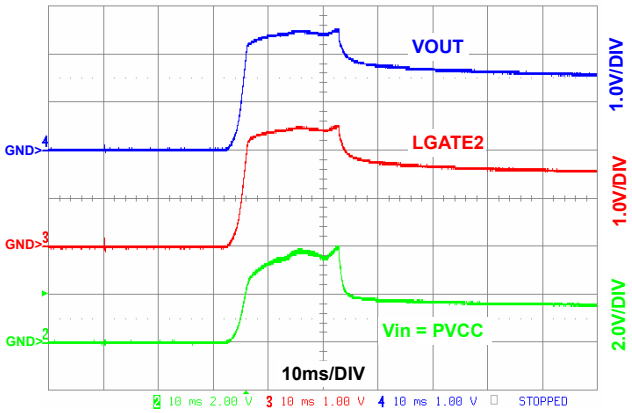


FIGURE 12. ISL8103EVAL1 PRE-POR OUTPUT OVER-VOLTAGE PROTECTION (START-UP WITH SHORTED UPPER FET)

Overvoltage Protection

To protect from an overvoltage event during normal operation, the ISL8103 continually monitors the output voltage. If the output voltage exceeds a specific limit (set internally), the controller commands the LGATE signals high, turning on the lower MOSFETs to keep the output voltage below a level that might cause damage to the Load. As shown in the overvoltage event in Figure 12, turning on the lower MOSFETs not only keeps the output voltage from rising, it also sinks a large amount of current, causing the input voltage to the power stage to drop. If this causes the input power supply voltage to fall below the POR level of the ISL8103, as seen at the end of the waveform in Figure 13, the controller responds by using the pre-POR overvoltage protection explained in the previous section. This allows the ISL8103 to always keep the output load safe from high voltage spikes during an entire overvoltage event.

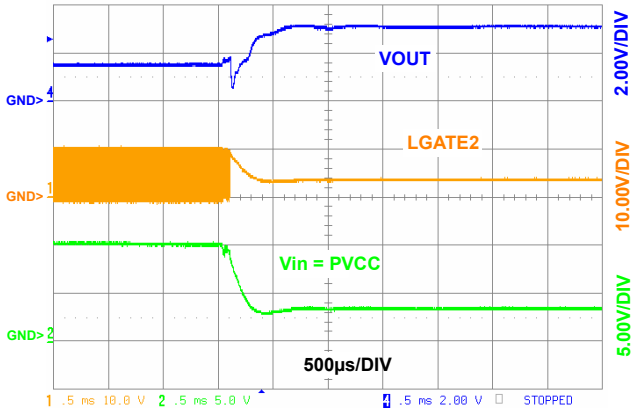


FIGURE 13. ISL8103EVAL1 PRE-POR OVERVOLTAGE PROTECTION

Efficiency

The efficiency of the ISL8103EVAL1 board, loaded from 0A to 90A, at both PVCC = 5V and 12V are plotted in Figure 14 for VOUT = 1.5V. Measurements were performed at room temperature and taken at thermal equilibrium with an air flow of 200LFM. The efficiency peaks just below 89% at 50A for the PVCC = 12V case and then levels off steadily to approximately 86.5% at 90A, while for the PVCC = 5V, efficiency peaks at around 90% at 25A and then falls down to approximately 85% at 90A.

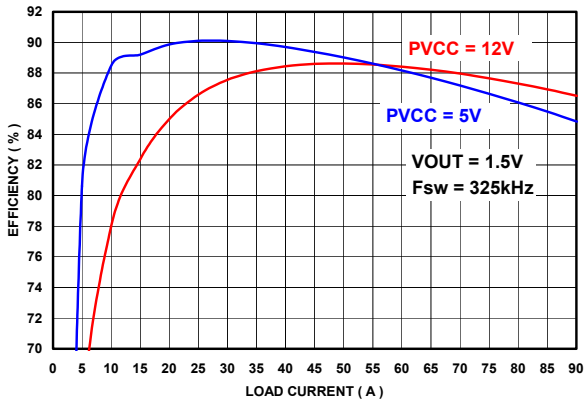


FIGURE 14. EFFICIENCY vs LOAD CURRENT

The efficiency for VOUT = 1.8V is plotted in Figure 15. The efficiency peaks around 90% at 50A for the PVCC = 12V case and then levels off steadily to approximately 88% at 90A, while for the PVCC = 5V, efficiency peaks at around 91% at 30A and then falls down to approximately 87% at 90A. The use of stronger air flow could improve the efficiency across the load range and keeps the components cooler leading to better reliability and longer component lives.

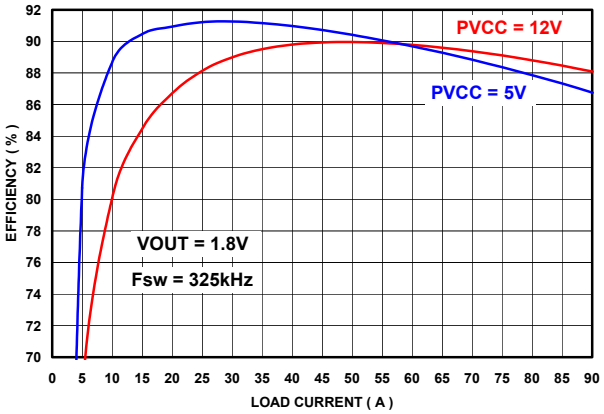


FIGURE 15. EFFICIENCY vs LOAD CURRENT

Modifications

Adjusting the Output Voltage

The output voltage can be adjusted by changing the 2 bit inputs (REF1, REF0) of internal DAC (externally connected with a resistor to REF). Please consult the data sheet for the available voltage ranges and the required settings.

The offset pin (OFS) allows for small-range (less than 100mV), positive or negative, offsetting of the output voltage. The board is shipped with R90 equal to 0Ω and R82 is not populated to provide an output voltage equal to the internal DAC setting. Should an output voltage setting outside the normal range provided via the internal DAC be required, a separate resistor divider connected from the load output terminals to VSEN pin as shown in Figure 16 is needed.

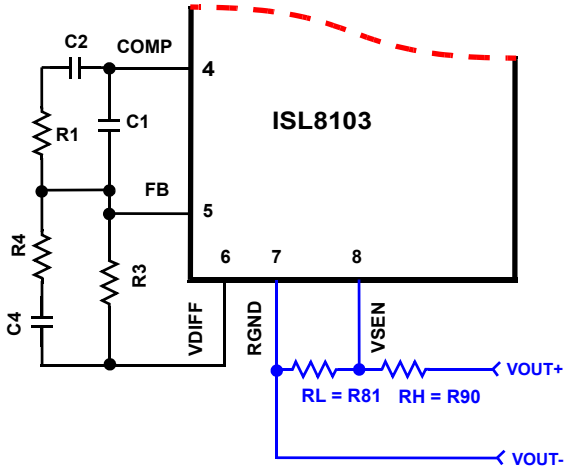


FIGURE 16. ADJUSTING VOUT OUTSIDE THE REF (DAC) RANGE

Use the following relationships to calculate the value of the resistors based on the known parameters.

$$R_L + R_H \leq 500\Omega$$

Choose $R_L = 300\Omega$

Choose a value of VREF that meets the following condition

$$VREF \geq VOUT - 0.8V$$

Choose a value for RL (for example 300Ω)

Calculate the value of the resistor RH

$$R_H = \frac{R_L \cdot (VOUT - REF)}{REF}$$

Example:

VOUT=2.1V

$$VREF \geq 2.1V - 0.8V \geq 1.3V$$

$$VREF = 1.5V$$

$$R_L = 300\Omega$$

$$R_H = \frac{300\Omega \cdot (2.1V - 1.5V)}{1.5V} = 120\Omega$$

Down-Converting From a Different Input Voltage

The ISL8103EVAL1 is powered from bench supplies, the input labelled '+12V' can be adjusted down as desired. If experimenting with a lower voltage, be mindful of a few aspects:

- The duty cycle of the controller is limited to 66%; the circuit will not be capable of properly regulating the output voltage should the input be reduced to a level low enough to induce duty cycle saturation
- As the evaluation board (as shipped) was not optimized for high duty cycle operation, closely monitor the board temperatures and increase the output current only as allowed by the board thermal behaviour
- The reduced input voltage will decrease the amount of loop gain the modulator provides in the feedback loop, as a result, expect a more sluggish transient response when operating the board at reduced down-conversion voltage
- The Evaluation Board (as shipped) have the +12V connected as the input to be down-converted and provides gate drive bias (PVCC). Since PVCC can assume any value between +5 and +12V, the Input can be reduced only to 5V. If a lower input voltage is desired, the PVCC voltage should be provided by a separate supply whose value does not drop below +5V. The VCC bias supply can be used in this case (Consult the section entitled ***PVCC Power Options*** for more details on how this can be accomplished)

Summary

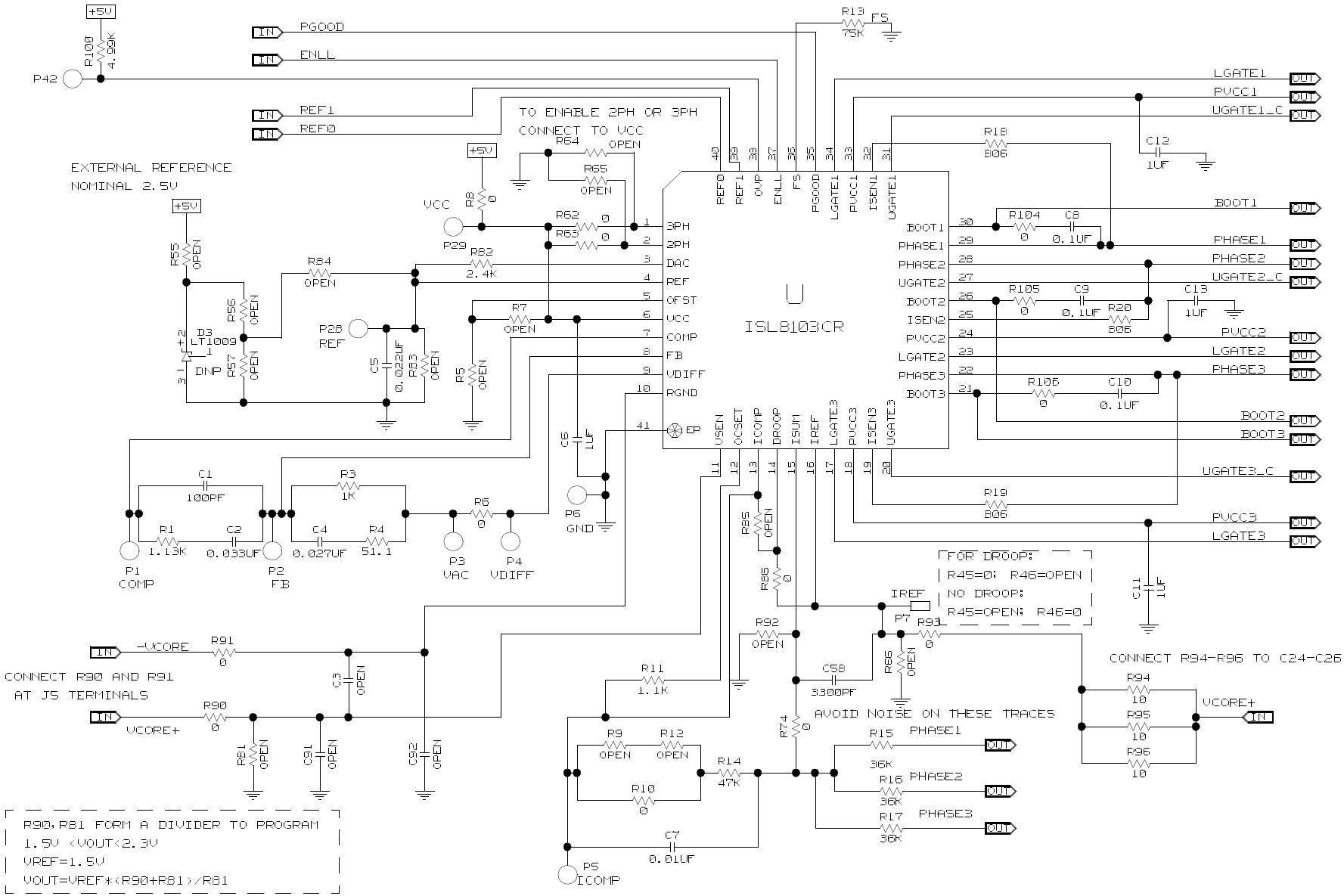
The ISL8103EVAL1 evaluation board showcases a highly integrated approach to providing control in a wide variety of applications. The sophisticated feature set and high-current MOSFET drivers of the ISL8103 yield a highly efficient power conversion solution with a reduced number of external components in a compact footprint. The following pages provide a board schematic, bill of materials and layout drawings to support implementation of this solution.

References

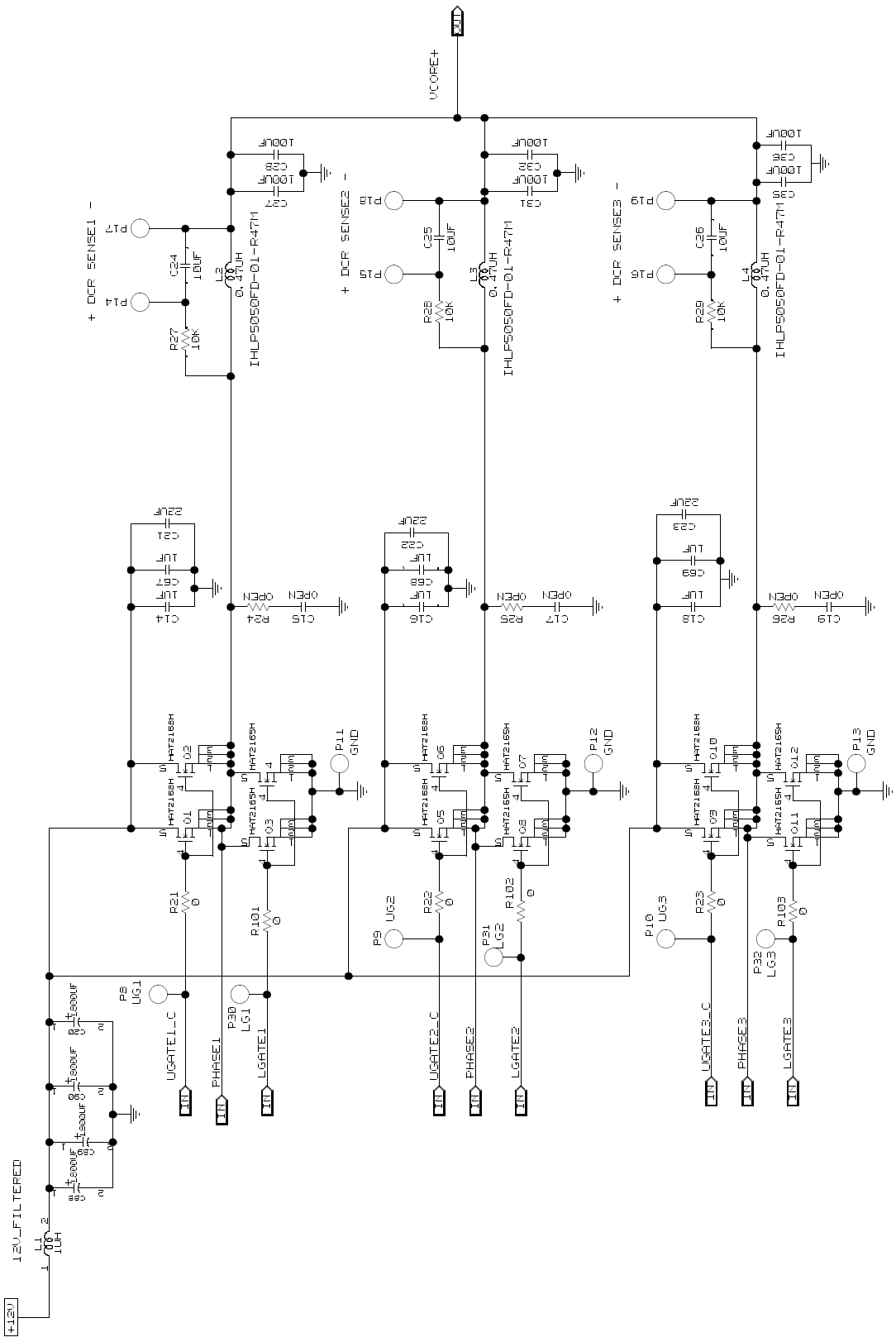
Intersil documents are available on the web at www.intersil.com.

[1] ISL8103 Data Sheet, Intersil Corporation, File No. FN9246.

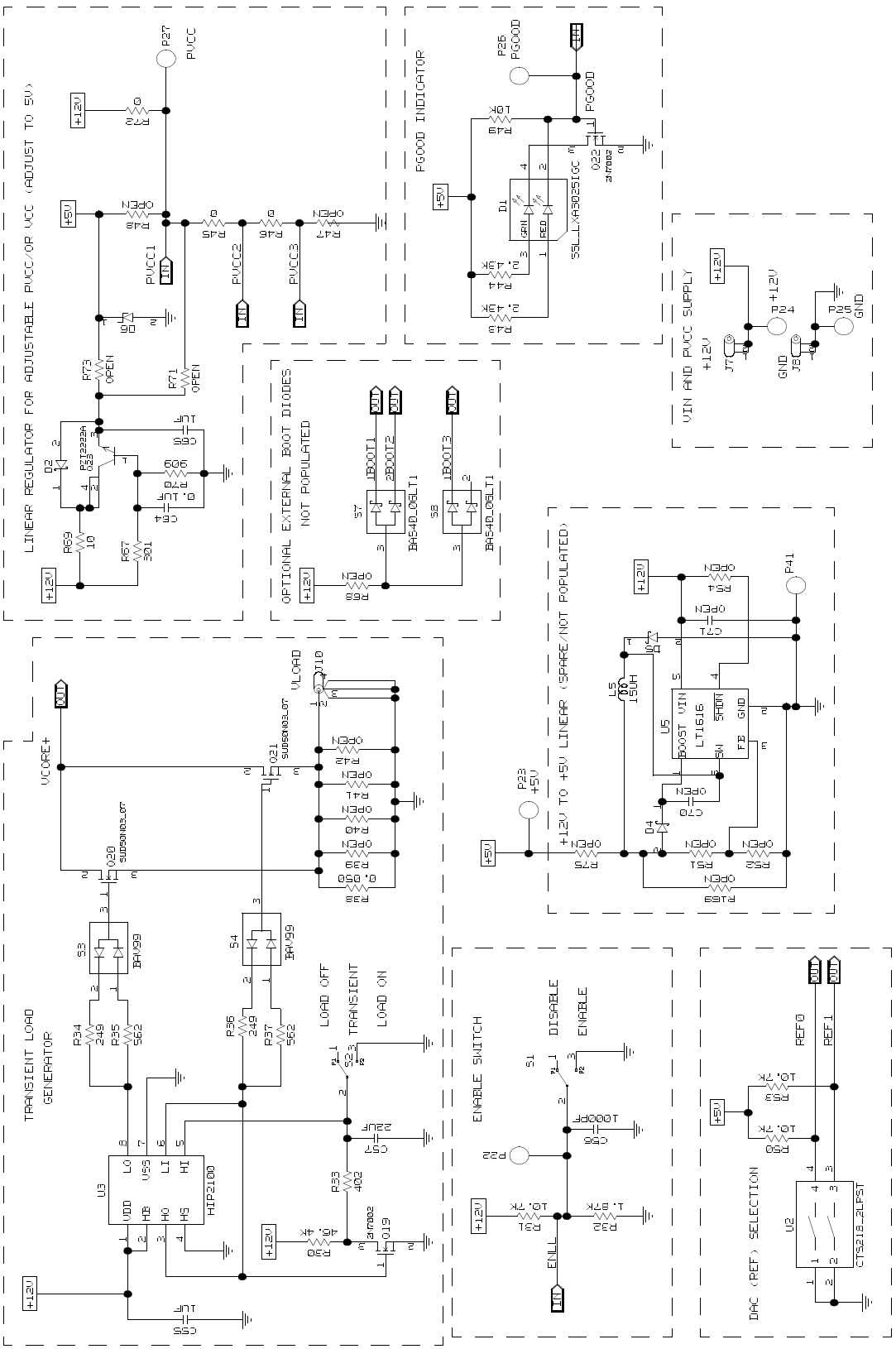
ISL8103EVAL1 Schematic



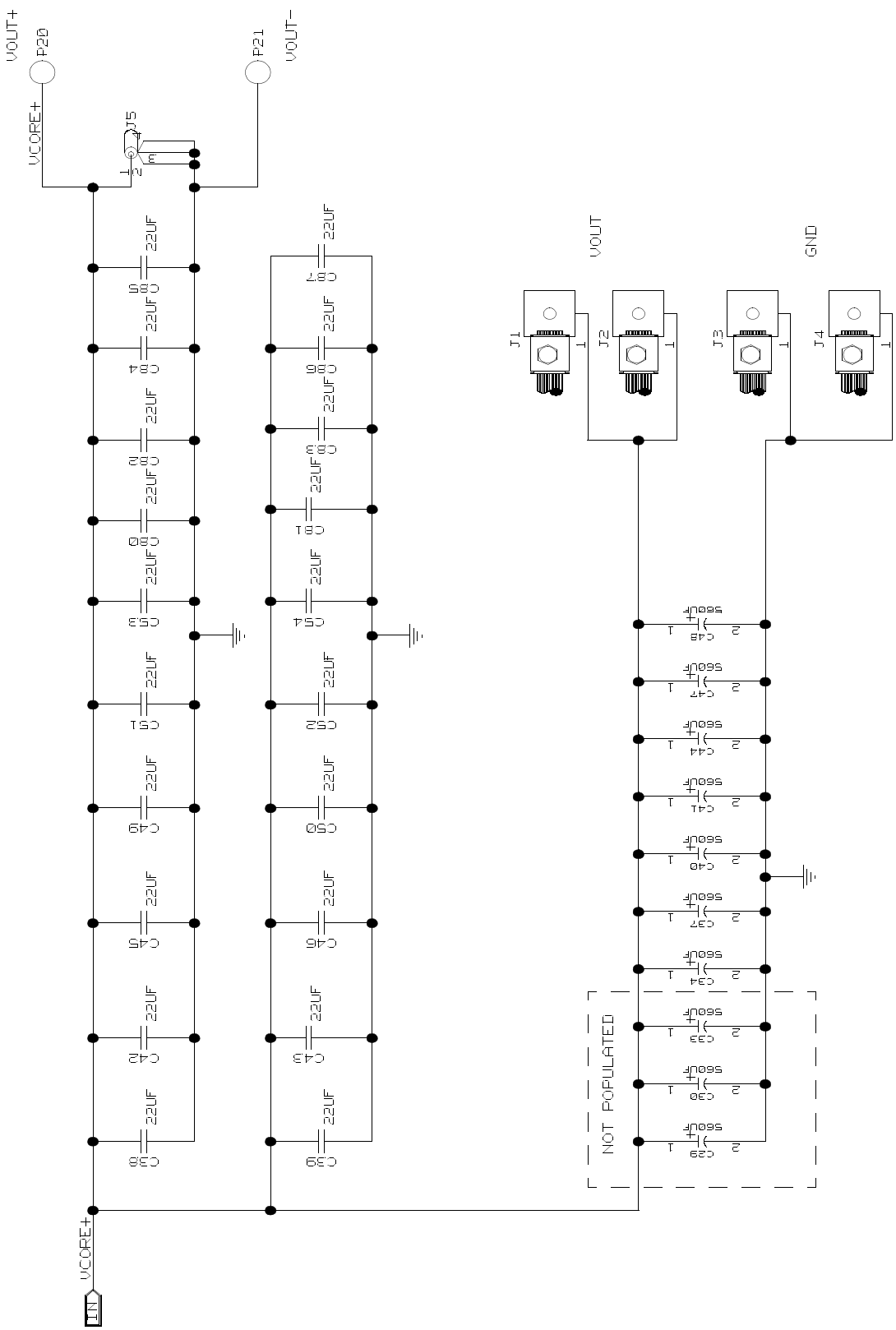
ISL8103EVAL1 Schematic



ISL8103EVAL1 Schematic



ISL8103EVAL1 Schematic



Bill of Materials for ISL8103EVAL1

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	CASE/ FOOTPRINT	MANUF. OR VENDOR	QTY
C34, 37, 40, 41, 44, 47, 48	4SEPC560M	Capacitor, TH, 8x13mm, 560µF, 4V, 20%, 7mΩ	8x13 mm	SANYO	7
DNP (C29, 30, 33)	4SEPC560M	Capacitor, TH, 8x13mm, 560µF, 4V, 20%, 7mΩ	8x13 mm	SANYO	0
C57	C3225X5R1A226M	Ceramic Capacitor, X5R, 10V, 22µF	1210	TDK	1
C56	GRM188R71H102KA ECJ-1VB1H102K C0603X7R500-102KNE	Ceramic Capacitor, X7R,0603, 50V,10%, 1000pF	0603	MURATA PANASONIC VENKEL	1
C58	C0603X7R500-332KNE 0603B332K500BT	CAPACITOR, SMD, 0603, 3300pF, 50V, 10%, X7R	0603	VENKEL BC COMPONENTS	1
C4	0.027µF Ceramic Cap	CAPACITOR, SMD, 0603, 0.027µF, 50V, 10%, X7R	0603	Any	1
C1	ECU-V1H101JCG C0805COG500-101JNE	CAPACITOR, SMD, 0805, 100pF, 50V, 5%, NPO	0805	PANASONIC VENKEL	1
C2	ECJ-1VB1E333K C0603X7R250-33KNE	CAPACITOR, SMD, 0603, 33000pF, 25V, 10%, X7R	0603	PANASONIC VENKEL	1
C7	C0805C103K5RACTU 08055C103KAT2A ECJ-2VB1H103K C0805X7R500-103KNE	CAPACITOR, SMD, 0805, 0.01µF, 50V, 10%, X7R	0805	KEMET AVX PANASONIC VENKEL	1
C8-C10, C64	GRM40X7R104K050AD C0805 1-4K5RAC7800 C0805X74500-104KNE	CAPACITOR, SMD, 0805, 0.1µF, 50V, 10%, X7R	0805	MURATA KEMET VENKEL	4
C65	C0805X7R160-105KNE C0805C105K4RAC	CAPACITOR, SMD, 0805, 1µF, 16V, 10%, X7R	0805	VENKEL KEMET	1
C6, C11-C13	08053D105KAT2A C0805X7R250-105KNE	CAPACITOR, SMD, 0805, 1.0µF, 25V, 10%, X5R	0805	AVX VENKEL	4
C5	ECJ-2VB1H223K C0805X7R500-223KNE	CAPACITOR, SMD, 805, 0.022µF, 50V, 10%, X7R	0805	PANASONIC VENKEL	1
C14, C16, C18, C55, C67, C68, C69	ECJ-3YB1C105K C1206X7R160-105KNE	CAPACITOR, SMD, 1206, 1µF, 16V, 10%, X7R	1206	PANASONIC VENKEL	7
C24-C26	C1206X7R100-106KNE	CAPACITOR, SMD, 1206, 10µF, 10V, 10%, X7R	1206	VENKEL Any	3
C38, C39, C42, C43, C45, C46, C49-C54, C80-C87	22µF Ceramic	CAPACITOR, SMD, 1206, 22µF, 6.3V, 20%, X5R	1206	Any	20
C27, C28, C31, C32, C35, C36	C3225X5R0J107M ECJ-4YB0J107M 12106D107MAT	CAPACITOR, SMD, 1210, 100µF, 6.3V, 20%, X5R	1210	TDK PANASONIC AVX	6
C21-C23	C3225X5R1C226M GRM32ER61C226ME20L	CAPACITOR, SMD, 1210, 22µF, 16V, 20%, X5R	1210	TDK MURATA	2
C20, C88-C90	16MBZ1800M10X23	CAP, RADIAL, 10x23, 1800µF, 16V, 20%, ALUM. ELEC	10x23	RUBYCON PANASONIC	4
DNP (L5)	1008PS-153K	COIL RF INDUC, SMD, 2.74mm, 15µH, 10%, 0.6A		COILCRAFT	0
L2-L4	IHLP-5050FD-01-R47M	COIL-PWR INDUCTOR, SMD, 13mm, 0.47µH, 20%, 55A, SHIELDED		VISHAY	3
J5, J10	131-4353-00	CONN-GEN, SCOPE PROBE TEST PT		Tektronix	2

Bill of Materials for ISL8103EVAL1 (Continued)

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	CASE/ FOOTPRINT	MANUF. OR VENDOR	QTY
P6, P11-P13, P21, P23-P25, P27, P41	1514-2	CONN-GEN, TERMINAL POST, TH, 0.09		KEYSTONE	10
DNP (P40)	11514-2	CONN-GEN, TERMINAL POST, TH, 0.09		KEYSTONE	0
J8	164-6218	CONN-PLUG, BANA-INSUL-SDRLESS, BLK, 4.23mm		MOUSER	1
J7	164-6219	CONN-PLUG, BANA-INSUL-SDRLESS, RED, 4.23mm, RA		MOUSER	1
P1-P5, P7-P10, P14-P20, P22, P26, P28-P32, P42	5002	CONN-GEN, MINI TEST POINT, VERTICAL, WHITE		MOUSER	24
S7, S8	BAS40-06LT1-T	DIODE-SCHOTTKY BARRIER, SMD, SOT-23, 3P, 40V		ON SEMICONDUCTOR	1
S3, S4	BAV99TA-T	DIODE-SWITCHING, SMD, SOT23, 70V, 0.2A		ZETEZX INC	2
D2	MBR0540T1-T	DIODE-RECTIFIER, SMD, SOD-123, 2P, 40V, 0.5A		ON SEMICONDUCTOR	1
DNP (D4, D5)	MBR0540T1-T	DIODE-RECTIFIER, SMD, SOD-123, 2P, 40V, 0.5A		ON SEMICONDUCTOR	0
DNP (D6)	ZMM5231B	DIODE-ZENER, SMD, MINI-MELF, 2 PIN, 5.1V, 500mW			0
D1	SSL-LXA3025IGC-TR	LED, SMD, 3x2.5mm, 4P, RED/GREEN, 12/20MCD, 2V		LUMEX	1
L1	T50-8/90-8T-16AWG-1µH	CORE, RADIAL, TH, 1.0µH, T50-8/90, 8TURNS, 16AWG		Any	1
U3	HIP2100IB	IC-HI FREQ BRIDGE DRIVER, 8P, SOIC, 100V		Intersil	1
U1	ISL8103IRZ	IC-3 PHASE PWM CONTROLLER, 40P, QFN, 6X6, Pb-Free		Intersil	1
Q19, Q22	2N7002-T	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA		Any	2
Q23	CZT3019	TRANSISTOR, NPN, 4P, SOT-223, 120V, 1A		Central Semiconductor	1
Q1, Q2, Q5, Q6, Q9, Q10	HAT2168H	MOSFET, 30V, 8.8mΩ	LFPAK	Renesas	6
Q3, Q4, Q7, Q8, Q11, Q1	HAT2165H	MOSFET, 30V, 3.4mΩ	LFPAK	Renesas	6
Q20, Q21	SUD50N03-07	TRANSIST-MOS, N-CHANNEL, SMD, TO-252, 30V, 20A	DPAK	VISHAY	2
R82	2.4kΩ	Resistor, SMD, 0, 1/16W, 5%	0603	Any	1
R94-R96	10Ω	Resistor, 10Ω, 1/16W, 5%	0603	Any	3
R6	20Ω	Resistor, 20Ω, 1/16W, 5%	0603	Any	1
R10, R45, R46, R62, R63, R74, R86, R90, R91, R93, R104-R106	0Ω	Shorting resistor	0603	Any	13
R3	1kΩ	Resistor, 1kΩ, 1/16W, 1%	0603	Any	1
R1	1.13kΩ	Resistor, 1.13kΩ, 1/16W, 1%	0603	Any	1

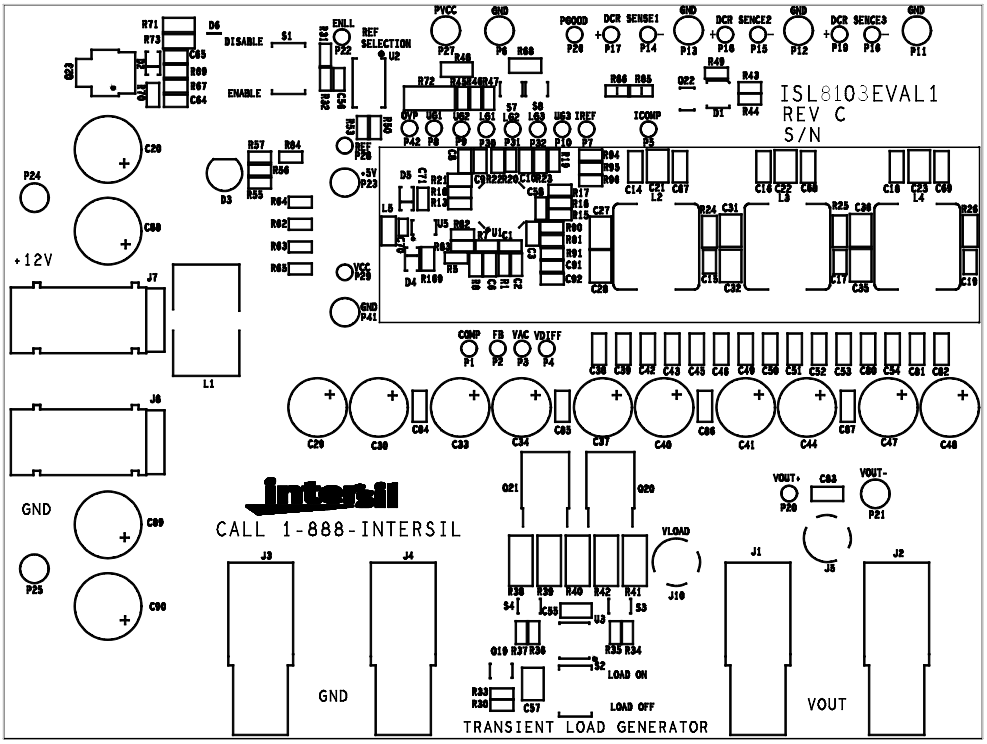
Bill of Materials for ISL8103EVAL1 (Continued)

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	CASE/ FOOTPRINT	MANUF. OR VENDOR	QTY
R27-R29, R49	10kΩ	Resistor, 10kΩ, 1/16W, 1%	0603	Any	4
R31, R50, R53	10.7kΩ	Resistor, 10.7kΩ, 1/16W, 1%	0603	Any	3
R11, R32	1.87kΩ	Resistor, 1.87kΩ, 1/16W, 1%	0603	Any	2
R43, R44	2.43kΩ	Resistor, 2.43kΩ, 1/16W, 1%	0603	Any	1
R34, R36	249Ω	Resistor, 249Ω, 1/16W, 1%	0603	Any	2
R33	402Ω	Resistor, 402Ω, 1/16W, 1%	0603	Any	1
R30	46.4kΩ	Resistor, 46.6kΩ, 1/16W, 1%	0603	Any	1
R14	47kΩ	Resistor, 47kΩ, 1/16W, 1%	0603	Any	1
R100	4.99kΩ	Resistor, 4.99kΩ, 1/16W, 1%	0603	Any	1
R4	51.1Ω	Resistor, 51.1Ω, 1/16W, 1%	0603	Any	1
R35, R37	562Ω	Resistor, 562Ω, 1/16W, 1%	0603	Any	2
R13	75kΩ	Resistor, 75kΩ, 1/16W, 1%	0603	Any	1
R15-R17	36kΩ	Resistor, 36kΩ, 1/16W, 1%	0603	Any	3
R18-R20	806Ω	Resistor, 806Ω, 1/16W, 1%	0603	Any	3
R69	10Ω	Resistor, 10Ω, 1/10W, 1%	0805	Any	1
R8, R21-R23, R101-R103	0Ω	Resistor, 0Ω, 1/10W, 5%	0805	Any	7
R67	301Ω	Resistor, 301Ω, 1/10W, 1%	0805	Any	1
R70	909Ω	Resistor, 909Ω, 1/10W, 1%	0603	Any	1
R72	0Ω	Resistor, 0Ω, 1W, 5%	2512	Any	1
R38	0.05Ω	Resistor, 0.05Ω, 1W, 5%	2512	Any	1
U2	218-2LPST	SWITCH, SMD, 2P, SLIDE, 150M HALF-PITCHGOLD		CTS	1
S1, S2	GT11MSCKE	SWITCH-TOGGLE, SMD, ULTRAMINI, 1P, SPST MINI		C&K	2
J1-J4	KPA8CTP	MTG HDWR, CBL.TERMINAL-LUG & SCREW, 6-14AWG		BERG/FCI	4
C3, C15, C17, C19, C70, C71, C91, C92	DNP				0
R5, R7, R9, R12, R24-R26, R39-R42, R47, R48, R51, R52, R54-R57, R64-R66, R68, R71, R73, R75, R81, R83-R85, R92, R169	DNP				0
DNP (D3)	LT1009CLP	IC-2.5V ADJ. SHUNT REGULATOR, TH, 3P, TO-92	TO-92	TI	0
DNP (U5)	LT1616ES6	IC-SWITCHING REGULATOR, 6P, SOT23, 0.6A	SOT23	Linear Tech	

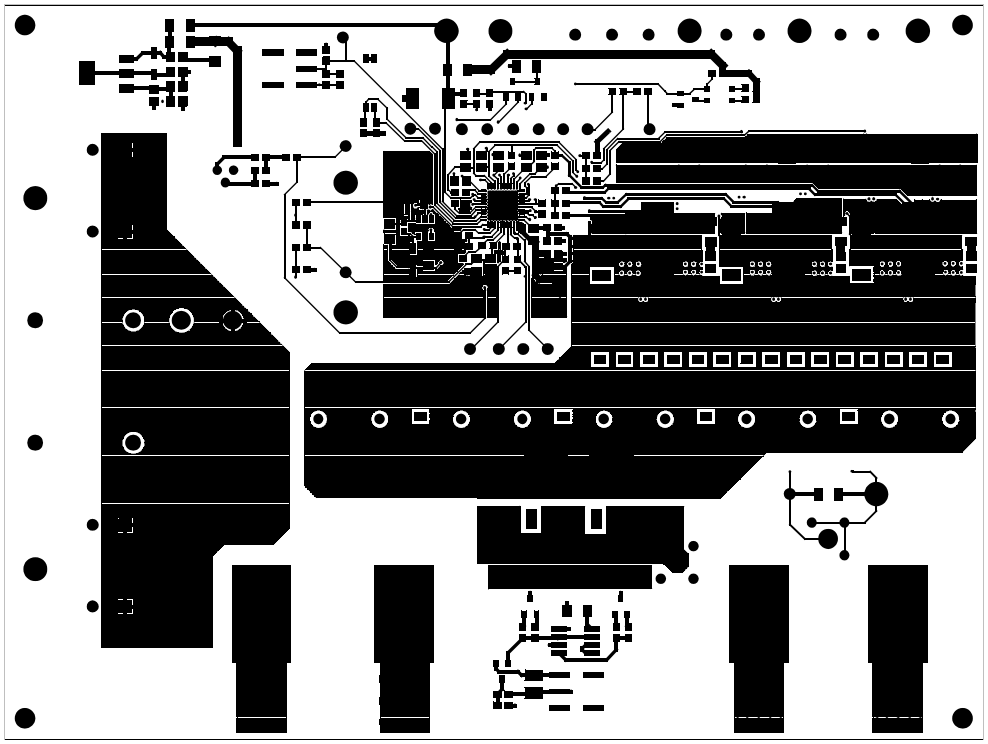
NOTE: DNP means do not populate

ISL8103EVAL1 Layout

TOP SILK SCREEN

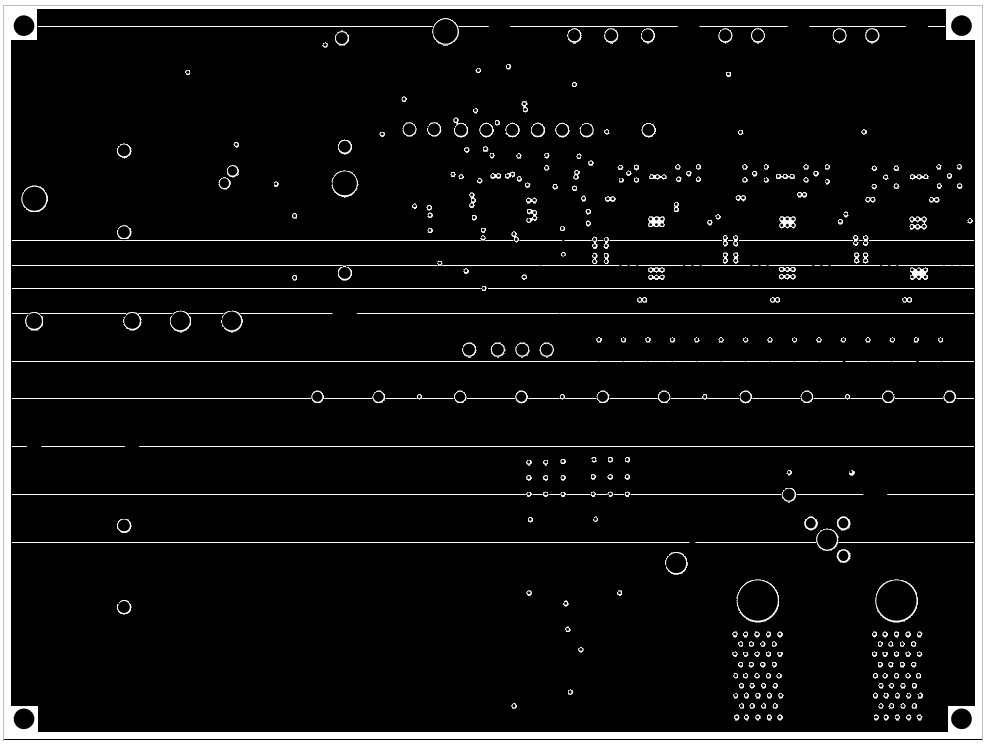


TOP LAYER (1st)

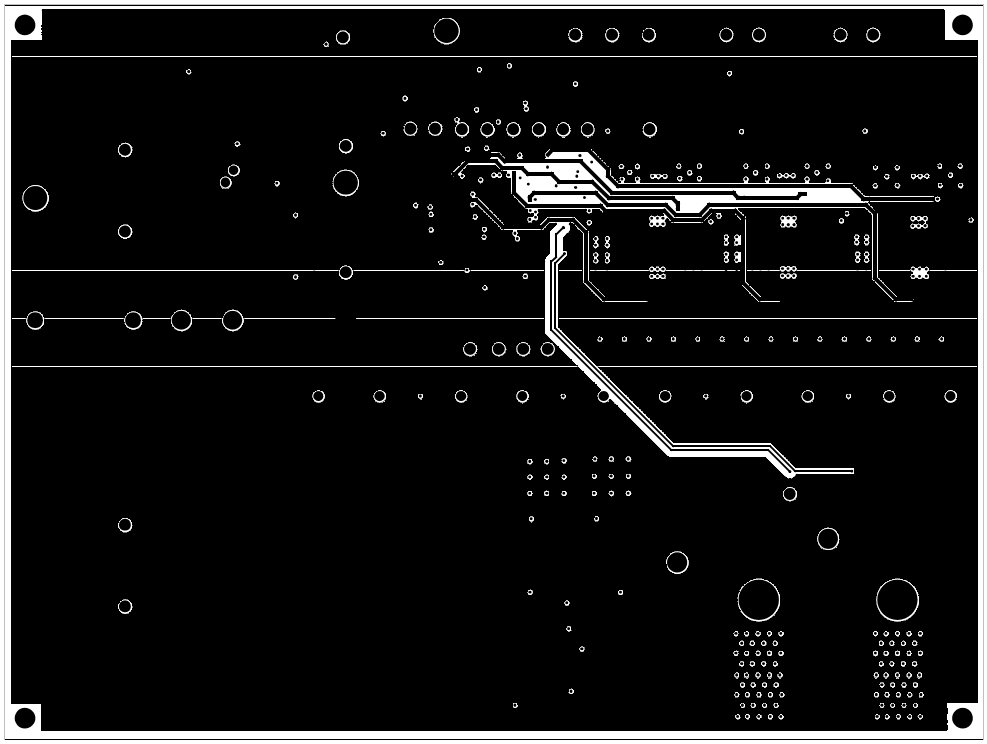


ISL8103EVAL1 Layout (Continued)

GROUND LAYER (2nd)

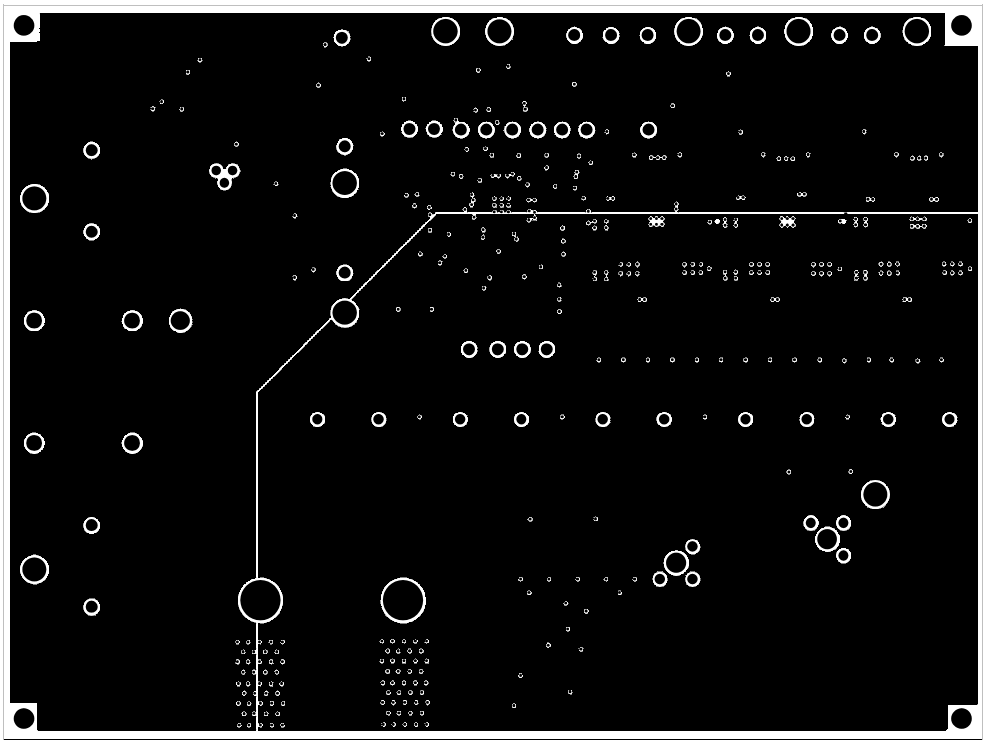


GND/SIGNAL LAYER (3rd)

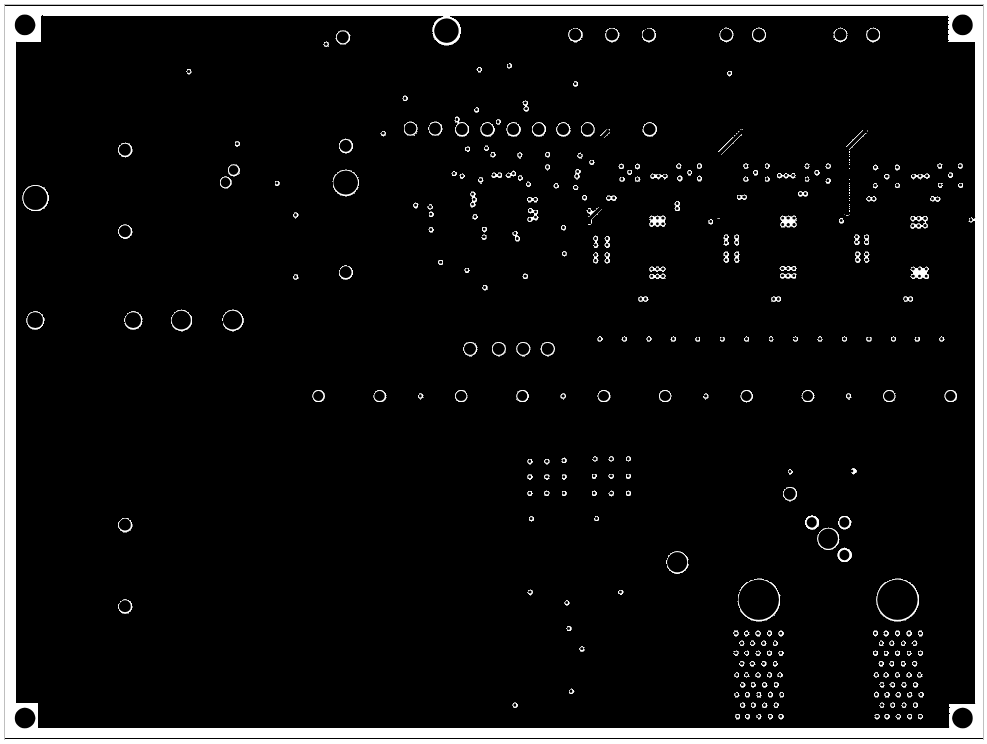


ISL8103EVAL1 Layout (Continued)

POWER LAYER (4th)

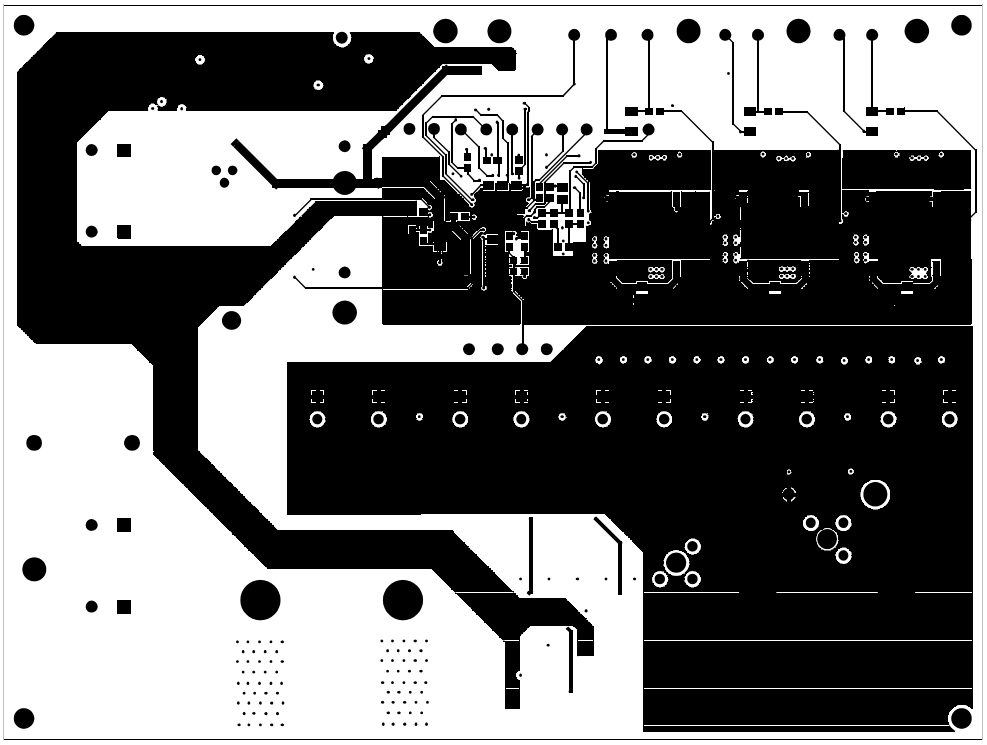


GND LAYER (5th)



ISL8103EVAL1 Layout (Continued)

POWER/SIGNAL LAYER (6th)



BOTTOM SILK SCREEN