

ISL9440AMGTHEVAL1Z - Power Module User Guide

Introduction

The ISL9440AMGTHEVAL1Z is Intersil's high performance, cost-effective power module for Xilinx's high speed GTH serial transceivers on Virtex-6 HXT Characterization Boards. Utilizing the popular [ISL9440A](#) and [ISL8009A](#) for the power stage, the module also features quad-DCP [ISL22346](#) for set point adjustment. Sequencing is achieved using Intersil's dual voltage monitor [ISL88012](#).

This user guide is intended to serve as a manual for using the ISL9440AMGTHEVAL1Z power module and also list its various performance characteristics.

Key Features

The ISL9440AMGTHEVAL1Z power module uses the three channel buck controller and single linear controller ISL9440A for generating voltage rails MGTHAVCC, MGTHAVCCRX and MGTHAVCCPLL. MGTHAVTT is generated using the tiny integrated FET regulator ISL8009A. Switching at 600kHz, the ISL9440A reduces output inductor and capacitor requirements. The ISL8009A integrates upper and lower power MOSFETs and switches at 1.6MHz, reducing external component requirements even further. Table 1 lists the specifications of each rail.

Voltage margining on all the output rails is achieved by changing the equivalent feedback resistor divider setting using the I²C bus controlled quad-Digitally Controlled Potentiometer (DCP) ISL22346.

The power module achieves excellent regulation by remotely sensing the output voltage close to its load. Figure 1 shows the block diagram implementation of the power module.

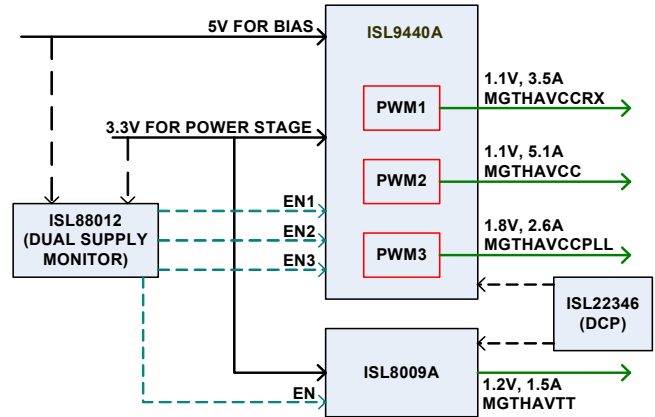


FIGURE 1. ISL9440AMGTHEVAL1Z BLOCK DIAGRAM

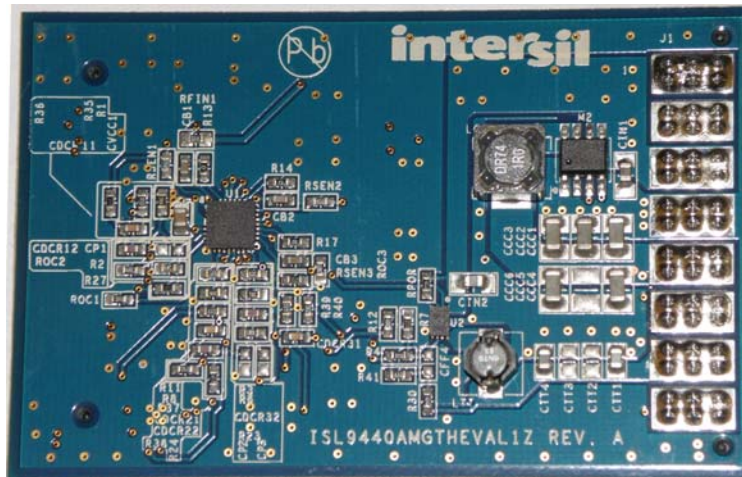


FIGURE 2. ISL9440AMGTHEVAL1Z TOP VIEW

TABLE 1. POWER MODULE PARAMETERS

PARAMETER	MGTHAVCC	MGTHAVCCRX	MGTHAVTT	MGTHAVCCPLL
Output Voltage	1.1V ±1%	1.1 ±1%	1.2 ±1%	1.8 ±1%
Rated Current	5.5A	4A	1.5A	3.2A
Peak to Peak Ripple	<10mV	<10mV	<10mV	<10mV

Please contact Intersil Marketing for ordering this power module.

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TABLE 2. ADDRESS BYTE AND VALUE OF WIPER REGISTER FOR MARGINING

OUTPUT RAIL	ADDRESS (HEX)	DEFAULT VALUE (HEX)	WR FOR -10% MARGINING (HEX)	WR FOR -5% MARGINING (HEX)	WR FOR +5% MARGINING (HEX)	WR FOR +10% MARGINING (HEX)	WR FOR +15% MARGINING (HEX)
MGTHARX	00	5D	6E	66	52	4A	42
MGTHAVCC	01	5D	6E	66	52	4A	42
MGTHAVCCPLL	10	37	5A	48	29	1B	0F
MGTHAVTT	11	56	6E	62	4C	43	39

Voltage Margining Using DCP

The ISL22346 is a quad-DCP that allows changing the center tap position by writing an 8-bit word into its Wiper Position (WP) register through the I²C bus. Changing the center tap position of DCP changes the equivalent feedback resistor divider and results in a change in output voltage.

The DCP can be identified via the I²C byte 'A0'. Please refer to the part datasheet for description of the I²C bus. Table 2 lists the specific address for each output rail. It also lists the typical value of the wiper register for each rail to achieve margining. Margining is fairly linear between the values shown.

Sequencing Using ISL88012

The power module uses the 5V input rail to bias the ISL9440A. The 3.3V input rail is used as input voltage for power conversion. The ISL88012 is a dual voltage monitor that signals a logic high when both the 5V and the 3.3V rails have started up. Subsequent RC circuits are used to generate delays on 'Enable' of each individual output rail to give the following start-up sequence:

1. MGTHAVCC powers up first.
2. MGTHAVCCRX powers up within 1ms of MGTHAVCC.
3. MGTHAVTT and MGTHAVCCPLL delayed relative to MGTHAVCC and MGTHAVCCRX by a minimum of 10 μ s.

Figure 3 shows a typical start-up waveform.

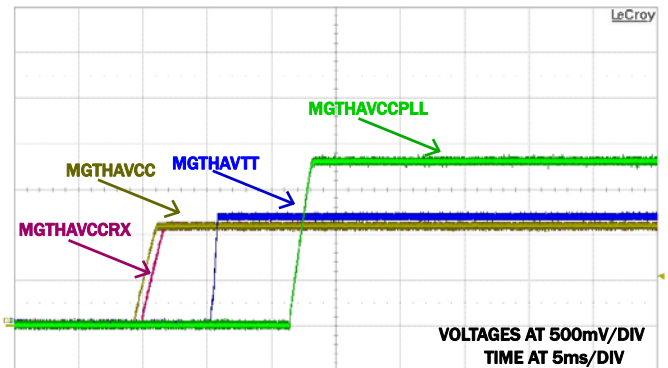


FIGURE 3. START-UP SEQUENCE

Protection Features

All the output rails feature overcurrent protection. Please refer to ISL9440A and ISL8009A datasheets for specific overcurrent protection mechanisms. The ISL9440A also has output over voltage protection. Both the controllers feature built-in thermal protection.

In the event remote sense feedback from control connector J2 is lost, the module will not get damaged. In fact, all the output rails of the power module continue good voltage regulation under such an event. This is achieved via a redundant internal feedback path.

Typical Performance Curves

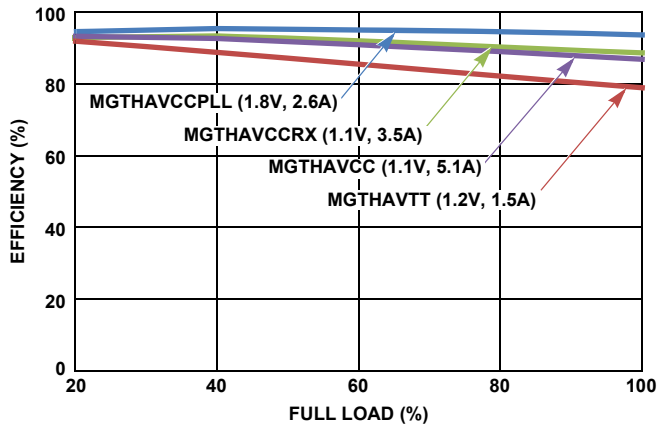


FIGURE 4. EFFICIENCY vs LOAD CURRENT

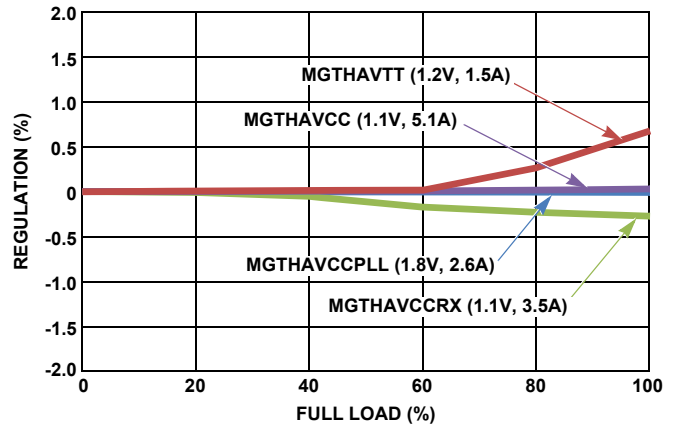


FIGURE 5. LOAD REGULATION

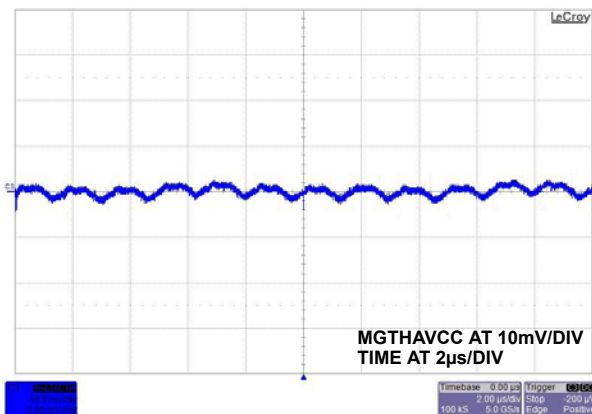


FIGURE 6. MGTHAVCC OUTPUT RIPPLE (LOAD = 5.1A)

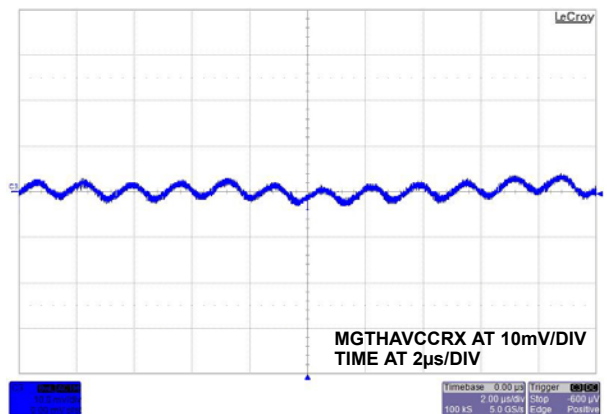


FIGURE 7. MGTHAVCCRX OUTPUT RIPPLE (LOAD = 3.5A)

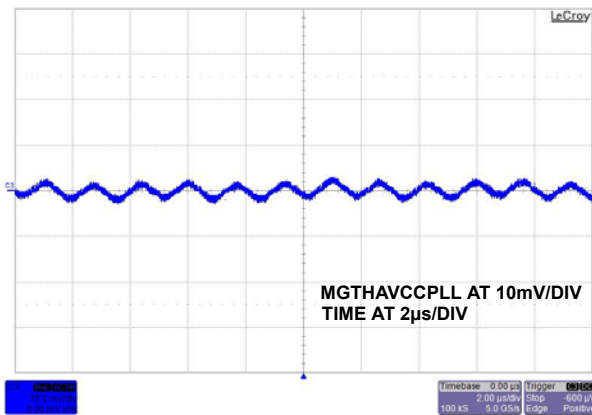


FIGURE 8. MGTHAVCCPLL OUTPUT RIPPLE (LOAD = 2.6A)

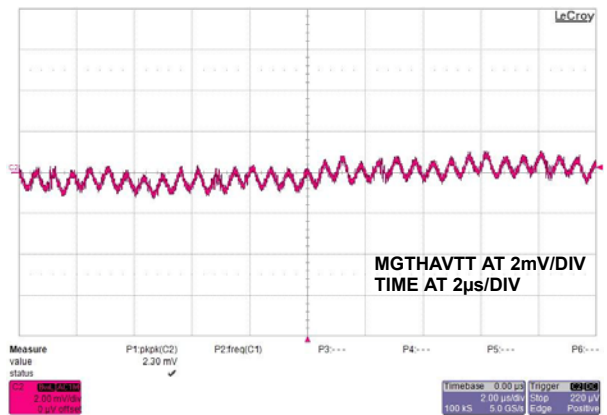
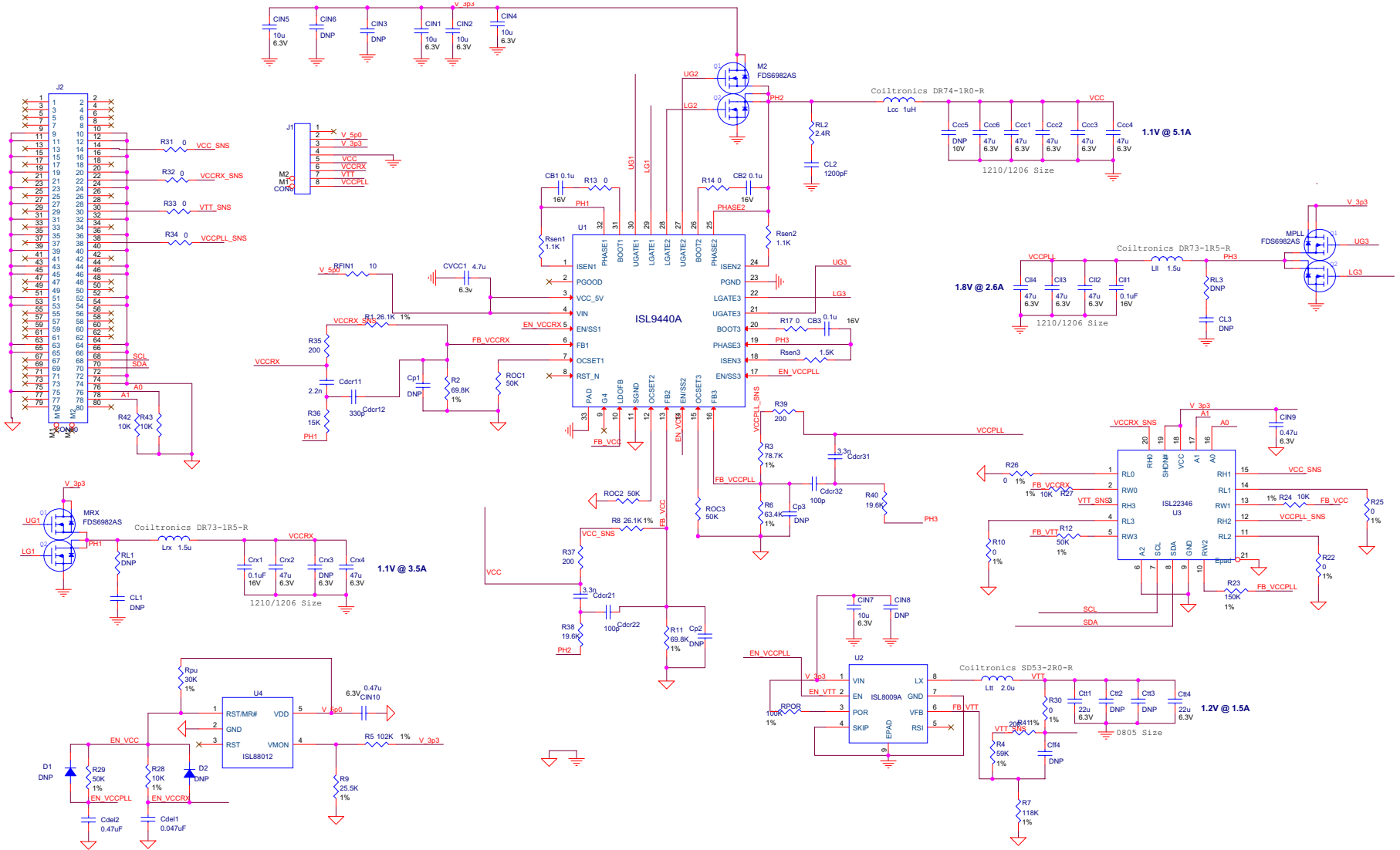


FIGURE 9. MGTHAVTT OUTPUT RIPPLE (LOAD = 1.5A)

Schematic



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TABLE 3. BILL OF MATERIALS

ITEM	QTY	PART REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
1	1	Cdcr32	100pF	100pF; 50V; NPO, SMD, 0603	TDK	C1608C0G1H101J
2	2	Cdcr12, Cdcr22	330pF	330pF; 50V; NPO, SMD, 0603	TDK	C1608C0G1H331J
3	5	CB1, CB2, CB3, Crx1, CII1	0.1µF	0.1µF; 50V; X7R; SMD; 0603	TDK	C1608X7R1H104K
4	1	CL2	1200pF	1200pF; 50V; X7R; SMD; 0603	TDK	C1608X7R1H122K
5	1	Cdcr31	3300pF	3300pF; 50V; X7R; SMD; 0603	TDK	C1608X7R1H332K
6	2	Cdcr11, Cdcr21	2200pF	2200pF; 50V; X7R; SMD; 0603	TDK	C1608X7R1H222K
7	1	Cdel1	0.047µF	0.047µF; 50V; X7R; SMD; 0603	TDK	C1608X7R1H473K
8	3	CIN9, CIN10, Cdel2	0.47µF	0.47µF; 50V; X7R; SMD; 0603	TDK	C1608X7R1H474K
9	5	CIN1, CIN2, CIN4, CIN5, CIN7	10µF	10µF; 10V; X5R; SMD; 0805	TDK	C2012X5R1A106K
10	2	Ctt1, Ctt4	22µF	22µF; 6.3V; X5R; SMD; 0805	TDK	C2012X5R1A226K
11	1	CVCC1	4.7µF	4.7µF; 6.3V; X5R; SMD; 0805	TDK	C2012X5R0J475K
12	10	Crx2, Crx4, Ccc1-Ccc4, Ccc6, CII2, CII3, CII4	47µF	47µF; 6.3V; X5R; SMD; 1206	TDK	C3216X5R0J476M
13	2	LLL, LRX	1.5µH	Inductor	Coiltronics	DR73-1R5-R
14	1	LCC	1.0µH	Inductor	Coiltronics	DR74-1R0-R
15	1	LTT	2.0µH	Inductor	Coiltronics	SD53-2R0-R
16	1	U3		Quad-DCP	Intersil	ISL22346UFRT20Z
17	1	U2		Integrated FET Regulator	Intersil	ISL8009AIRZ
18	1	U4		Dual Voltage Monitor	Intersil	ISL88012IH546Z
19	1	U1		Three Channel Buck and One Linear Regulator Controller	Intersil	ISL9440AIRZ
20	3	MRX, M2, MPLL		N-Channel MOSFET	Fairchild	FDS6982AS
21	4	R35, R37, R39, R41	200Ω	Resistor, SMD, 0603, 1%		
22	1	RL2	2.4Ω	Resistor, SMD, 0603, 1%		
23	12	R10, R13, R14, R17, R22, R25, R26, R30, R31, R32, R33, R34.	0Ω	Resistor, SMD, 0603, 1%		
24	5	R24, R27, R28, R42, R43	10kΩ	Resistor, SMD, 0603, 1%		
25	1	RPOR	100kΩ	Resistor, SMD, 0603, 1%		
26	1	R5	102kΩ	Resistor, SMD, 0603, 1%		
27	2	RSEN1, RSEN2	1.1kΩ	Resistor, SMD, 0603, 1%		
28	1	R7	118kΩ	Resistor, SMD, 0603, 1%		
29	1	RSEN3	1.5kΩ	Resistor, SMD, 0603, 1%		
30	1	R36	15kΩ	Resistor, SMD, 0603, 1%		
31	1	R23	150kΩ	Resistor, SMD, 0603, 1%		
32	2	R38, R40	19.6kΩ	Resistor, SMD, 0603, 1%		
33	1	R9	25.5kΩ	Resistor, SMD, 0603, 1%		
34	2	R1, R8	26.1kΩ	Resistor, SMD, 0603, 1%		
35	1	Rpu	30kΩ	Resistor, SMD, 0603, 1%		

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TABLE 3. BILL OF MATERIALS (Continued)

ITEM	QTY	PART REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
36	5	R12, R29, ROC1, ROC2, ROC3	49.9k Ω	Resistor, SMD, 0603, 1%		
37	1	R4	59k Ω	Resistor, SMD, 0603, 1%		
38	1	R6	63.4k Ω	Resistor, SMD, 0603, 1%		
39	2	R2, R11	69.8k Ω	Resistor, SMD, 0603, 1%		
40	1	R3	78.7k Ω	Resistor, SMD, 0603, 1%		
41	1	RFIN	10 Ω	Resistor, SMD, 0603, 1%		
42	1	J2		Signal Connector	Samtec	BSE-040-01-L-D-A
43	1	J1		Power Connector	Samtec	MPS-08-7.70-01-L-V

ISL9440AMGTHEVAL1Z PCB Layout

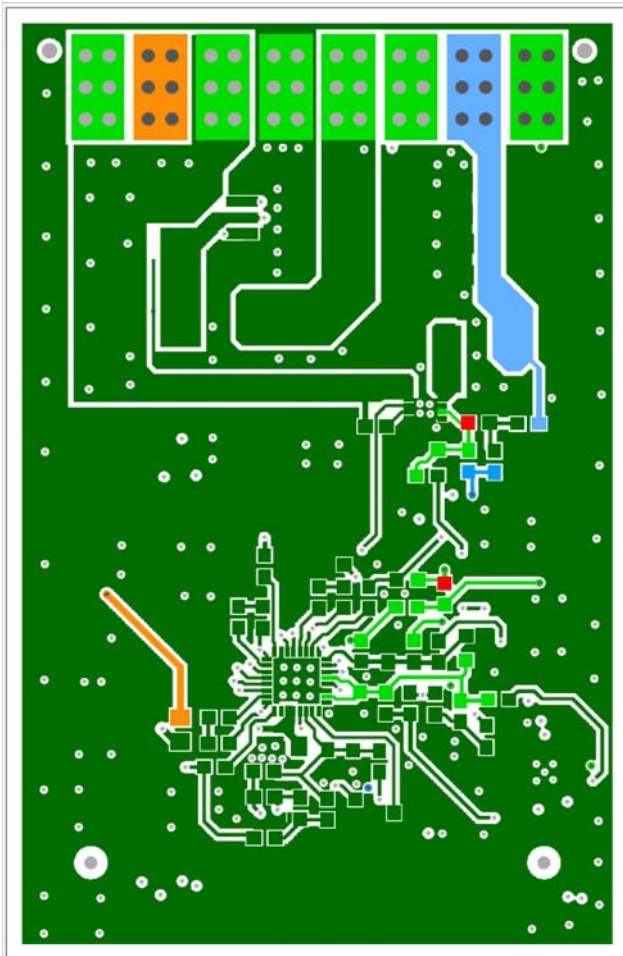


FIGURE 10. TOP LAYER

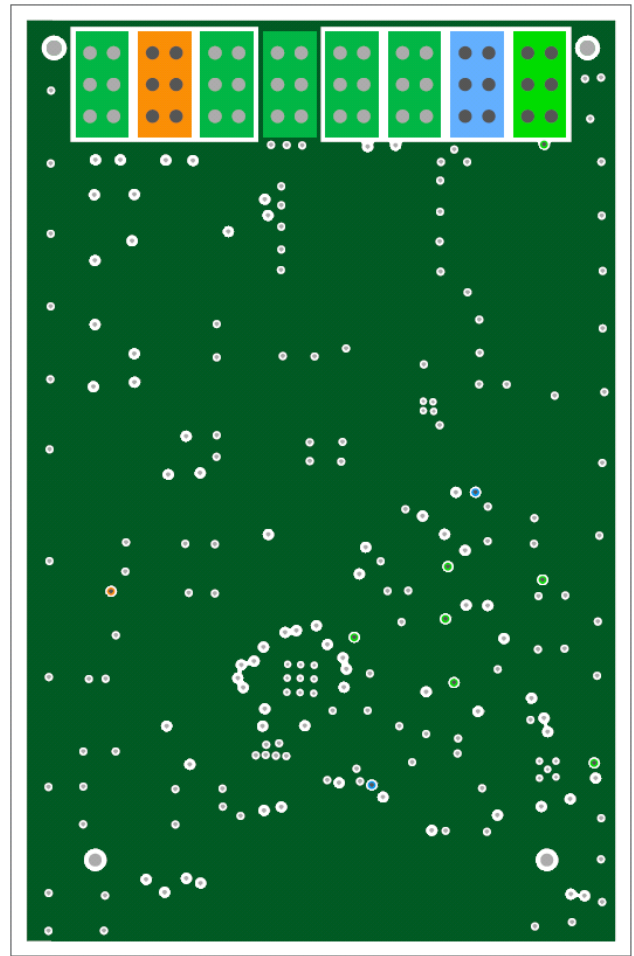


FIGURE 11. SECOND LAYER (SOLID GROUND)

ISL9440AMGTHEVAL1Z PCB Layout (Continued)

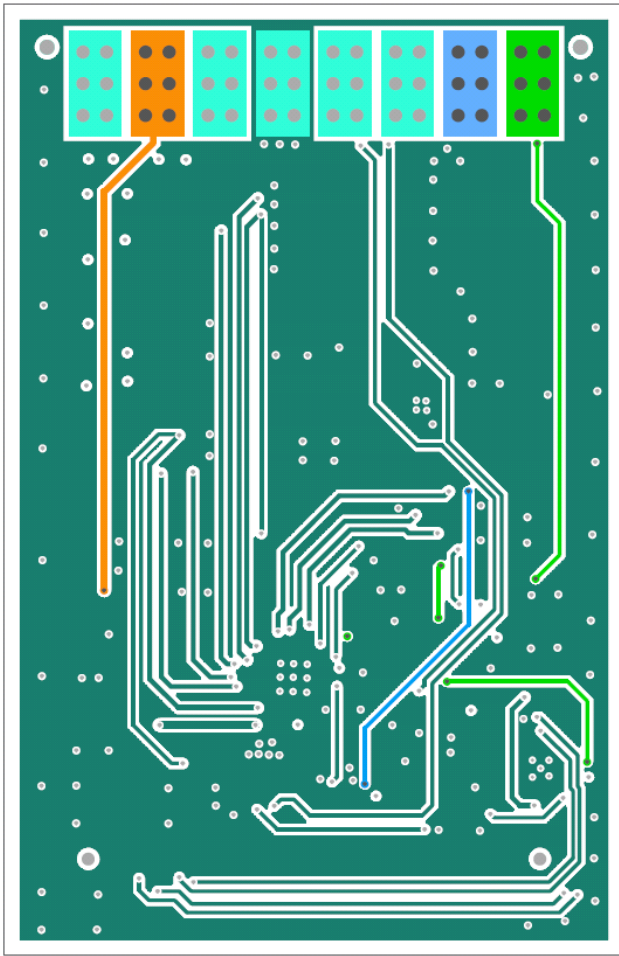


FIGURE 12. THIRD LAYER

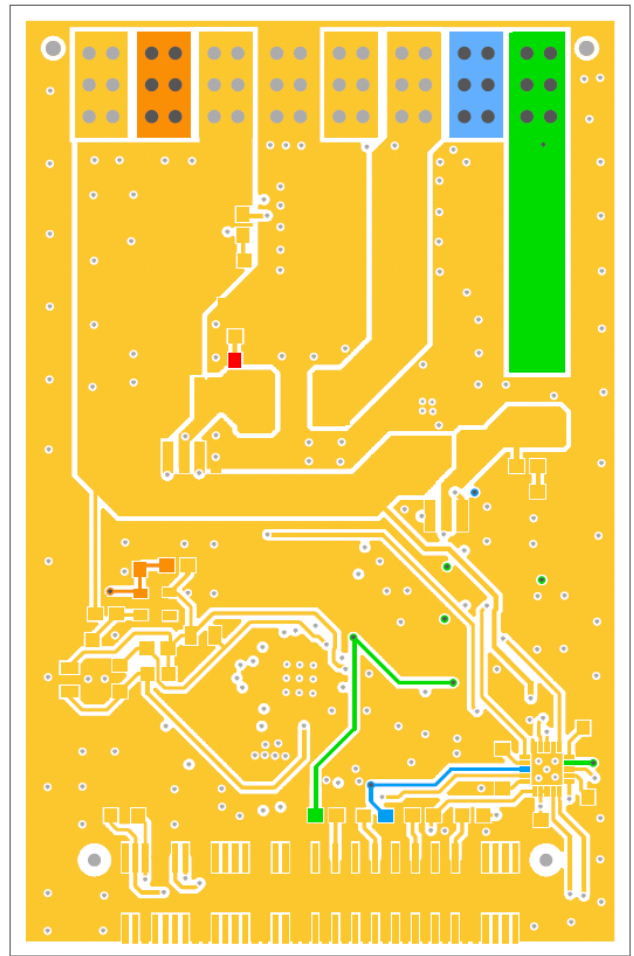


FIGURE 13. BOTTOM LAYER

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