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User's Manual

SH7670 CPU Board
M3A-HS71

User's Manual

Renesas 32-Bit RISC Microcomputers
SuperH™ RISC engine Family / SH7670 Series

Renesas Electronics
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M3A-HS71 SCHEMATICS

Chapter1
Overview

1.1 Overview

The SH7670 CPU board is a CPU evaluation board designed for users to evaluate the functionality and performance of the SH7670 group of Renesas Technology original microcomputers, as well as develop and evaluate the application software for this group of microcomputers. The features of the SH7670 evaluation board are as follows.

Board Part Number: M3A-HS71

<The Features of SH7670 CPU Board>

- As external memories, a 64MB (8 Mbytes) flash memory (16-bit bus connection), two 256MB (32 Mbytes) SDRAMs (32-bit bus connection) are mounted.
- As the SH7670 peripheral function interface, a USB connector, LAN connector are standard mounted. In addition, the general purpose 20-pin MIL standard connector is also installed as the connector for MPEG transport stream interface (STIF).
- All pins of SH7670 data bus, address bus, and on-chip peripheral functions are connected to the extension connector. (For extension board and monitoring signals with using measurement instruments)
- The on-chip emulator E10A-USB made by Renesas Technology (with no AUD function: 14-pin connector) can be used.

1.2 Configuration

Figure 1.2.1 shows an example of system configuration using the SH7670 CPU board.

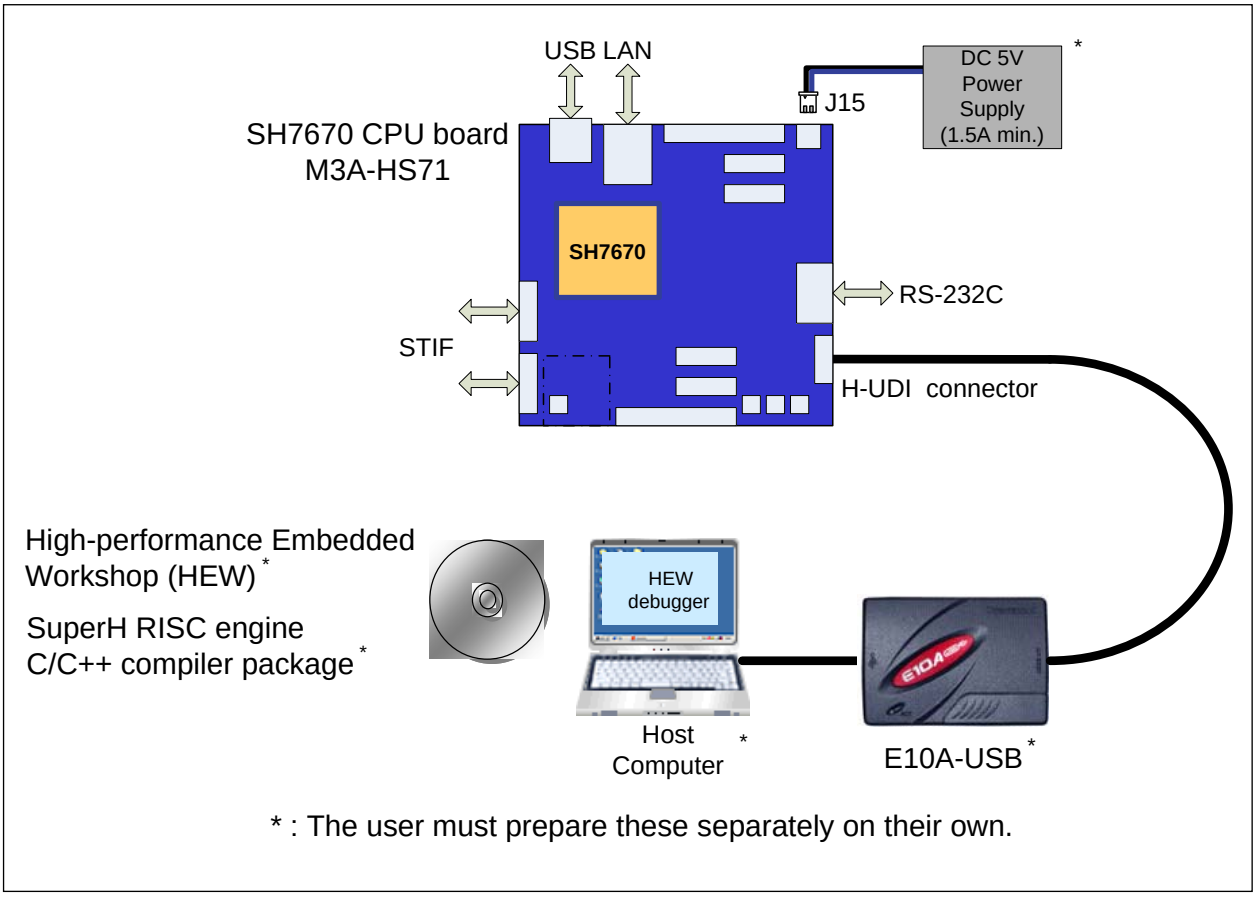


Figure 1.2.1 SH7670 CPU Board System Configuration Example

1.3 External Specifications

Table 1.3.1 and Table 1.3.2 list the external specifications of SH7670 CPU board.

Table 1.3.1 External Specifications of SH7670 CPU Board (1)

No.	Item	Content
1	CPU	SH7670 ● Input(XIN) clock: 16.67 MHz ● Bus clock: Maximum 66.67 MHz, ● CPU clock: Maximum 200 MHz ● On-chip memory • RAM: 32KB • Instruction cache : 8 KB • Operand cache : 8 KB Power voltage: internal : 1.2 V, I/O 3.3 V 256-pin BGA 0.8 mm pitch (Package code: PRBG0256GA-A)
2	External Memory	The following memories are mounted ● SDRAM • EDS2516APTA-75 (Elpida) x 2 : 64 MB • 32-bit bus width ● Flash memory • S29GL064A90TFIR4 : 8 MB • 16-bit data bus width fixed ● EEPROM (IIC3) ・HN58X24128FPIE x 1 : 16KB
3	Ether	● RJ-45LAN connector with on-chip pulse transformer (8-pin, RJ-45) ● Realtek PHY-LSI RTL8201CP-VD-LF is mounted
4	USB	● USB connector →Series A socket built-in. (Mini-AB/Mini-B connectors for Host/Function evaluation can be mounted on the board) ● VBUS power control
5	Connectors and Through-hole	● H-UDI connector (14-pin) ● Serial port connector (D-sub 9-pin) ● 20-pin MIL standard connector • SH7670 extension connector: 4 pcs. • SH7670 ST I/F connector : 2 pcs. ● 40-pin MIL standard connector • SH7670 extension connector: 2 pcs.
6	LED	● Power LED (1 pc.) ● User LED (Connect to the port pins of SH7670): 4 pcs. ● LED for Ethernet communication status (5 pcs.)

Table 1.3.2 External Specifications of SH7670 CPU Board (2)

No.	Item	Content
7	Switch	● Reset switch: 1 pc. ● NMI switch: 1 pc. ● IRQ0 switch: 1 pc. ● Test switch: 1 pc. ● DIP switch for mode setting: 1 pc. (5-pole) ● DIP switch for user: 1 pc. (4-pole) ● Switch for PHY controller operation mode : 1 pc. (6-pole)
8	Board Size	● Dimensions : 145mm x 150mm ● Mounting form : 4-layer, double-side mounted ● Board configuration : 1 board

1.4 Block Diagram of SH7670 CPU Board

Figure 1.4.1 shows the system block diagram of SH7670 CPU board.

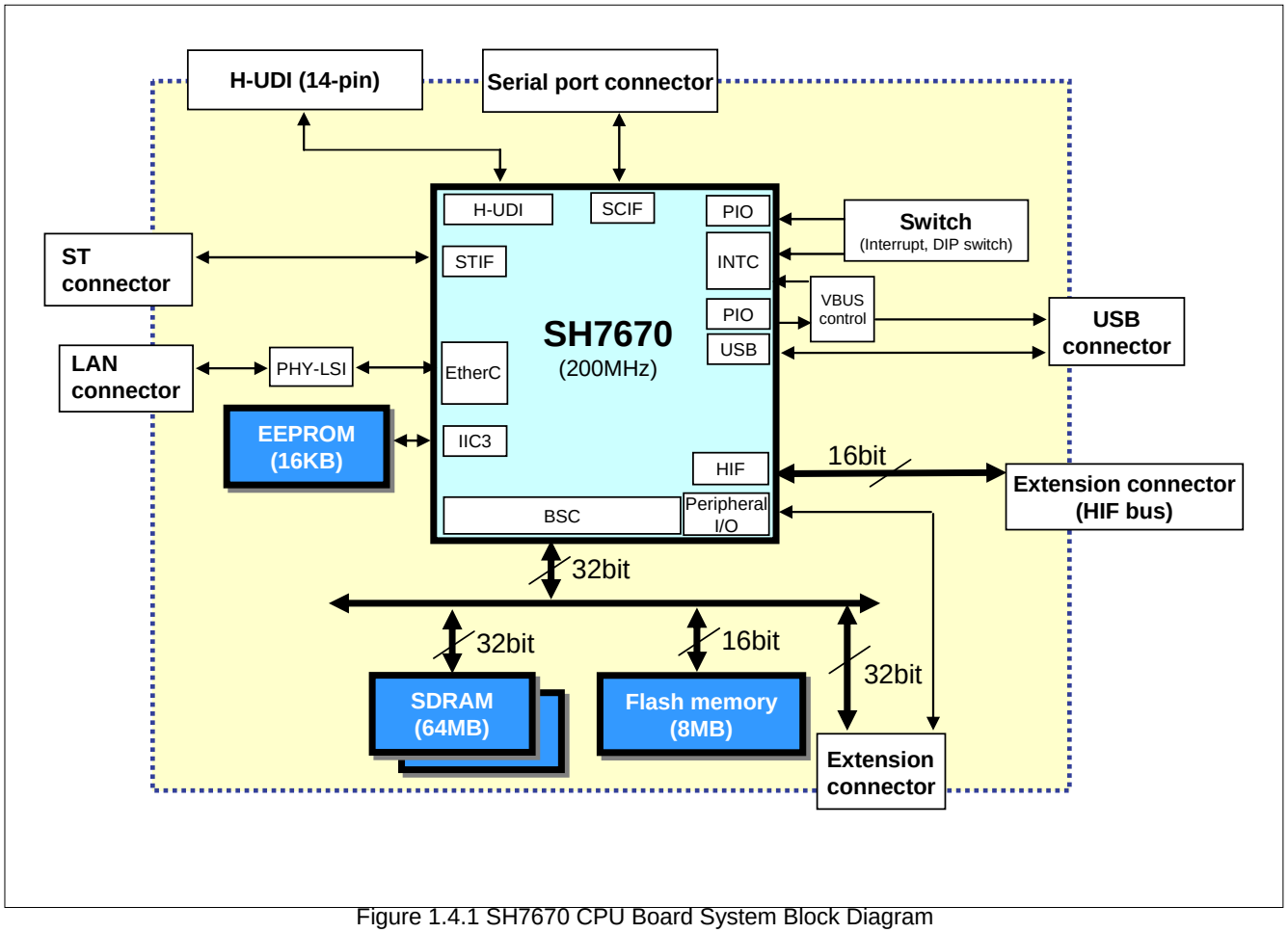
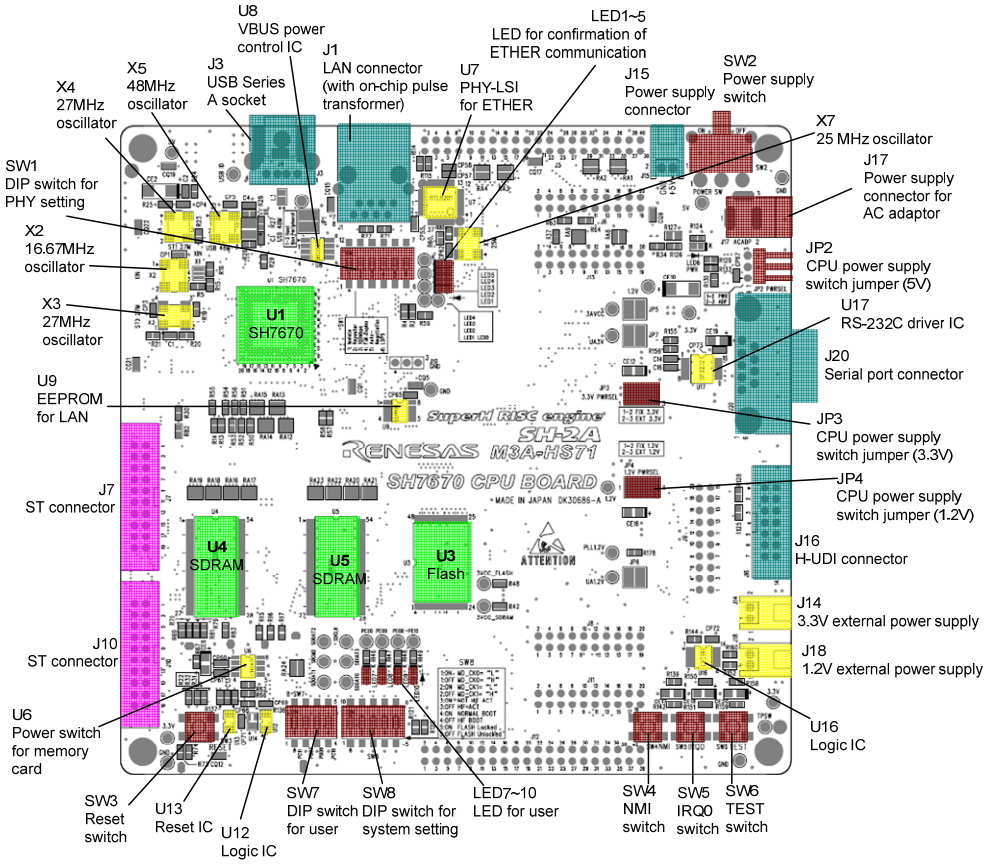


Figure 1.4.1 SH7670 CPU Board System Block Diagram

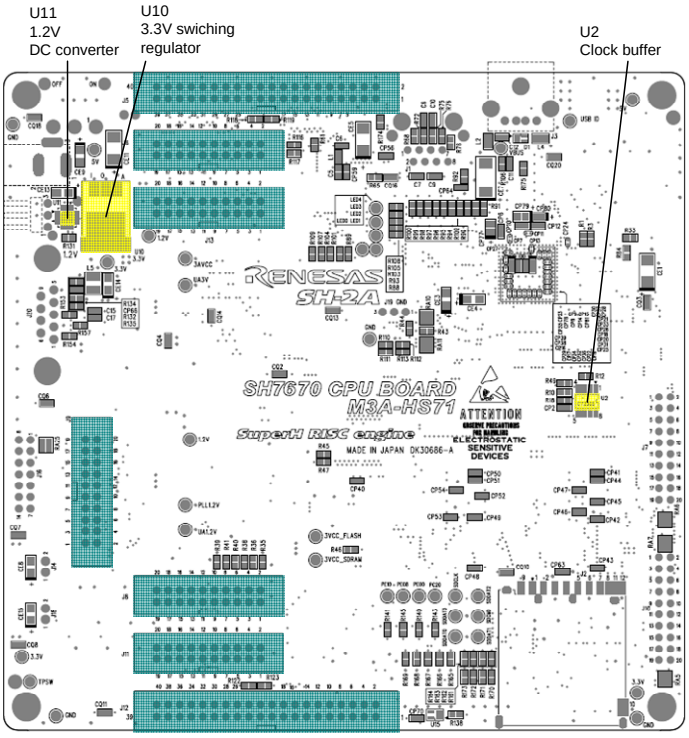
1.5 External View

Figure 1.5.1 shows the SH7670 CPU board overview (the image of component placement).

<Top view of the component side>



<Top view of the solder side>



: SH7670 extension connector (Not mounted)

Figure 1.5.1 SH7670 CPU Board Overview

1.6 SH7670 CPU Board Memory Mapping

Figure 1.6.1 shows the SH7670 memory mapping of the SH7670 CPU board.

Logical Address	SH7670 Logical Space	SH7670 CPU Board Memory Mapping
H'0000 0000 H'007F FFFF	CS0 Space: 64 MB	Flash Memory (8 MB) 16-bit bus
		User Area
H'0400 0000	Reserved Area	Reserved Area (Disabled)
H'0800 0000	Reserved Area	Reserved Area (Disabled)
H'0C00 0000 H'0FFF FFFF	CS3 space: 64 MB	SDRAM (64 MB) 32-bit bus
H'1000 0000	CS4 space: 64 MB	User Area
H'1400 0000	CS5 space: 64 MB	User Area
H'1800 0000	CS6 space: 64 MB	User Area
H'1C00 0000	Reserved Area	Reserved Area (Disabled)
H'2000 0000	CS0~CS6 space (Cache disabled space)	CS0~CS6 space (Cache disabled space)
H'8000 0000	Reserved Area (Disabled)	Reserved Area (Disabled)
H'FFF8 0000	On-chip RAM (32 KB)	On-chip RAM (32 KB)
H'FFF8 8000 H'FFF8 FFFF	On-chip RAM Reserved	On-chip RAM Reserved
H'FFFC 0000 H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module

Figure 1.6.1 SH7670 CPU Board Memory Mapping

1.7 Absolute Maximum Ratings

Table 1.7.1 lists the absolute maximum ratings of the SH7670 CPU board.

Table 1.7.1 Absolute Maximum Ratings of the SH7670 CPU Board

Symbol	Parameter	Rated Value	Remarks
VCC	5V system power supply voltage	-0.3V to 6.0V	Relative to VSS
3VCC	3.3V system power supply voltage	-0.3V to 4.6V	Relative to VSS
1.2VCC	1.2V system power supply voltage	-0.3V to 1.7V	Relative to VSS
Topr	Operating ambient temperature	-10°C to 55°C	No dewdrops allowed. Use in corrosive gas environment prohibited.
Tstr	Storage ambient temperature	-20°C to 60°C	No dewdrops allowed. Use in corrosive gas environment prohibited.

Note: The ambient temperature refers to the air temperature in places closest possible to the board.

1.8 Recommended Operating Conditions

Table 1.8.1 lists the recommended operating conditions of the SH7670 CPU board.

Table 1.8.1 Operating Condition of SH7670 CPU Board

Symbol	Parameter	Rated Value	Remarks
VCC	5V system power supply voltage	4.75V to 5.25V	Relative to VSS
3VCC	3.3V system power supply voltage	3.0V to 3.6V	Relative to VSS
1.2VCC	1.2V system power supply voltage	1.1V to 1.3V	Relative to VSS
-	Maximum current consumption in the board	Within 1.5A	
Topr	Operating ambient temperature	0°C to 40°C	No dewdrops allowed. Use in corrosive gas environment prohibited.

Chapter2
Functional Overview

2.1 Functional Overview

Table 2.1.1 lists the function modules of SH7670 CPU board.

Table 2.1.1 Functional Modules of SH7670 CPU Board

Section	Function	Content
2.2	CPU	SH7670 ● Input(XIN) Clock: 16.67 MHz ● Bus Clock: 66.67 MHz ● CPU Clock: Maximum 200 MHz
2.3	Memory	The following memories are mounted ● SDRAM: Maximum 64 MB • EDS2516APTA-75 x 2: 64 MB • 32-bit bus width ● Flash memory • S29GL064A90TFIR4 x 1: 8 MB • 16-bit data bus width fixed ● EEPROM • HN58X24128FPIE x 1: 16 KB
2.4	USB Interface	Mounts USB connector
2.5	Serial Port Interface	Connects the SH7670 SCIF0 to serial port connector
2.6	ST Interface	Connects the SH7670 ST interface signal to the ST connector(channel 1 and 2)
2.7	LAN Interface	Connects the SH7670 Ethernet controller to PHY LSI
2.8	I/O Port	Connects the SH7670 I/O port
2.9	Power Supply Circuit	Controls the system power control of SH7670 CPU board
2.10	Clock Module	Clock control
2.11	Reset Module	Reset control for device mounted on the SH7670 CPU board
2.12	Interrupt Switch	Connects the NMI pin and IREQ0 pin
2.13	E10A-USB Interface	SH7670 H-UDI interface
-	Operational Specifications	Connector, switch, LED ● SH7670 extension connector ● Switch, LED ● H-UDI connector Details are described in Chapter 3

2.2 CPU

2.2.1 SH7670 Outline

The SH7670 CPU board contains the 32-bit RISC microcomputer SH7670 that operates with a maximum 200MHz of CPU clock frequency.

2.2.2 SH7670 Pin Function Used on SH7670 CPU Board

Table 2.2.1~Table 2.2.8 list the SH7670 pin functions used on the SH7670 CPU board.

Table 2.2.1 SH7670 Pin Selection Used on SH7670 CPU Board (1)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
Clock	EXTAL	I	External clock	Inputs 16.67 MHz from oscillator	Connects to oscillator
	XTAL	O	Crystal		Crystal resonator is connected
	CKIO	O	System clock	Clock output	CKIO is branched to connect the followings • Connects to SDRAM • Connects to an extension connector
Operating Mode	MD_BW	I	Mode setting	The bus width for CS0 space is set to 16-bit. MD_BW="L"	Connects to GND
	MD_CK1 MD_CK0	I	Clock mode setting	Clock mode is switched. Clock mode 0 : MD_CLK0="L",MD_CLK1="L" Clock mode 1 : MD_CLK0="H",MD_CLK1="L" Clock mode 3 : MD_CLK0="H",MD_CLK1="H" Switching between MD_CLK0 and MD_CLK1 is executed with the DIP switch SW.	• Connects to DIP switch for mode setting MD_CK0, MD_CK1
System Control	RES#	I	Power-on reset	When power-on-reset and pressing the reset SW, it becomes a power-on-reset state.	Connects to reset circuit
Bus Control	CS0#	O	Chip select	Chip select signal CS0#	Connects to CE# signal of NOR flash memory (U3-26)
	CS3#	O	Chip select	Chip select signal CS3#	• Connects to the CS# pin of SDRAM (U4-19,U5-19) • Connects to an extension connector (J9-11),
	CS4#	O	Chip select	Chip select signal CS4#(PB06/CS4#)	Connects to an extension connector (J9-5)
	CS5#	O	Chip select	Chip select signal CS5#(PB05/CS5#/CE1A#/IRQ3/TEND1)	Connects to an extension connector (J8-11)
	CS6#	O	Chip select	Chip select signal CS6#(PB03/CS6#/CE1B#/IRQ1/DREQ1)	Connects to an extension connector (J9-7)
	CKE	O	CK enable	CK enable signal CKE	• Connects to the CKE# pin of SDRAM (U4-37,U5-37) • Connects to an extension connector (J9-14)

Table 2.2.2 SH7670 Pin Selection Used on SH7670 CPU Board (2)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
	RAS#	O	RAS	RAS signal RAS#	• Connects to the RAS# pin of SDRAM (U4-18,U5-18) • Connects to an extension connector (J9-12)
	CAS#	O	CAS	CAS signal CAS#	• Connects to the CAS# pin of SDRAM (U4-17,U5-17) • Connects to an extension connector (J9-13)
	RD/WR#	O	Read-write	Read-write signal RD/WR#	• Connects to the WE# pin of SDRAM (U4-16,U5-16) • Connects to an extension connector (J9-15)
	RD#	O	Read	Read signal RD#	• Connects to the OE# signal of NOR flash memory (U3-28) • Connects to an extension connector (J12-5)
	WE0#/DQMLL	O	Least significant byte written/least significant byte selection	D7-D0 is selected WE0#/DQMLL(WE0#/DQMLL)	• Connects to the WE# pin of NOR flash memory (U3-11) • Connects to the DQML pin of SDRAM (U5-15) • Connects to an extension connector (J9-19)
	WE1#/DQMLU	O	Third byte written/third byte selection	D15-D8 is selected DQMLU(WE1#/DQMLU/WE#)	• Connects to the DQMU pin of SDRAM (U5-39) • Connects to an extension connector (J9-18)
	WE2#/DQMUL	O	Second byte written/second byte selection	D23-D16 is selected DQMUL(WE2#/DQMUL/ICIORD#)	• Connects to the DQMU pin of SDRAM (U4-15) • Connects to an extension connector (J9-17)
	WE3#/DQMUU	O	Most significant byte written/most significant byte selection	D31-D24 is selected DQMUU(WE3#/DQMUU/ICIOWR#)	• Connects to the DQML pin of SDRAM (U4-39) • Connects to an extension connector (J9-16)
	WAIT#	I	Wait	WAIT#: PB00/WAIT#/SDA	Connects to an extension connector (J9-10)
Address Bus	A25-A00	O	Address bus	26-bit address bus	• A25-A00 Connects to an extension connector (J12) • A22-A01 Connects to FLASH (U3) • A16-A02 Connects to SDRAM (U4,U5)
Data Bus	D31-D00	O	Data bus	32-bit data bus	• D15-D00 Connects to FLASH (U3) • D31-D00 SDRAM(U4,U5) Connects to an extension connector (J5)

Table 2.2.3 SH7670 Pin Selection Used on SH7670 CPU Board (3)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
INTC	IRQ	I	Interrupt request	Interrupt request pin which can select level and edge input. Each IRQ pin is connected to the followings. • IRQ7#(PD07/IRQ7#/SDCLK) • IRQ6#(PD06/IRQ6#/SDCMD) • IRQ5#(PD05/IRQ5#/SDCD) • IRQ4#(PD04/IRQ4#/SDWP) • IRQ3#(PD03/IRQ3#/SDDATA3) • IRQ2#(PD02/IRQ2#/SDDATA2) • IRQ1#(PD01/IRQ1#/SDDATA1) • IRQ0#(PD00/IRQ0#/SDDATA0) • IRQ3(PB05/CS5#/CE1A#/IRQ3/TEND1) • IRQ2(PB04/CE2A#/IRQ2/DACK1) • IRQ1(PB03/CS6#/CE1B#/IRQ1/DREQ1) • IRQ0(PB02/CE2B#/IRQ0)	• Connects to an extension connector IRQ7#(J8-12) IRQ6#(J8-13) IRQ5#(J8-14) IRQ4#(J8-15) IRQ3#(J8-16) IRQ2#(J8-17) IRQ1#(J8-18) IRQ0#(J8-19) IRQ3(J8-11) IRQ2(J9-6) IRQ1(J9-7) IRQ0(J9-8) • Connects to push switch IRQ0 (SW5) • Connects to VBUS IRQ1(U8-2)
DMAC	DREQ1 DREQ0	I	DMA transfer request	External DMA transfer request input pin DREQ1(PB03/CS6#/CE1B#/IRQ1/DREQ1) DREQ0(PF09/ST0_VLD/DREQ0)	• Connects to an extension connector DREQ1(J9-7) • Connects to ST connector DREQ1(J7-16)
	DACK1 DACK0	O	DMA transfer request is acknowledged	Request acknowledge output pin to external DMA transfer request DACK1(PB04/CE2A#/IRQ2/DACK1) DACK0(PF10/ST0_SYC//DACK0)	• Connects to an extension connector DACK1(J9-6) • Connects to ST connector DACK0(J7-15)
	TEND1 TEND0	O	DMA transfer completion output	DMA transfer completion output signal TEND1(PB05/CS5#/CE1A#/IRQ3/TEND1) TEND0(PF11/ST0_PWM/TEND0)	• Connects to an extension connector TEND1(J8-11) • Connects to ST connector TEND0(J7-17)
Ether	CRS	I	Carrier sense	Carrier sense pin CRS(PC15/CRS)	Connects to PHY-LSI (U7-23)
	COL	I	Collision	Collision detection pin COL(PC14/COL)	Connects to PHY-LSI (U7-1)
	MII_TXD3 MII_TXD2 MII_TXD1 MII_TXD0	O	Sending data	4-bit sending data pin MII_TXD3(PC07/MII_TXD3) MII_TXD2(PC06/MII_TXD2) MII_TXD1(PC05/MII_TXD1) MII_TXD0(PC04/MII_TXD0)	Connects to PHY-LSI MII_TXD3(U7-3) MII_TXD2(U7-4) MII_TXD1(U7-5) MII_TXD0(U7-6)
	TX_EN	O	Sending enable	Indicates that sending data is ready for MII_TXD3-0 TX_EN(PC12/TX_EN)	Connects to PHY-LSI (U7-2)
	TX_CLK	I	Sending clock	Reference timing of TX_EN, TX_ER, and MII_TXD3-0 TX_CLK(PC13/TX_CLK)	Connects to PHY-LSI (U7-7)
	TX_ER	O	Sending error	Pins notifying PHY-LSI of the error in transmitting TX_ER(PC11/TX_ER)	Connects to an extension connector (J11-6)
	MII_RXD3 MII_RXD2 MII_RXD1 MII_RXD0	I	Receive data	4-bit receiving data pin MII_RXD3(PC03/MII_RXD3) MII_RXD2(PC02/MII_RXD2) MII_RXD1(PC01/MII_RXD1) MII_RXD0(PC00/MII_RXD0)	Connects to PHY-LSI MII_RXD3(U7-18) MII_RXD2(U7-19) MII_RXD1(U7-20) MII_RXD0(U7-21)
	RX_DV	I	Receive data valid	Indicates that there is enabled receiving data for MII_RXD3-0 RX_DV(PC08/RX_DV)	Connects to PHY-LSI (U7-22)

Table 2.2.4 SH7670 Pin Selection Used on SH7670 CPU Board (4)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
Ether	RX_CLK	I	Receiving clock	Reference timing of RX_DV, RX_ER, and MII_RXD3-0 RX_CLK(PC10/RX_CLK)	Connects to PHY-LSI (U7-16)
	RX_ER	I	Receive error	Pins recognizing the error state occurred in receiving RX_ER: (PC09/RX_ER)	Connects to PHY-LSI (U7-24)
	MDC	O	Clock for management	Reference timing input of transfer information by MDIO MDC: (PC17/MDC)	Connects to PHY-LSI (U7-25)
	MDIO	I/O	Data I/O for management	Bidirectional pin for exchanging management information MDIO(PC16/MDIO)	Connects to PHY-LSI (U7-26)
	WOL	O	MAGIC packet receive	Pin indicating Magic Packet™ * receive WOL(PC20/WOL)	Connects to an extension connector (J11-3)
	LNKSTA	I	Link status	Link state input pin from PHY-LSI LNKSTA(PC18/LNKSTA)	Connects to an extension connector (J11-4)
	EXOUT	O	General output	External output pin EXOUT(PC19/EXOUT)	Connects to an extension connector (J11-5)
STIF	ST_CLKOUT	O	Clock output	Data clock output ST_CLKOUT	Connects to ST connector (J7-2,J10-2)
	ST1_CLKIN ST0_CLKIN	I	Clock input	Data clock input ST1_CLKIN(ST1_CLKIN/SSISCK1) ST0_CLKIN(ST0_CLKIN/SSISCK0)	Connects to ST connector ST1_CLKIN(J10-1) ST0_CLKIN(J7-1)
	ST1_SYC ST0_SYC	I/O	Synchronous signal	Synchronous signal ST1_SYC(PE10/ST1_SYC/CTS2) ST0_SYC(PF10/ST0_SYC/DACK0)	Connects to ST connector ST1_SYC(J10-15) ST0_SYC(J7-15)
	ST1_REQ ST0_REQ	I/O	Request	Request signal ST1_REQ(PE08/ST1_REQ/TxD2) ST0_REQ(PF08/ST0_REQ)	Connects to ST connector ST1_REQ(J10-18) ST0_REQ(J7-18)
	ST1_VLD ST0_VLD	I/O	Data enable	Data enable ST1_VLD(PE09/ST1_VLD/SCK2) ST0_VLD(PF09/ST0_VLD/DREQ0)	Connects to ST connector ST1_VLD(J10-16) ST0_VLD(J7-16)
	ST1_D7 ST1_D6 ST1_D5 ST1_D4 ST1_D3 ST1_D2 ST1_D1 ST1_D0 ST0_D7 ST0_D6 ST0_D5 ST0_D4 ST0_D3 ST0_D2 ST0_D1 ST0_D0	I/O	Data	Data (0 is used for serial mode) ST1_D7(PE07/ST1_D7/SSIWS1) ST1_D6(PE06/ST1_D6/SSIDATA1) ST1_D5(PE05/ST1_D5/RTS1) ST1_D4(PE04/ST1_D4/CTS1) ST1_D3(PE03/ST1_D3/SCK1) ST1_D2(PE02/ST1_D2/RxD1) ST1_D1(PE01/ST1_D1/TxD1) ST1_D0(PE00/ST1_D0/RxD2) ST0_D7(PF07/ST0_D7/SSIWS0) ST0_D6(PF06/ST0_D6/SSIDATA0) ST0_D5(PF05/ST0_D5/RTS0) ST0_D4(PF04/ST0_D4/CTS0) ST0_D3(PF03/ST0_D3/SCK0) ST0_D2(PF02/ST0_D2/RxD0) ST0_D1(PF01/ST0_D1/TxD0) ST0_D0(PF00/ST0_D0)	Connects to ST connector ST1_D7(J10-11) ST1_D6(J10-6) ST1_D5(J10-12) ST1_D4(J10-5) ST1_D3(J10-13) ST1_D2(J10-4) ST1_D1(J10-14) ST1_D0(J10-3) ST0_D7(J7-11) ST0_D6(J7-6) ST0_D5(J7-12) ST0_D4(J7-5) ST0_D3(J7-13) ST0_D2(J7-4) ST0_D1(J7-14) ST0_D0(J7-3)

Table 2.2.5 SH7670 Pin Selection Used on SH7670 CPU Board (5)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
STIF	ST1_VCO_CLKIN, ST0_VCO_CLKIN	I	VCX0 clock	VCX0 clock ST1_VCO_CLKIN (ST1_VCO_CLKIN/AUDIO_CLK)	Connects to ST connector ST1_VCO_CLKIN (J10-19) ST0_VCO_CLKIN (J7-19)
	ST1_PWM ST0_PWM	O	PWM output	PWM output ST1_PWM(PE11/ST1_PWM/RTS2) ST0_PWM(PF11/ST0_PWM/TEND0)	Connects to ST connector ST1_PWM(J10-17) ST0_PWM(J7-17)
USB	DP	I/O	USB D+ Data	USB bus D+ Data	Connects to USB (J3-3)
	DM	I/O	USB D- Data	USB bus D- data	Connects to USB (J3-2)
	VBUS	I	VBUS input	Connects to Vbus of USB bus	Connects to USB (J3-1)
	REFRIN	I	Reference input	Connects to USBAPVss through 5.6KΩ±1% resistance	Connects to USB
	USB_X1 USB_X2	I/O	Input between crystal resonator for USB and external clock	Crystal resonator for USB is connected. USB_X1 can input an external clock	Connects to crystal resonator (48 MHz) for USB (X5)
	AV33	I	USB analog pin power supply	Transceiver analog pin power supply	Connects to 3.3V
	AG33	I	USB analog pin GND	Transceiver analog pin GND	Connects to GND
	DV33	I	USB digital pin power supply	Transceiver digital pin power supply	Connects to 3.3V
	DG33	I	USB digital pin GND	Transceiver digital pin GND	Connects to GND
	AV12	I	USB analog core power supply	Transceiver analog core power supply	Connects to 1.2V
	AG12	I	USB analog core GND	Transceiver analog core GND	Connects to GND
	DV12	I	USB digital pin power supply	Transceiver digital pin power supply	Connects to 1.2V
	DG12	I	USB digital pin GND	Transceiver digital pin GND	Connects to GND
	UV12	I	USB digital core power supply	Transceiver digital core power supply	Connects to 1.2V
	UG12	I	USB digital core GND	Transceiver digital core GND	Connects to GND

Table 2.2.6 SH7670 Pin Selection Used on SH7670 CPU Board (6)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
HIF	HIFD15-HIFD00	I/O	HIF data bus	Address/data/command I/O for HIF HIFD15(PG15/HIFD15) HIFD14(PG14/HIFD14) HIFD13(PG13/HIFD13) HIFD12(PG12/HIFD12) HIFD11(PG11/HIFD11) HIFD10(PG10/HIFD10) HIFD09(PG09/HIFD09) HIFD08(PG08/HIFD08) HIFD07(PG07/HIFD07) HIFD06(PG06/HIFD06) HIFD05(PG05/HIFD05) HIFD04(PG04/HIFD04) HIFD03(PG03/HIFD03) HIFD02(PG02/HIFD02) HIFD01(PG01/HIFD01) HIFD00(PG00/HIFD00)	Connects to an extension connector HIFD15(J13-4) HIFD14(J13-5) HIFD13(J13-6) HIFD12(J13-7) HIFD11(J13-8) HIFD10(J13-9) HIFD09(J13-10) HIFD08(J13-11) HIFD07(J13-12) HIFD06(J13-13) HIFD05(J13-14) HIFD04(J13-15) HIFD03(J13-16) HIFD02(J13-17) HIFD01(J13-18) HIFD00(J13-19)
	HIFCS#	I	HIF chip select	Chip select input for HIF HIFCS#(PG23/HIFCS#)	Connects to an extension connector (J8-3)
	HIFRS	I	HIF register select	Instruction of switching access type for HIF HIFRS(PG22/HIFRS)	Connects to an extension connector (J8-4)
	HIFWR#	I	HIF write	Write strobe signal HIFWR#(PG21/HIFWR#)	Connects to an extension connector (J8-5)
	HIFRD#	I	HIF read	Read strobe signal HIFRD#(PG20/HIFRD#)	Connects to an extension connector (J13-3)
	HIFINT#	O	HIF interrupt	Interrupt request from HIF to external device HIFIHT#(PG19/HIFINT#)	Connects to an extension connector (J8-6)
	HIFMD	I	HIF mode	HIF boot mode is specified HIFMD only enable for power-on-reset by RES# pin (HIFMD/PA25/A25)	Connects to the DIP switch for mode setting (SW8-7)
	HIFDREQ	O	HIFDMAC transfer request	For external device, DMAC transfer to HIFRAM is requested HIFDREQ(PG18/HIFDREQ)	Connects to an extension connector (J8-7)
	HIFEBL	I	HIF pin enable	By inputting high level, HIF pin except this pin is activated HIFEBL(PG16/HIFEBL)	Connects to an extension connector (J8-9)
	HIFRDY	O	HIF boot ready	Indicates that, in this LSI, reset to HIF module is released to be possible to acknowledge the access to HIF module from external devices. HIFRDY(PG17/HIFRDY)	Connects to an extension connector (J8-8)

Table 2.2.7 SH7670 Pin Selection Used on SH7670 CPU Board (7)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
IIC3	SCL	I/O	Serial clock	Serial clock I/O pin SCL(PB01/IOIS16#/SCL)	• Connects to EEPROM (U9-6) • Connects to an extension connector (J9-9)
	SDA	I/O	Serial data	Serial data I/O pin SDA(PB00/WAIT#/SDA)	• Connects to EEPROM (U9-5) • Connects to an extension connector (J9-10)
SCIF	TXD2 TXD1 TXD0	O	Sending data	Pins for sending data TXD2(PE08/ST1_REQ/TxD2) TXD1(PE01/ST1_D1/TxD1) TXD0(PF01/ST0_D1/TxD0)	• Connects to ST connector TXD2(J10-18) TXD1(J10-14) TXD0(J7-14) • TxD0 is also connected to serial connector
	RXD2 RXD1 RXD0	I	Receiving data	Pins for receiving data RXD2(PE00/ST1_D0/RxD2) RXD1(PE02/ST1_D2/RxD1) RXD0(PF02/ST0_D2/RxD0)	• Connects to ST connector RXD2(J10-3) RXD1(J10-4) RXD0(J7-4) • RxD0 is also connected to serial connector
	SCK2 SCK1 SCK0	I/O	Serial clock	Clock input pin SCK2(PE09/ST1_VLD/SCK2) SCK1(PE03/ST1_D3/SCK1) SCK0(PF03/ST0_D3/SCK0)	Connects to ST connector SCK2(J10-16) SCK1(J10-13) SCK0(J7-13)
	RTS2# RTS1# RTS0#	O	Send request	Modem control pin RTS2#(PE11/ST1_PWM/RTS2#) RTS1#(PE05/ST1_D5/RTS1#) RTS0#(PF05/ST0_D5/RTS0#)	Connects to ST connector RTS2#(J10-17) RTS1#(J10-12) RTS0#(J7-12)
	CTS2# CTS1# CTS0#	I	Send possible	Modem control pin CTS2#(PE10/ST1_SYC/CTS2#) CTS1#(PE04/ST1_D4/CTS1#) CTS0#(PF04/ST0_D4/CTS0#)	Connects to ST connector CTS2#(J10-15) CTS1#(J10-5) CTS0#(J7-5)
SSI	SSIDATA1 SSIDATA0	I/O	SSI data I/O	Serial data I/O pin SSIDATA1(PE06/ST1_D6/SSIDATA1) SSIDATA0(PF06/ST0_D6/SSIDATA0)	Connects to an extension connector SSIDATA1(J11-18) SSIDATA0(J11-19)
	SSISCK1 SSISCK0	I/O	SSI clock I/O	Serial clock I/O pin SSISCK1(ST1_CLKIN/SSISCK1) SSISCK0(ST0_CLKIN/SSISCK0)	Connects to an extension connector SSISCK1(J11-14) SSISCK0(J11-15)
	SSIWS1 SSIWS0	I/O	SSI clock LR I/O	Word selection I/O pin SSIWS1(PE07/ST1_D7/SSIWS1) SSIWS0(PF07/ST0_D7/SSIWS0)	Connects to an extension connector SSIWS1(J11-16) SSIWS0(J11-17)
	AUDIO_ CLK	I	External clock for SSI audio	External clock for audio is input AUDIO_CLK (ST1_VCO_CLKIN/AUDIO_CLK)	Connects to an extension connector (J11-13)

Table 2.2.8 SH7670 Pin Selection Used on SH7670 CPU Board (8)

Type	Pin	I/O	Name	Function of SH7670 CPU Board	Destination to Connect
IO port	PB06, PB07, PC11, PC19	I	Input port for DIP switch	Assigned in DIP switch for user	Connects to DIP switch for user (SW7)
	PB04	O	Enable (VBUS)	Connects to the VBUS power control IC	Connects to the VBUS power control IC (U8-1)
	PB05	O	Enable (LTC1470)	Connects to the memory card power control IC LTC1470	Connects to the memory card power control IC LTC1470 (U6-4)

Note *: Magic Packet is a trademark of Advanced Micro Devices, Inc.

2.2.3 SH7670 Multiplex Pin Used on the SH7670 CPU Board

Table 2.2.9 to Table 2.2.15 list the function selections of SH7670 multiplex pin used on the SH7670 CPU board.

These pins are set to the port input pin as initial values. Thus, the MD bit of port control register should be set to use the peripheral functions (except I/O port).

Table 2.2.9 Function Selection of SH7670 Multiplex Pin (BSC)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
BSC	A25	PACRH2	PA25MD0 = B'1	PA25/A25
	A24	PACRH2	PA24MD0 = B'1	PA24/A24
	A23	PACRH1	PA23MD0 = B'1	PA23/A23
	A22	PACRH1	PA22MD0 = B'1	PA22/A22
	A21	PACRH1	PA21MD0 = B'1	PA21/A21
	A20	PACRH1	PA20MD0 = B'1	PA20/A20
	A19	PACRH1	PA19MD0 = B'1	PA19/A19
	A18	PACRH1	PA18MD0 = B'1	PA18/A18
	A17	PACRH1	PA17MD0 = B'1	PA17/A17

Table 2.2.10 Function Selection of SH7670 Multiplex Pin (SCIF)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
SCIF	RxD0	PFCRL1	PF2MD[1:0] = B'10	PF02/ST0_D2/RxD0
	TxD0	PFCRL1	PF1MD[1:0] = B'10	PF01/ST0_D1/TxD0

Table 2.2.11 Function Selection of SH7670 Multiplex Pin (Ether)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
Ether	MDC	PCCRH1	PC17MD0 = B'1	PC17/MDC
	MDIO	PCCRH1	PC16MD0 = B'1	PC16/MDIO
	CRS	PCCRL2	PC15MD0 = B'1	PC15/CRS
	COL	PCCRL2	PC14MD0 = B'1	PC14/COL
	TX_EN	PCCRL2	PC12MD0 = B'1	PC12/TX_EN
	TX_CLK	PCCRL2	PC13MD0 = B'1	PC13/TX_CLK
	TX_ER	PCCRL2	PC11MD0 = B'1	PC11/TX_ER
	RX_DV	PCCRL2	PC8MD0 = B'1	PC08/RX_DV
	RX_CLK	PCCRL2	PC10MD0 = B'1	PC10/RX_CLK
	RX_ER	PCCRL2	PC9MD0 = B'1	PC09/RX_ER
	MII_TXD0	PCCRL1	PC4MD0 = B'1	PC04/MII_TXD0
	MII_TXD1	PCCRL1	PC5MD0 = B'1	PC05/MII_TXD1
	MII_TXD2	PCCRL1	PC6MD0 = B'1	PC06/MII_TXD2
	MII_TXD3	PCCRL1	PC7MD0 = B'1	PC07/MII_TXD3
	MII_RXD0	PCCRL1	PC0MD0 = B'1	PC00/MII_RXD0
	MII_RXD1	PCCRL1	PC1MD0 = B'1	PC01/MII_RXD1
	MII_RXD2	PCCRL1	PC2MD0 = B'1	PC02/MII_RXD2
	MII_RXD3	PCCRL1	PC3MD0 = B'1	PC03/MII_RXD3

Table 2.2.12 Function Selection of SH7670 Multiplex Pin (STIF)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
STIF	ST0_D7	PFCRL1	PF7MD[1:0] = B'01	PF07/ST0_D7/SSIWS0
	ST0_D6	PFCRL1	PF6MD[1:0] = B'01	PF06/ST0_D6/SSIDATA0
	ST0_D5	PFCRL1	PF5MD[1:0] = B'01	PF05/ST0_D5/RTS0#
	ST0_D4	PFCRL1	PF4MD[1:0] = B'01	PF04/ST0_D4/CTS0#
	ST0_D3	PFCRL1	PF3MD[1:0] = B'01	PF03/ST0_D3/SCK0
	ST0_D2	PFCRL1	PF2MD[1:0] = B'01	PF02/ST0_D2/RxD0
	ST0_D1	PFCRL1	PF1MD[1:0] = B'01	PF01/ST0_D1/TxD0
	ST0_D0	PFCRL1	PF0MD0 = B'1	PF00/ST0_D0
	ST0_SYC	PFCRL2	PF10MD[1:0] = B'01	PF10/ST0_SYC/DACK0
	ST0_VLD	PFCRL2	PF9MD[1:0] = B'01	PF09/ST0_VLD/DREQ0
	ST0_PWM	PFCRL2	PF11MD[1:0] = B'01	PF11/ST0_PWM/TEND0
	ST0_REQ	PFCRL2	PF8MD0 = B'1	PF08/ST0_REQ
	ST0_CLKIN	PFCRL2	PF13MD[1:0] = B'01	ST0_CLKIN/SSISCK0
	ST1_D7	PECRL1	PE7MD[1:0] = B'01	PE07/ST1_D7/SSIWS1
	ST1_D6	PECRL1	PE6MD[1:0] = B'01	PE06/ST1_D6/SSIDATA1
	ST1_D5	PECRL1	PE5MD[1:0] = B'01	PE05/ST1_D5/RTS1#
	ST1_D4	PECRL1	PE4MD[1:0] = B'01	PE04/ST1_D4/CTS1#
	ST1_D3	PECRL1	PE3MD[1:0] = B'01	PE03/ST1_D3/SCK1
	ST1_D2	PECRL1	PE2MD[1:0] = B'01	PE02/ST1_D2/RxD1
	ST1_D1	PECRL1	PE1MD[1:0] = B'01	PE01/ST1_D1/TxD1
	ST1_D0	PECRL1	PE0MD[1:0] = B'01	PE00/ST1_D0/RxD2
	ST1_SYC	PECRL2	PE10MD[1:0] = B'01	PE10/ST1_SYC/CTS2#
	ST1_VLD	PECRL2	PE9MD[1:0] = B'01	PE09/ST1_VLD/SCK2
	ST1_PWM	PECRL2	PE11MD[1:0] = B'01	PE11/ST1_PWM/RTS2#
	ST1_REQ	PECRL2	PE8MD[1:0] = B'01	PE08/ST1_REQ/TxD2
	ST1_CLKIN	PECRL2	PE13MD[1:0] = B'01	ST1_CLKIN/SSISCK1
	ST1_VCO_CLKIN	PECRL2	PE12MD[1:0] = B'01	ST1_VCO_CLKIN/AUDIO_CLK

Table 2.2.13 Function Selection of SH7670 Multiplex Pin (HIF)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
HIF	HIFD15	PGCRL2	PG15MD0 = B'1	PG15/HIFD15
	HIFD14	PGCRL2	PG14MD0 = B'1	PG14/HIFD14
	HIFD13	PGCRL2	PG13MD0 = B'1	PG13/HIFD13
	HIFD12	PGCRL2	PG12MD0 = B'1	PG12/HIFD12
	HIFD11	PGCRL2	PG11MD0 = B'1	PG11/HIFD11
	HIFD10	PGCRL2	PG10MD0 = B'1	PG10/HIFD10
	HIFD09	PGCRL2	PG09MD0 = B'1	PG09/HIFD09
	HIFD08	PGCRL2	PG08MD0 = B'1	PG08/HIFD08
	HIFD07	PGCRL1	PG07MD0 = B'1	PG07/HIFD07
	HIFD06	PGCRL1	PG06MD0 = B'1	PG06/HIFD06
	HIFD05	PGCRL1	PG05MD0 = B'1	PG05/HIFD05
	HIFD04	PGCRL1	PG04MD0 = B'1	PG04/HIFD04
	HIFD03	PGCRL1	PG03MD0 = B'1	PG03/HIFD03
	HIFD02	PGCRL1	PG02MD0 = B'1	PG02/HIFD02
	HIFD01	PGCRL1	PG01MD0 = B'1	PG01/HIFD01
	HIFD00	PGCRL1	PG00MD0 = B'1	PG00/HIFD00
	HIFCS#	PGCRH2	PG23MD0 = B'1	PG23/HIFCS#
	HIFRS	PGCRH2	PG22MD0 = B'1	PG22/HIFRS
	HIFWR#	PGCRH2	PG21MD0 = B'1	PG21/HIFWR#
	HIFRD#	PGCRH2	PG20MD0 = B'1	PG20/HIFRD#
	HIFINT#	PGCRH2	PG19MD0 = B'1	PG19/HIFINT#
	HIFDREQ	PGCRH2	PG18MD0 = B'1	PG18/HIFDREQ
	HIFRDY	PGCRH2	PG17MD0 = B'1	PG17/HIFRDY
	HIFEBL	PGCRH2	PG16MD0 = B'1	PG16/HIFEBL

Table 2.2.14 Function Selection of SH7670 Multiplex Pin (IIC3)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
IIC3	SCL	PBCRL1	PB1MD[1:0] = B'10	PB01/IOIS16#/SCL
	SDA	PBCRL1	PB0MD[1:0] = B'10	PB00/WAIT#/SDA

Table 2.2.15 Function Selection of SH7670 Multiplex Pin (Example for reference)

Peripheral Function	Pin	SH7670 Port Control Register		SH7670 Multiplex Pin
		Register	MD Bit Setting Value	
BSC	BS#	PBCRL1	PB7MD0 = B'1	PB07/BS#
	CS4#	PBCRL1	PB6MD0 = B'1	PB06/CS4#
	CS5B#/CE1A#	PBCRL1	PB5MD[1:0] = B'01	PB05/CS5#/CE1A#/IRQ3/TEND1
	CE2A#	PBCRL1	PB4MD[1:0] = B'01	PB04/CE2A#/IRQ2/DACK1
	CS6#/CE1B#	PBCRL1	PB3MD[1:0] = B'01	PB03/CS6#/CE1B#IRQ1/DREQ1
	CE2B#	PBCRL1	PB2MD[1:0] = B'01	PB02/CE2B#/IRQ0
	IOIS16#	PBCRL1	PB1MD[1:0] = B'01	PB01/IOIS16#/SCL
	WAIT#	PBCRL1	PB0MD[1:0] = B'01	PB00/WAIT#/SDA
SCIF	RTS2#	PECRL2	PE11MD[1:0] = B'10	PE11/ST1_PWM/RTS2#
	CTS2#	PECRL2	PE10MD[1:0] = B'10	PE10/ST1_SYC/CTS2#
	SCK2	PECRL2	PE9MD[1:0] = B'10	PE09/ST1_VLD/SCK2
	TxD2	PECRL2	PE8MD[1:0] = B'10	PE08/ST1_REQ/TxD2
	RTS1#	PECRL1	PE5MD[1:0] = B'10	PE05/ST1_D5/RTS1#
	CTS1#	PECRL1	PE4MD[1:0] = B'10	PE04/ST1_D4/CTS1#
	SCK1	PECRL1	PE3MD[1:0] = B'10	PE03/ST1_D3/SCK1
	RxD1	PECRL1	PE2MD[1:0] = B'10	PE02/ST1_D2/RxD1
	TxD1	PECRL1	PE1MD[1:0] = B'10	PE01/ST1_D1/TxD1
	RxD2	PECRL1	PE0MD[1:0] = B'10	PE00/ST1_D0/RxD2
	RTS0#	PFCRL1	PF5MD[1:0] = B'10	PF05/ST0_D5/RTS0 #
	CTS0#	PFCRL1	PF4MD[1:0] = B'10	PF04/ST0_D4/CTS0#
	SCK0	PFCRL1	PF3MD[1:0] = B'10	PF03/ST0_D3/SCK0
DMAC	TEND0	PFCRL2	PF11MD[1:0] = B'10	PF11/ST0_PWM/TEND0
	DACK0	PFCRL2	PF10MD[1:0] = B'10	PF10/ST0_SYC/DACK0
	DREQ0	PFCRL2	PF9MD[1:0] = B'10	PF09/ST0_VLD/DREQ0
	TEND1	PBCRL1	PB5MD[1:0] = B'11	PB05/CS5#/CE1A#/IRQ3/TEND1
	DACK1	PBCRL1	PB4MD[1:0] = B'11	PB04/CE2A#/IRQ2/DACK1
	DREQ1	PBCRL1	PB3MD[1:0] = B'11	PB03/CS6#/CE1B#/IRQ1/DREQ1
SSI	SSIWS1	PECRL1	PE7MD[1:0] = B'10	PE07/ST1_D7/SSIWS1
	SSIDATA1	PECRL1	PE6MD[1:0] = B'10	PE06/ST1_D6/SSIDATA1
	SSISCK1	PECRL2	PE13MD[1:0] = B'10	ST1_CLKIN/SSISCK1
	SSIWS0	PFCRL1	PF7MD[1:0] = B'10	PF07/ST0_D7/SSIWS0
	SSIDATA0	PFCRL1	PF6MD[1:0] = B'10	PF06/ST0_D6/SSIDATA0
	SSISCK0	PFCRL2	PF13MD[1:0] = B'10	ST0_CLKIN/SSISCK0
	AUDIO_CLK	PECRL2	PE12MD[1:0] = B'10	ST1_VCO_CLKIN/AUDIO_CLK
INTC	IRQ7#	PDCRL1	PD7MD[1:0] = B'01	PD07/IRQ7#/SDCLK
	IRQ6#	PDCRL1	PD6MD[1:0] = B'01	PD06/IRQ6#/SDCMD
	IRQ5#	PDCRL1	PD5MD[1:0] = B'01	PD05/IRQ5#/SDCD
	IRQ4#	PDCRL1	PD4MD[1:0] = B'01	PD04/IRQ4#SDWP
	IRQ3#	PDCRL1	PD3MD[1:0] = B'01	PD03/IRQ3#/SDDAT3
	IRQ2#	PDCRL1	PD2MD[1:0] = B'01	PD02/IRQ2#/SDDAT2
	IRQ1#	PDCRL1	PD1MD[1:0] = B'01	PD01/IRQ1#/SDDAT1
	IRQ0#	PDCRL1	PD0MD[1:0] = B'01	PD00/IRQ0#/SDDAT0
	IRQ3	PBCRL1	PB5MD[1:0] = B'10	PB05/CS5#/CE1A#/IRQ3/TEND1
	IRQ2	PBCRL1	PB4MD[1:0] = B'10	PB04/CE2A#/IRQ2/DACK1
	IRQ1	PBCRL1	PB3MD[1:0] = B'10	PB03/CS6#/CE1B#/IRQ1/DREQ1
	IRQ0	PBCRL1	PB2MD[1:0] = B'10	PB02/CE2B#/IRQ0

2.3 Memory

The SH7670 CPU board includes the RAM (32 KB) built in SH7670, external flash memory, external SDRAM, and external EEPROM.

The details are described as follows.

2.3.1 RAM built in SH7670

32 KB RAM, 8 KB instruction cache, and 8 KB operand cache are built in the SH7670.

2.3.2 Flash Memory Interface

The SH7670 CPU board standard mounts the flash memory shown in Table 2.3.1 for storing the user program.

The flash memory to boot operates with the external bus 16-bit mode fixed and the power supply voltage operates with single 3.3V. Also, the flash memory write protect can be controlled enable or disable by the DIP switch.

Figure 2.3.1 shows the flash memory interface block diagram and Table 2.3.2 lists the bus state controller setting (write/read) at 66.67 MHz operation for the SH7670 bus clock.

Table 2.3.1 Flash Memory Outline

Part Number	Bus Size	Capacity	Access Time
S29GL064A90TFIR4	16-bit mode	8 MB (16-bit x 4M word x 1pc.)	90 ns

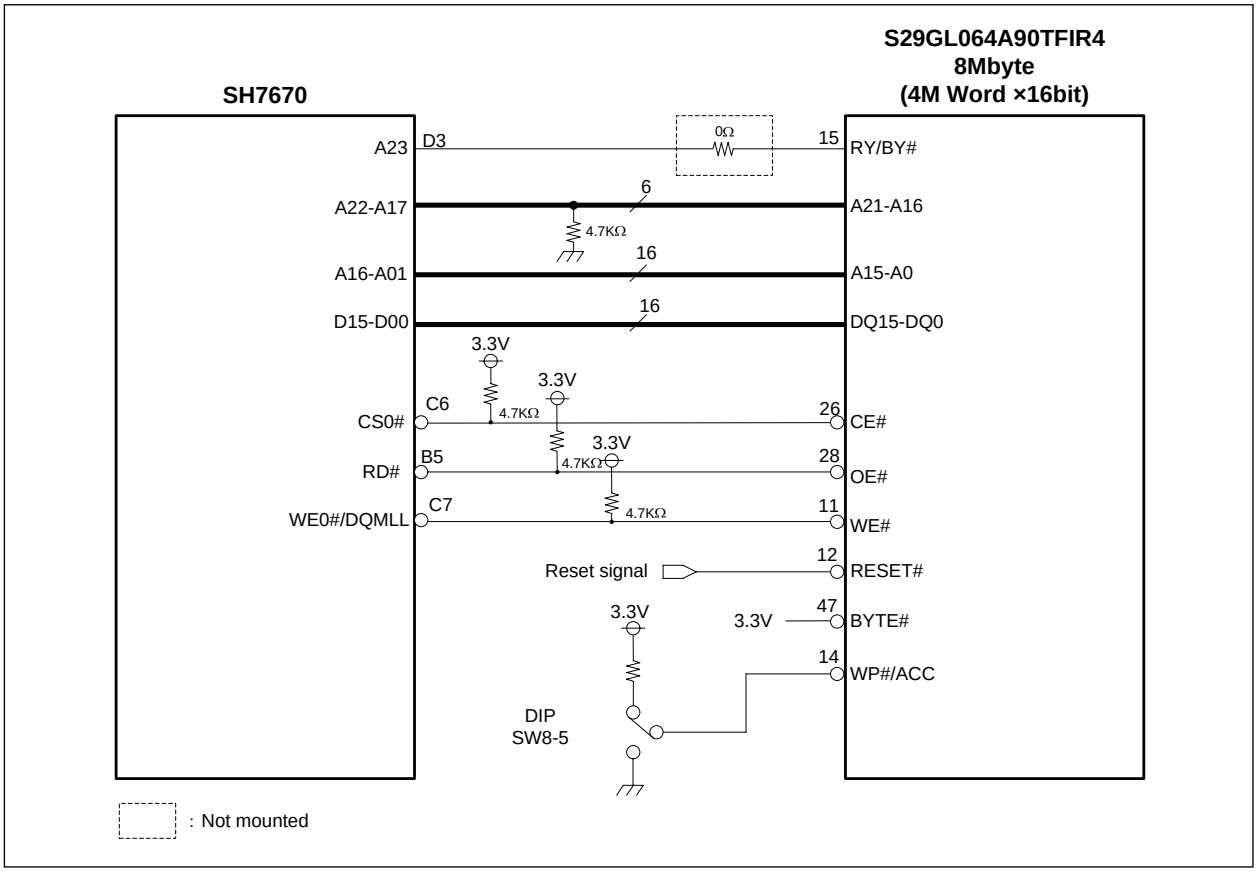


Figure 2.3.1 Flash Memory Interface Block Diagram

Table 2.3.2 Bus State Controller Setting (Flash Memory Write/Read)

User Area	Target Device	Bus State Controller Setting
CS0	S29GL064A90TFIR4	CS0 space bus control register :CS0BCR Initial value: H'36DB 0600 (at MD_BW ="L") Recommended setting value : H'1000 0400 • Idle cycles between write-read cycles and write-write cycles IWW[2:0] = B'001; 1 idle cycle inserted • Data bus specification BSZ[1:0] = B'10 ; 16-bit bus width CS0 space wait control register: CS0WCR Initial value: H'0000 0500 Recommended setting value : H'0000 0AC1 • Assert delay cycle from RD# and WEn# to address and CS0# assert SW[1:0] = B'01; 1.5 cycles • Number of access wait cycle WR[3:0] = B'0110; 5 cycles • CS0# negate delay cycle from RD# and WEn# negate to address HW[1:0] = B'01; 1.5 cycles

<Write/Read Timing>

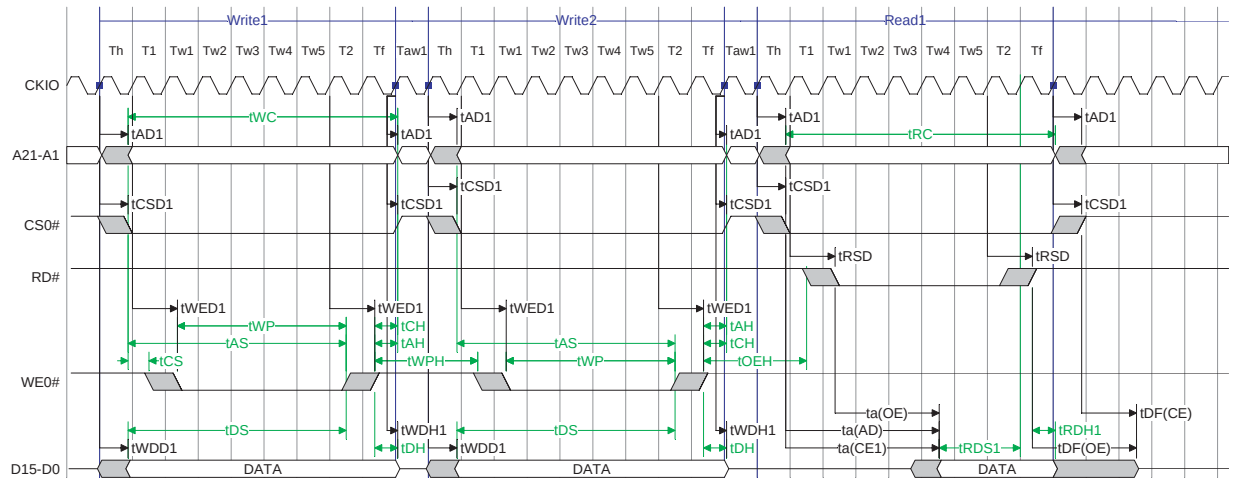


Figure 2.3.2 Example of Flash Memory Read/Write Access Timing

2.3.3 External SDRAM Interface

The SH7670 CPU board standard mounts two 32-Mbyte SDRAMs as external SDRAM. It uses the bus state controller with on-chip SH7670 to control the SDRAM.

Accessing to SDRAM is 32-bit bus access.

Table 2.3.3 lists the SDRAM specification used on the SH7670 CPU board, and Figure 2.3.3 shows the SDRAM interface block diagram.

Table 2.3.3 SDRAM Specification

Specification	Content
Part Number	EDS2516APTA-75
Configuration	32 Mbytes (16-bit bus width) × 2 pcs.
Capacity	64 Mbytes
Access Time	5.4ns
CAS Latency	2 (at bus clock 66.67 MHz)
Refresh Interval	8192 refresh cycles every 64 ms
Low Address	A11- A0
Column Address	A8 - A0
Number of Banks	4 bank operations controlled by BA0, BA1

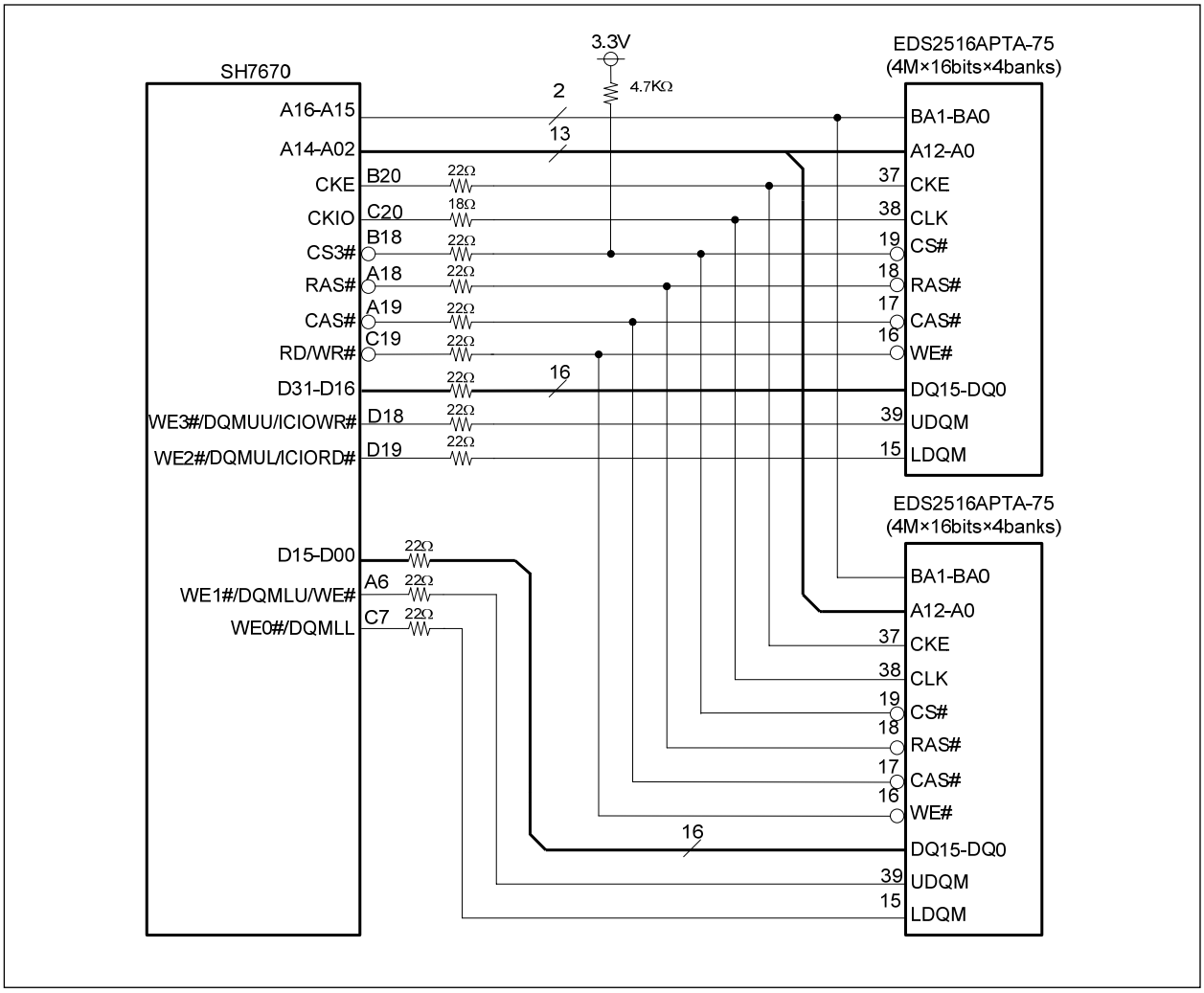


Figure 2.3.3 External SDRAM Interface Block Diagram

Table 2.3.4 lists the example for bus state controller setting at 66.67 MHz operation for the SH7670 bus clock.

Table 2.3.4 Bus State Controller Setting (SDRAM Read/Write)

User Area	Target Device	Bus State Controller Setting
CS3	EDS2516APTA-75	CS3 space bus control register : CS3BCR Initial value: H'36DB 0600 Recommended setting value : H'0000 4600 (at 32 bus width) • Memory specification TYPE[2:0] = B'100; SDRAM • Data bus specification BSZ[1:0] = B'11; 32 bit bus width CS3 space wait control register: CS3WCR Initial value: H'0000 0500, Recommended setting value: H'0000 2892 • Wait precharge completion cycle count WTRP[1:0] = B'01; 1 cycle • Number of wait cycles from ACTV to READ (A) /WRITE (A) command WTRCD[1:0] = B'10; 2 cycles • Area 3CAS latency A3CL[1:0] = B'01; 2 cycles • Wait precharge start cycle count TRWL[1:0] = B'10; 2 cycles • Idle cycles between REF command/self refresh release and ACTV/REF/MRS command WTRC[1:0] = B'10; 5 cycles SDRAM control register: SDCR Initial value: H'0000 0000, Recommended setting value: H'0000 0811 • Refresh control RFSH = B'1; Refresh is performed • Refresh control RMODE = B'0 ; Auto-refreshing • Bank Active mode BACTV = B'0; Auto-precharge mode • Number of bits of row address for area 3 A3ROW[1:0] = B'01; 13 bits • Number of bits of column address for area3 A3COL[1:0] = B'01; 9 bits Refresh timer control/Status register: RTCSR Initial value : H'0000 0000, Recommended setting value:H'A55A 0010 • Clock select CKS[2:0] = B'010; Bϕ/16 • Refresh count RRC[2:0] = B'000; Once Refresh Time Constant Register: RTCOR Initial value: H'0000 0000, Recommended setting value: H'A55A 0020 *The refresh request interval when clock select is set to Bϕ/16 is as follows. 1 cycle: 240 nsec (66.67 MHz/16=4.17 MHz) Refresh request intervals in the SDRAM: 7.8μsec/time 7.8usec /240nsec = 32(0x20) cycle/ refresh counts

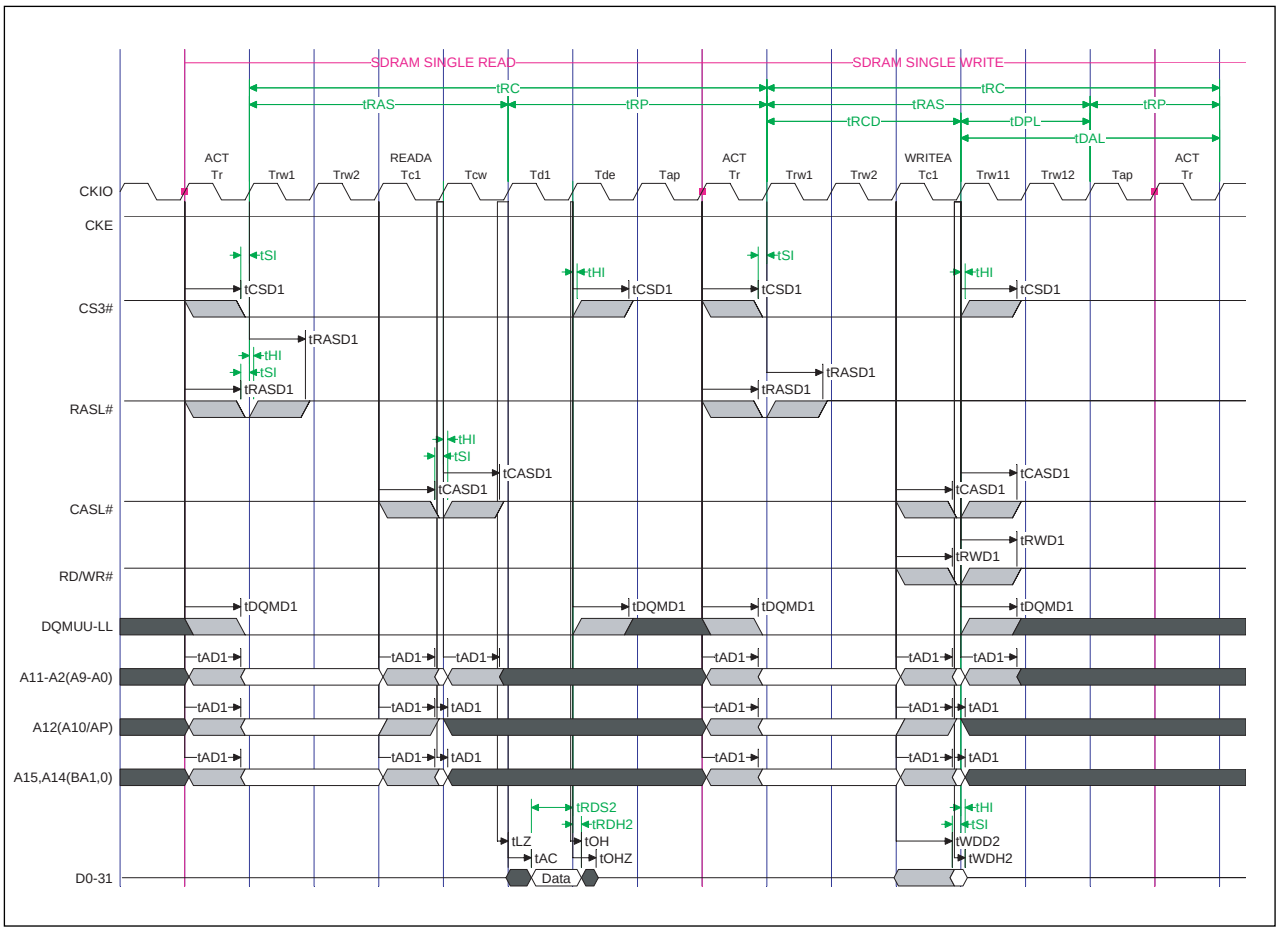


Figure 2.3.4 SDRAM Single Read/Write Timing Example

2.3.4 External EEPROM Interface

The SH7670 CPU board standard mounts 128k-bit EEPROM. It uses the I²C bus interface built in SH7670 to control the EEPROM.

Table 2.3.5 lists the EEPROM specification outline, and Figure 2.3.5 shows the EEPROM interface block diagram.

Table 2.3.5 EEPROM Specification Outline

Part Number	Interface	Capacity	Package
HN58X24128FPIE	Double-wire serial (I²C)	128k-bit(16k-word × 8-bit)	8-pin SOP

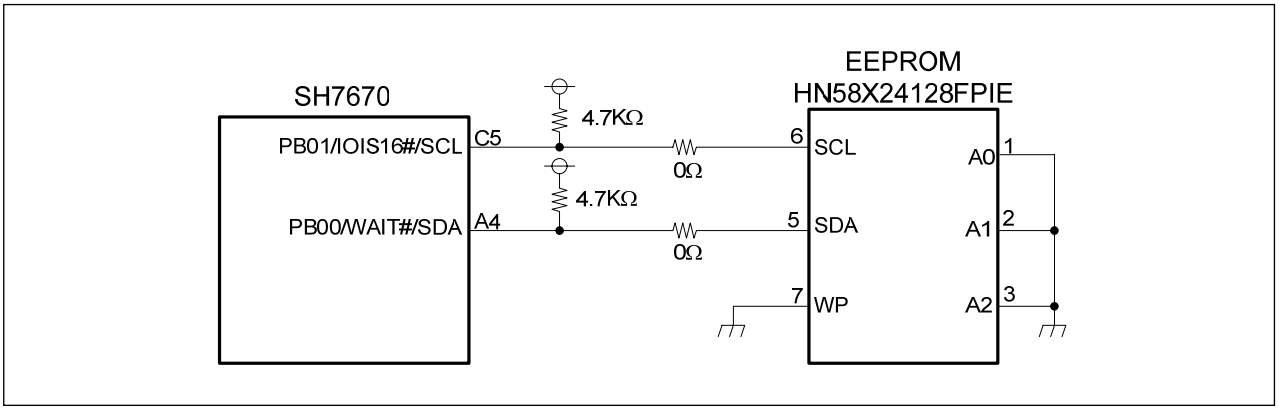


Figure 2.3.5 EEPROM Interface Block Diagram

2.4 USB Interface

The SH7670 mounted on the SH7670 CPU board contains the USB controller preparing for function control function and host control function for the USB standard 2.0.

In addition, the USB series A receptacle is standard mounted as a connector. The board is configured to be able to mount a Mini-B receptacle. When a Mini-AB receptacle or Mini-B receptacle is mounted, the USB series A receptacle should be removed.

Figure 2.4.1 shows USB interface block diagram.

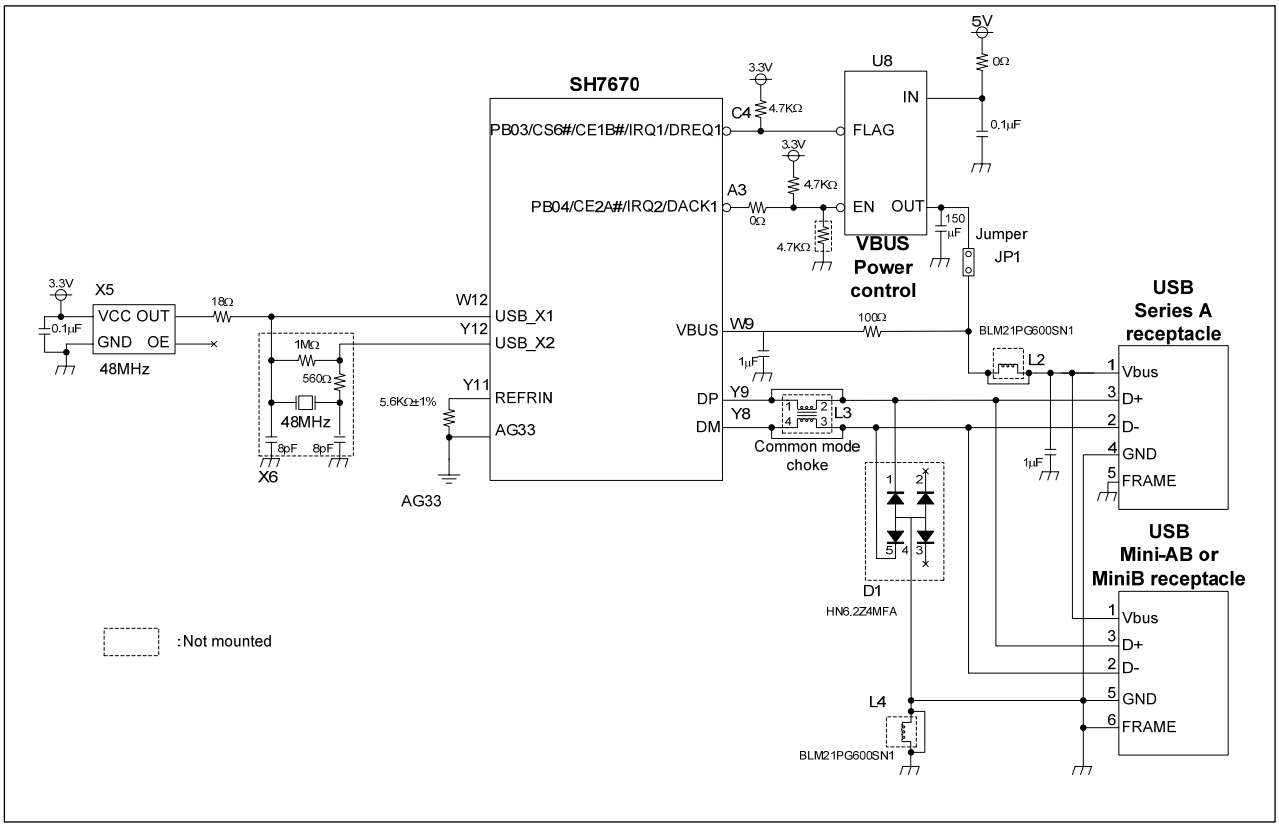


Figure 2.4.1 USB Interface Block Diagram

[VBUS Power Supply/Over Current Detection Control]

In the VBUS power supply control, the VBUS power is supplied by setting the port PB04 to "L" level output, and the VBUS power supply can be cut by setting the port PB04 to "H" level output. When the over current is flowed to the VBUS, the over current detection can be checked by the interrupt or input port with the PB03/IRQ1 pins connected to the pin FLAG of U8 to output "L" level from the pin FLAG of U8.

2.5Serial Port Interface

The SH7670 mounted on the SH7670 CPU board includes a UART module. On the SH7670 CPU board, the SCIF channel 0 is connected to the serial port connector. When the serial port interface is used, ST ch.0 cannot be used. Figure 2.5.1 shows the serial port interface block diagram on the SH7670 CPU board.

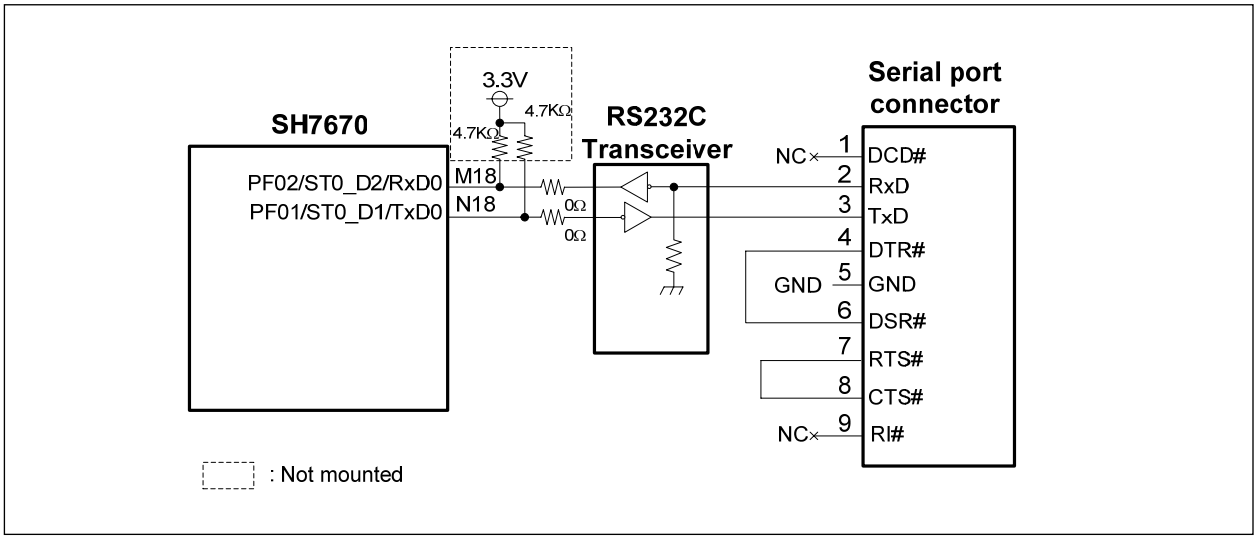


Figure 2.5.1 Serial Port Interface Block Diagram

2.6 ST Interface

The SH7670 CPU board includes the ST connector. When the ST interface is used, the serial port interface cannot be used.

Figure 2.6.1 shows the ST interface block diagram.

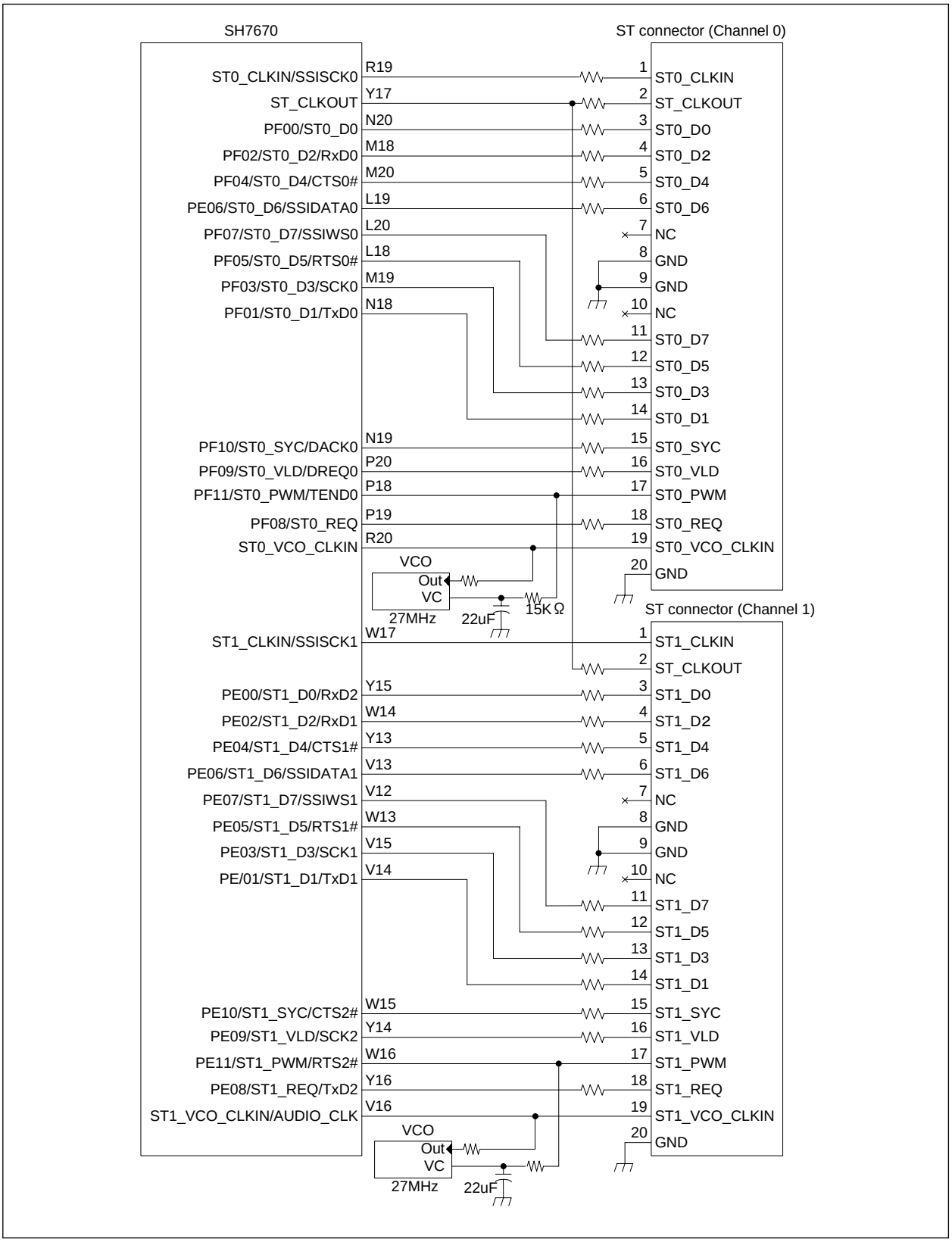


Figure 2.6.1 ST Interface Block Diagram

2.7 LAN Interface

The SH7670 mounted on the SH7670 CPU board includes the Ethernet controller in compliance with MAC layer standard of IEEE802.3. The PHY address is fixed to H'01 by the pin processing in the external circuit of PHYA00-PHYA04 pin.

Figure 2.7.1 shows the LAN interface block diagram on the SH7670 CPU board.

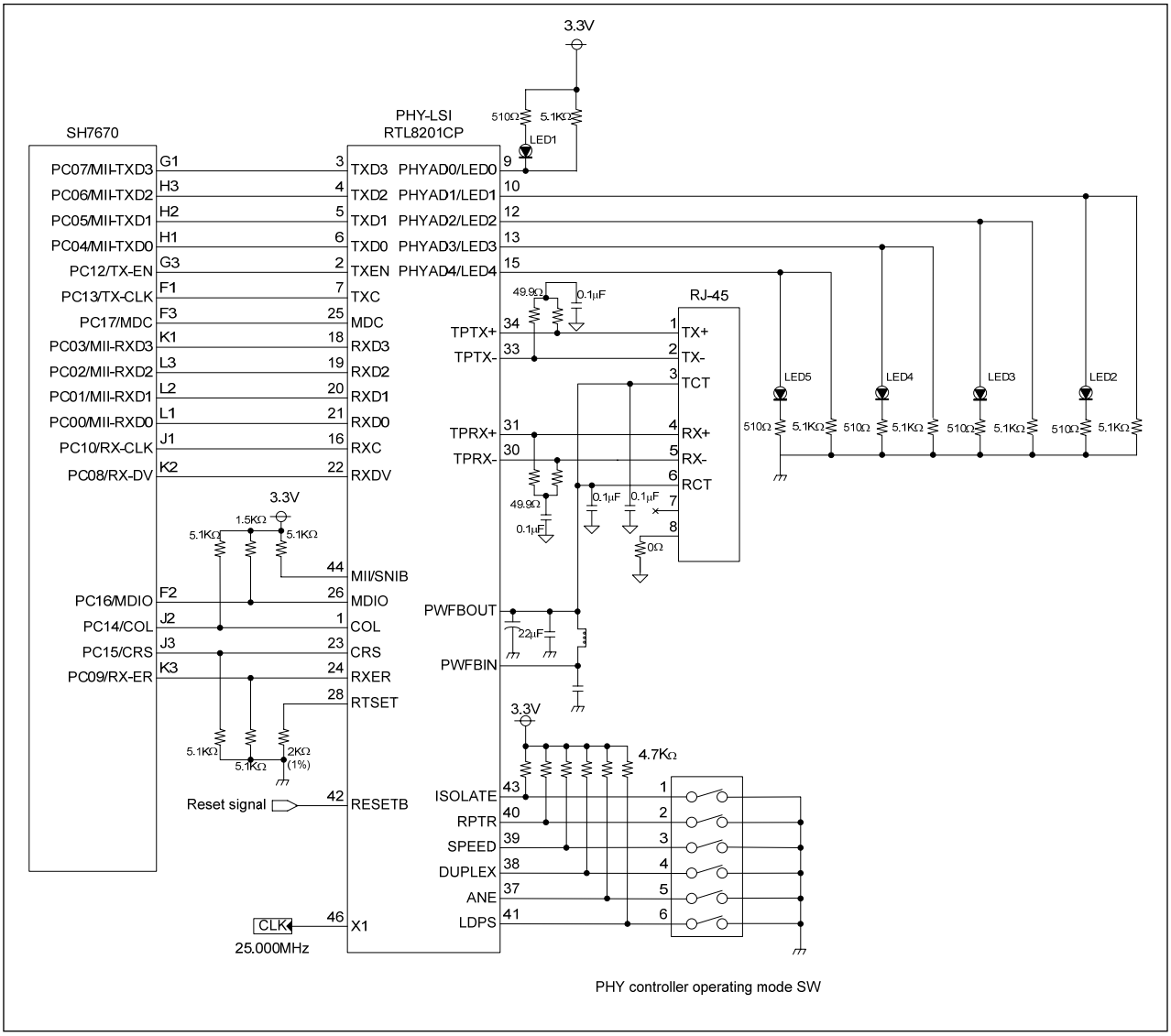


Figure 2.7.1 LAN Interface Block Diagram

The PHY controller operation mode SW (SW1) mounted on the SH7670 CPU board is the switch that determines the operation mode of Ethernet PHY controller mounted on the SH7670 CPU board. This switch is set to Low (0V) in ON, and High (3.3V) in OFF.

Table 2.7.1 lists the description for PHY controller operating mode SW function.

Table 2.7.1 PHY Controller Operating Mode SW Function

Number	Setting		Function	Initial Value
SW1-1	ON	ISOLATE = “L”	Isolate Disable	Initial value
ISOLATE	OFF	ISOLATE = “H”	Isolate Enable	
SW1-2	ON	RPTR = “L”	Repeater mode Disable	Initial value
RPTR	OFF	RPTR = “H”	Repeater mode Enable	
SW1-3	ON	SPEED = “L”	100 Mbps Disable	
SPEED	OFF	SPEED = “H”	100 Mbps Enable	Initial value
SW1-4	ON	DUPLEX = “L”	Full Duplex Disable	
DUPLEX	OFF	DUPLEX = “H”	Full Duplex Enable	Initial value
SW1-5	ON	ANE = “L”	Auto-negotiation Disable	
ANE	OFF	ANE = “H”	Auto-negotiation Enable	Initial value
SW1-6	ON	LDPS = “L”	LDPS mode Disable	Initial value
LDPS	OFF	LDPS “H”	LDPS mode Enable	

Note: SW1-2 should be set to Repeater mode Disable during the half-duplex mode of 10Base-T.

The LED1 to 5 indicate the status of Ethernet PHY controller mounted on the SH7670 CPU board. Thus, the communication state of Ethernet can be confirmed.

Table 2.7.2 lists the Ethernet communication state.

Table 2.7.2 Ethernet Communication State

Number	Light on/off	Description
LED1	On	Ethernet is being LINK UP
LINK	Off	Ethernet is being LINK UP
LED2	On	Ethernet is full duplex
DUPLEX	Off	Ethernet is half duplex
LED3	On	Ethernet is connected with 10BASE-T
10ACT	Off	Ethernet is not connected with 10BASE-T
LED4	On	Ethernet is connected with 100BASE-T
100ACT	Off	Ethernet is not connected with 100BASE-T
LED5	On	COLLISION is occurred on the communication of Ethernet
COLLISION	Off	COLLISION is not occurred on the communication of Ethernet

2.8 I/O Port

In the SH7670 CPU board, the I/O port of SH7670 is connected to the extension connector.

Moreover, some I/O port are connected to the DIP switch and LED for users to be used freely.

Figure 2.8.1 shows the I/O port block diagram, Table 2.8.1 lists the switch function, and Table 2.8.2 lists the I/O port function.

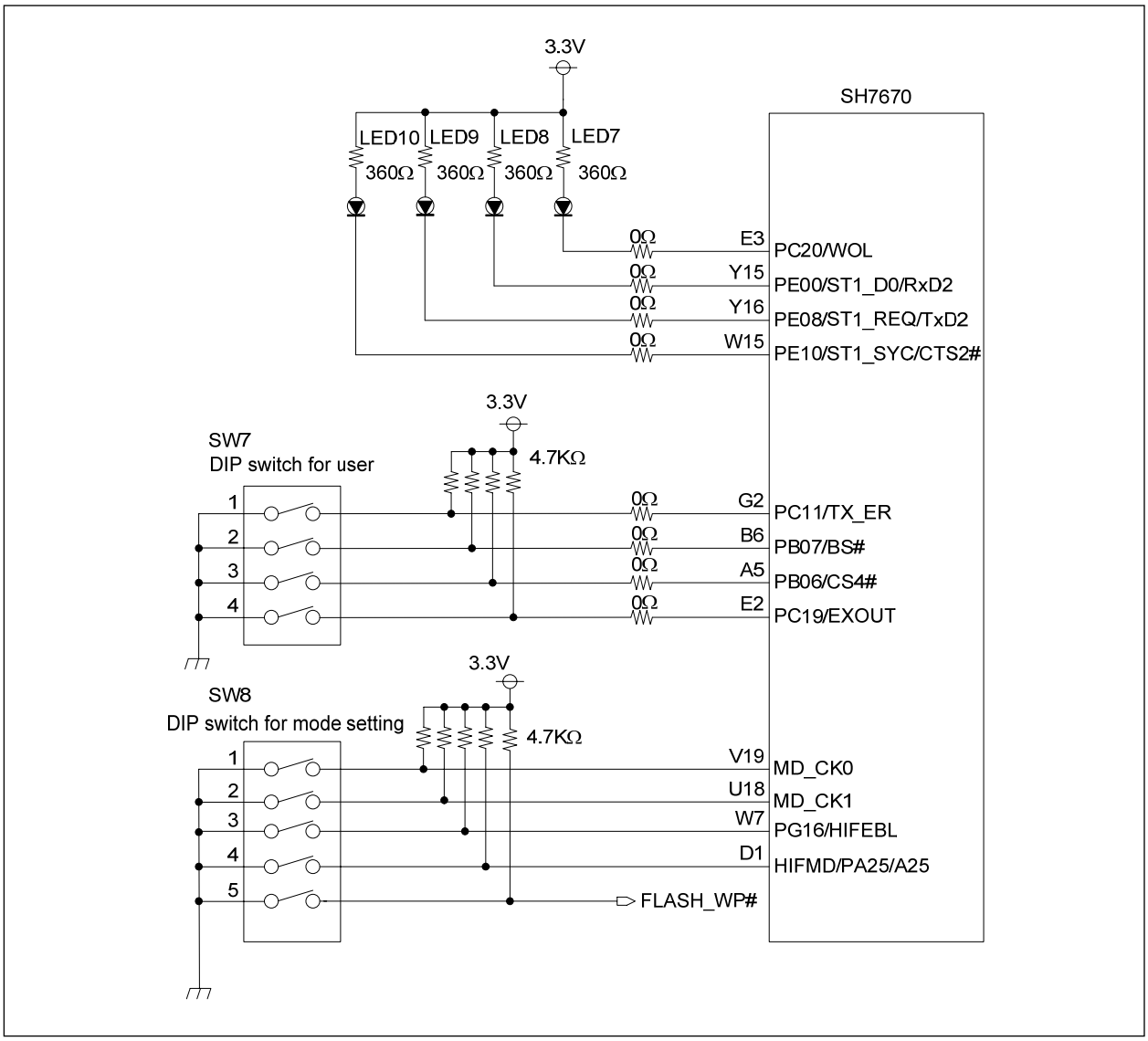


Figure 2.8.1 I/O Port Block Diagram

Table 2.8.1 Switch SW8 Function

Number	Setting		Function
SW1 MD_CK0	OFF	MD_CK0 = “H”	Mode / MD_CK0 / MD_CK1 0 / L / L 1 / H / L 3 / H / H
	ON	MD_CK0 = “L”	
SW2 MD_CK1	OFF	MD_CK1 = “H”	
	ON	MD_CK1 = “L”	
SW3 HIFEBL	OFF	HIFEBL = “H”	HIF pin is activated
	ON	HIFEBL = “L”	HIF is deactivated
SW4 HIFMD	OFF	HIFMD = “H”	Start-up from host interface (HIF)
	ON	HIFMD = “L”	Not start-up from host interface (HIF)
SW5 FLASH_WP#	OFF	FLASH_WP# = “H”	Write protect released on flash memory
	ON	FLASH_WP# = “L”	Write protect on flash memory

Table 2.8.2 I/O Port Function

SH7670 I/O Port Name	Connection on SH7670 CPU Board
PA17-PA23	Flash memory, Extension connector
PA24-PA25	Extension connector
PB00-PB01	EEPROM, Extension connector
PB02	SW, Extension connector
PB03-PB04	USB(VBUS) , Extension connector
PB05	Extension connector
PB06-PB07	SW, Extension connector
PC00-PC10,PC12-PC18	PHY-LSI, Extension connector
PC11,PC19	SW, Extension connector
PC20	LED, Extension connector
PD00-PD07	Extension connector
PE01-07,PE09,PE11	ST connector, Extension connector
PE00,PE08,PE10	LED, ST connector, Extension connector
PF01-PF02	RS232C, ST connector, Extension connector
PF00,PF03-PF11	ST connector, Extension connector
PG00-PG15,PG17-PG23	Extension connector (HIF)
PG16	SW, Extension connector (HIF)

2.9 Power Supply Circuit

In the SH7670 CPU board, 5V-power supply is input to the board to generate 3.3V and 1.2V by a regulator.

The regulator used is an output voltage variable type so that any voltage value can be generated by changing the resistance.

Figure 2.9.1 shows the block diagram of SH7670 CPU board power supply circuit.

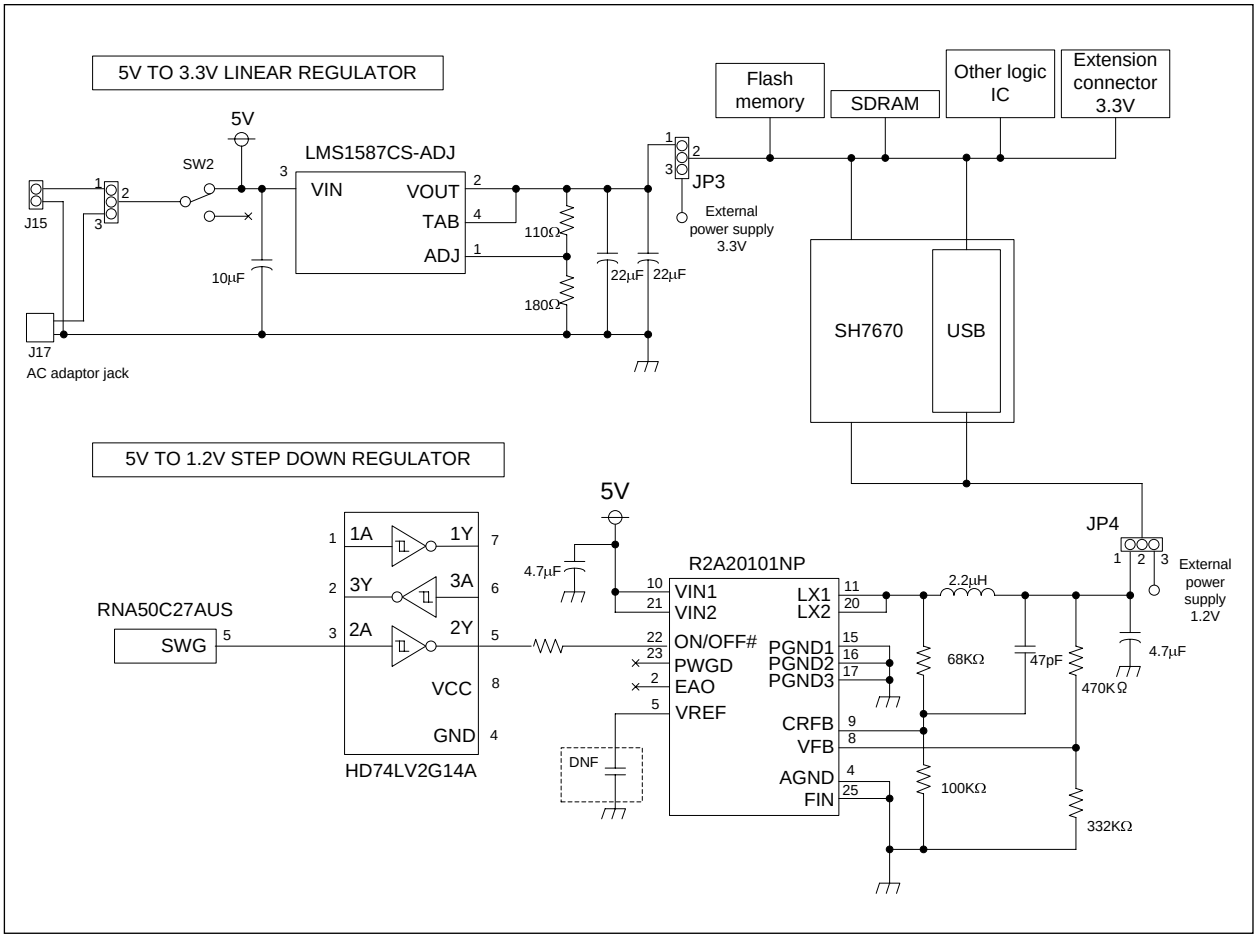


Figure 2.9.1 Power Supply Circuit Block Diagram

2.10 Clock Module

The clock module of SH7670 CPU board consists of two blocks.

• Output from oscillator is connected to SH7670 EXTAL

• Ceramic oscillator is connected to EXTAL and XTAL

The 16.67MHz oscillator is connected to this board.

The bus clock output from SH7670 is connected to SDRAM through dumping.

When an extension board is connected to an extension connector, it is recommended that the clock buffer with on-chip PLL is mounted to supply the stable clock signal.

Figure 2.10.1 shows the clock module block diagram.

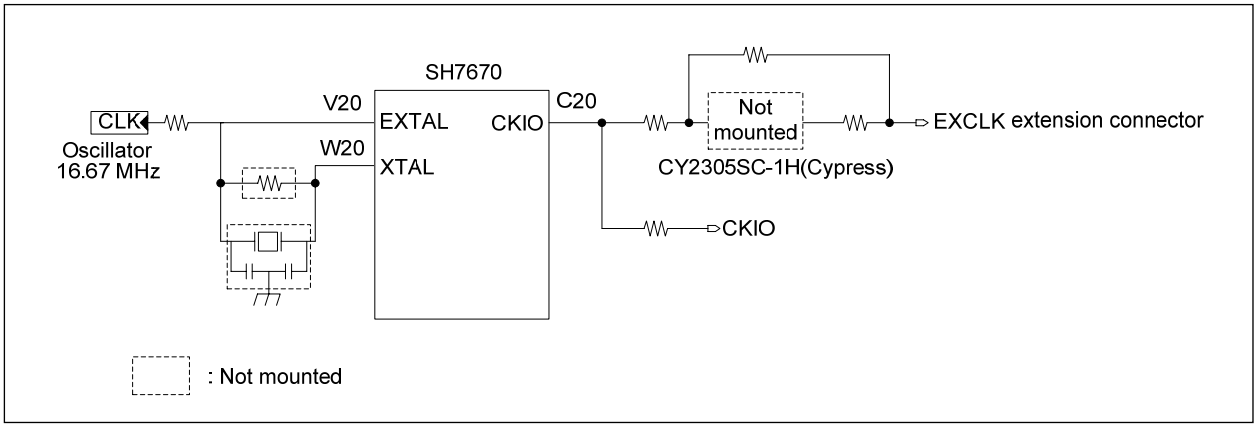


Figure 2.10.1 Clock Module Block Diagram

2.11 Reset Module

This module controls the SH7670 mounted on the SH7670 CPU board and the reset signal connected to flash memory and PHY-LSI.

Figure 2.11.1 shows the SH7670 CPU board reset module block diagram.

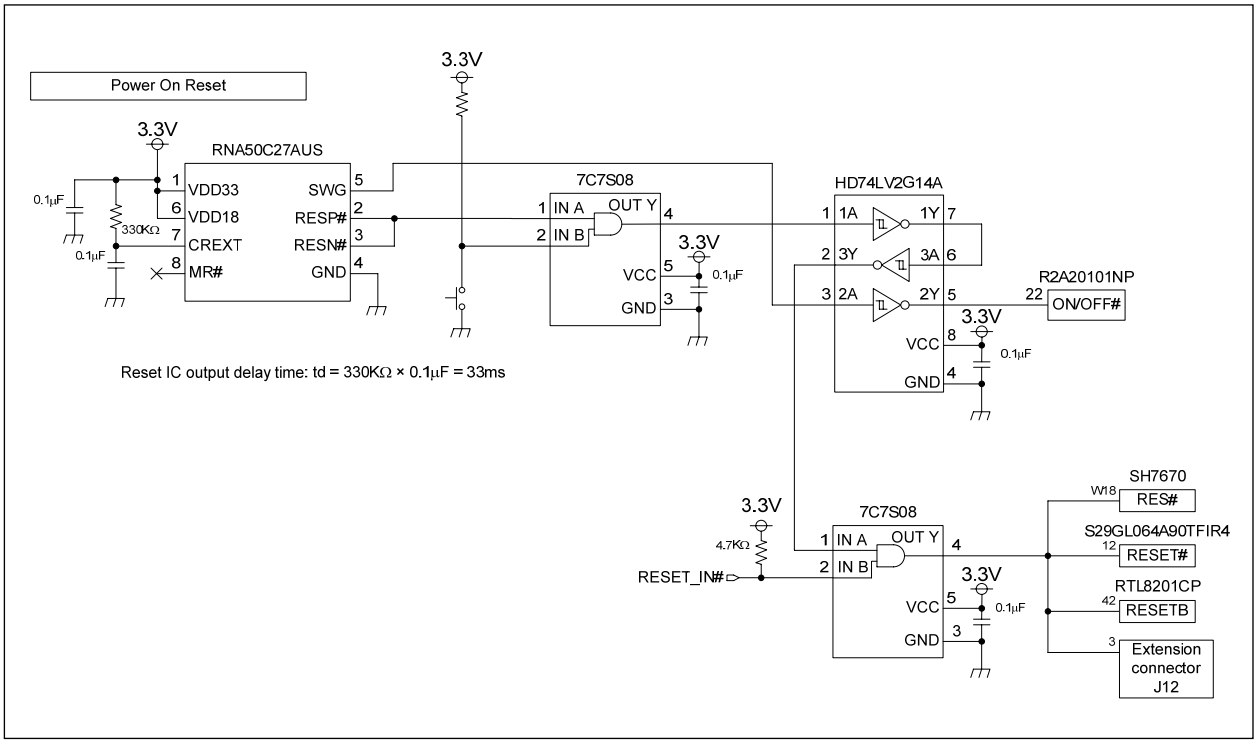


Figure 2.11.1 Reset Module Block Diagram

2.12 Interrupt Switch

In the SH7670 CPU board, the push switches are connected to the SH7670 NMI pin and IRQ0 pin.

Users can freely use the test switch by wiring a jumper on the TP pin.

Figure 2.12.1 shows the interrupt switch block diagram.

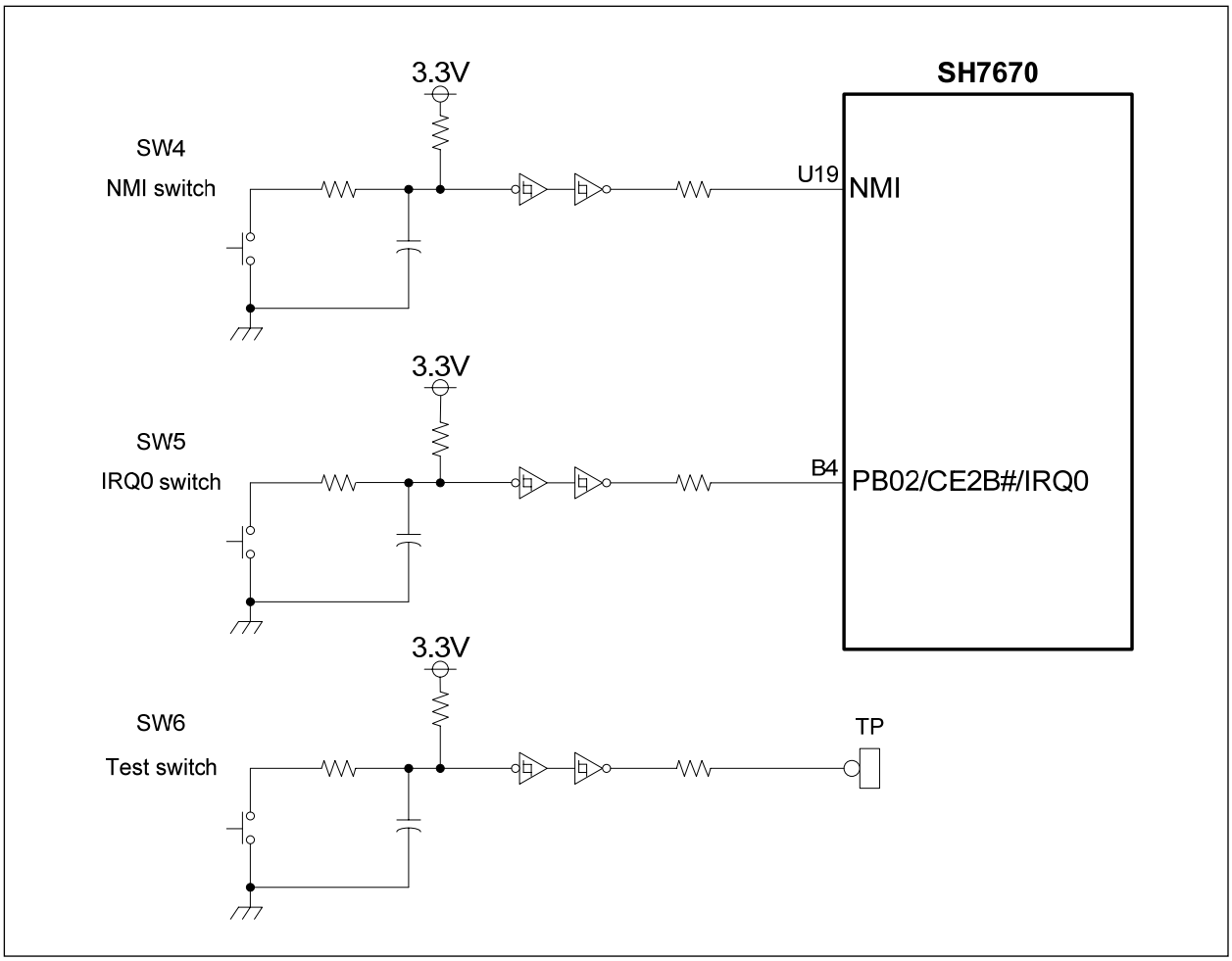


Figure 2.12.1 Interrupt Switch Block Diagram

2.13 E10A-USB Interface

The SH7670 CPU board contains a 14-pin H-UDI connector to connect to the E10A-USB.

Figure 2.13.1 shows the E10A-USB interface block diagram.

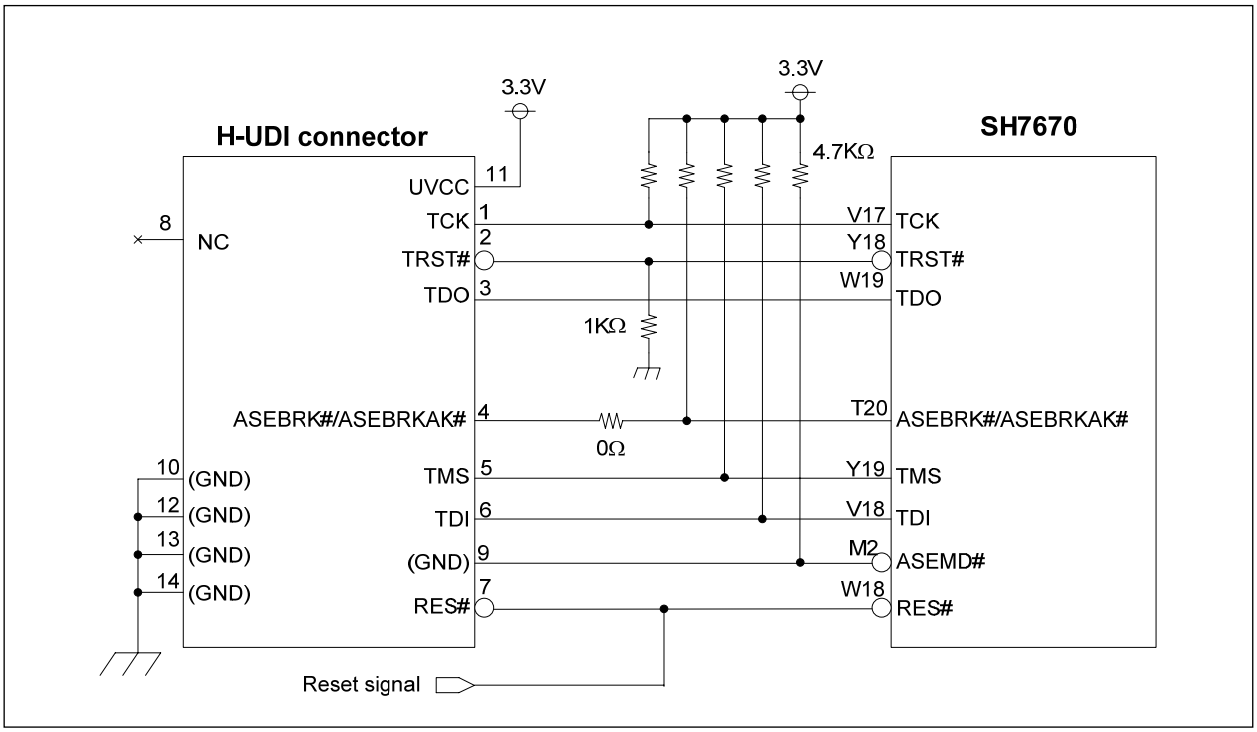


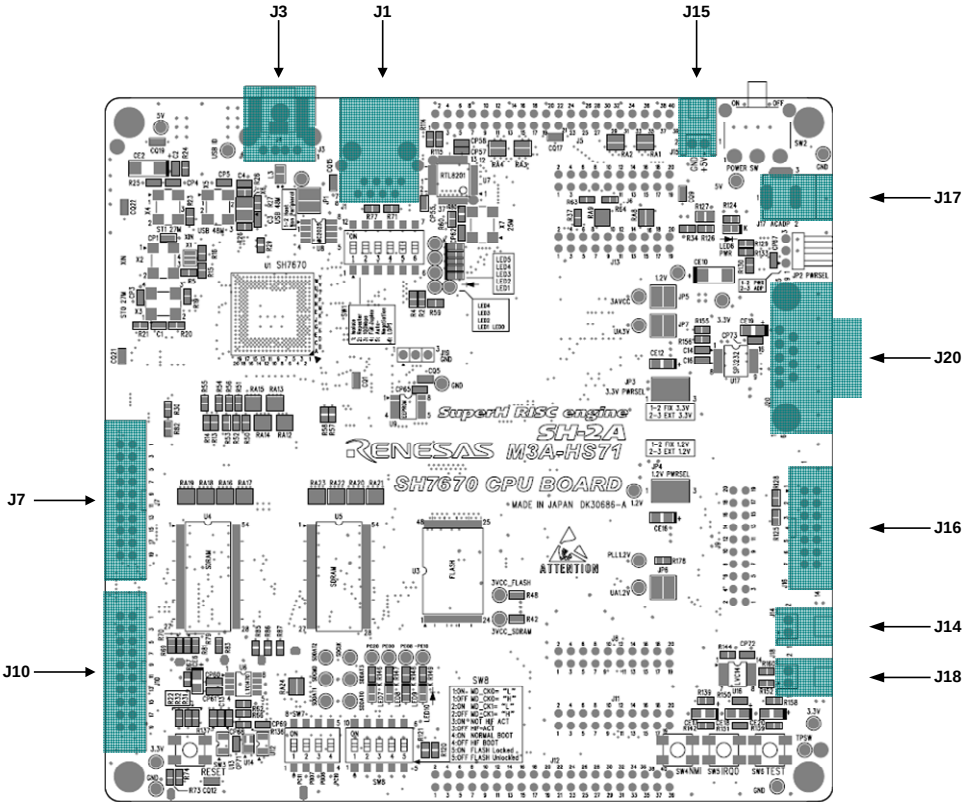
Figure 2.13.1 E10A-USB Interface Block Diagram

Chapter3
Operational Specifications

3.1 SH7670 CPU Board Connector Overview

Figure 3.1.1 shows the SH7670 CPU board connector assignments.

<Top view of the component side>



<Top view of the solder side>

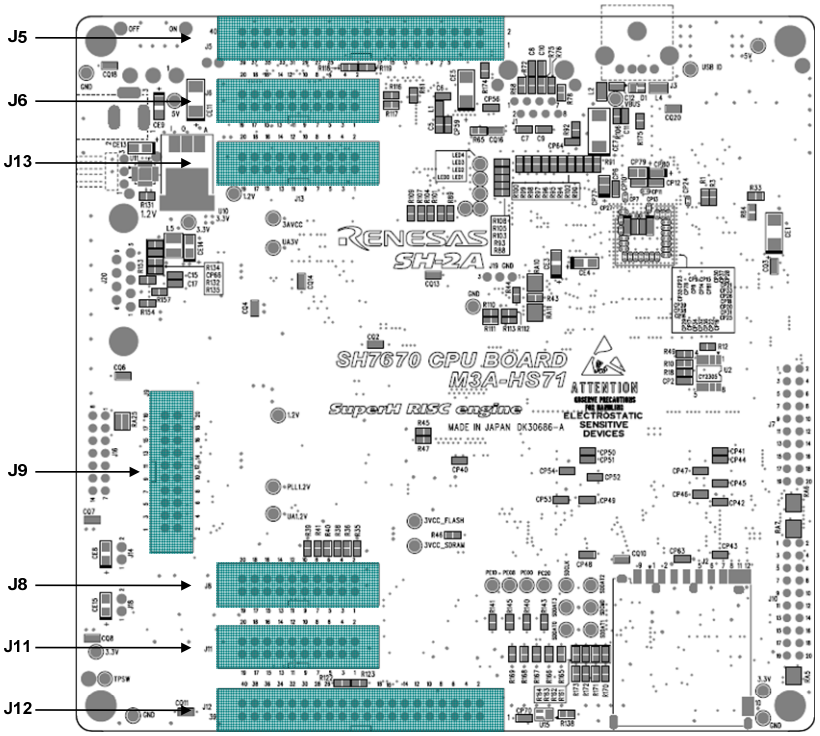


Figure 3.1.1 SH7670 CPU Board Connector Assignments

3.1.1 LAN Connector (J1)

The SH7670 CPU board includes the LAN connector (J1).

Figure 3.1.2 shows the LAN connector pin assignments (J1).

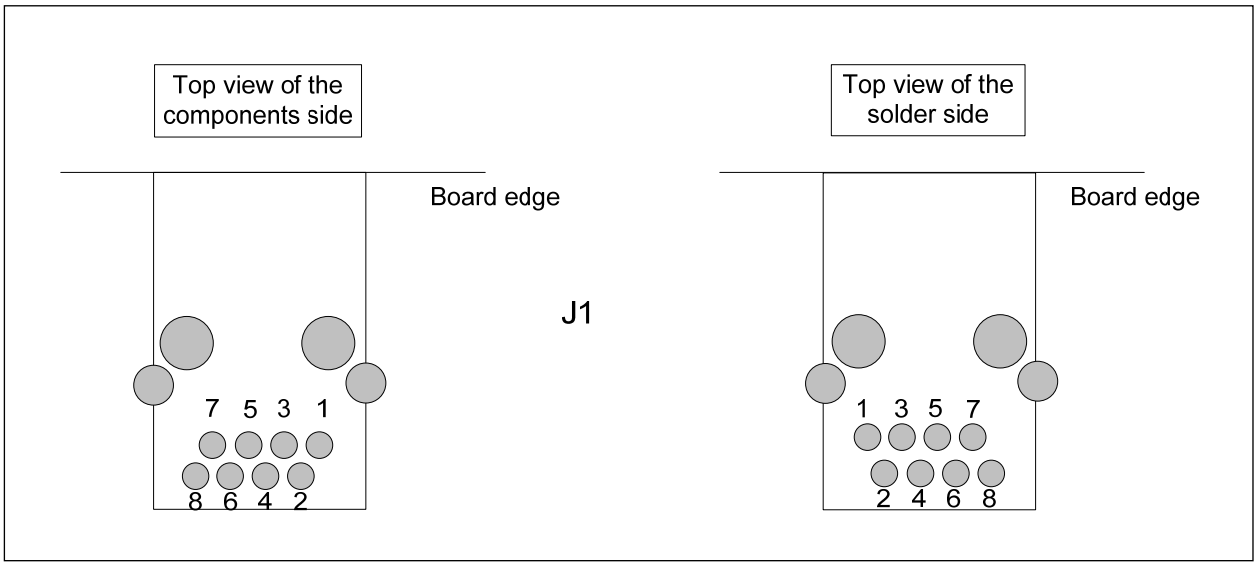


Figure 3.1.2 LAN Connector Pin Assignments (J1)

Table 3.1.1 lists the LAN connector pin assignments (J1).

Table 3.1.1 LAN Connector Pin Assignments (J1)

Pin	Signal Name	Pin	Signal Name
1	TD+	2	TD-
3	TCT	4	RD+
5	RD-	6	RCT
7	NC	8	NC

3.1.2USB Connector (J3)

The SH7670 CPU board includes the USB connector.

Figure 3.1.3 shows the USB connector pin assignments.

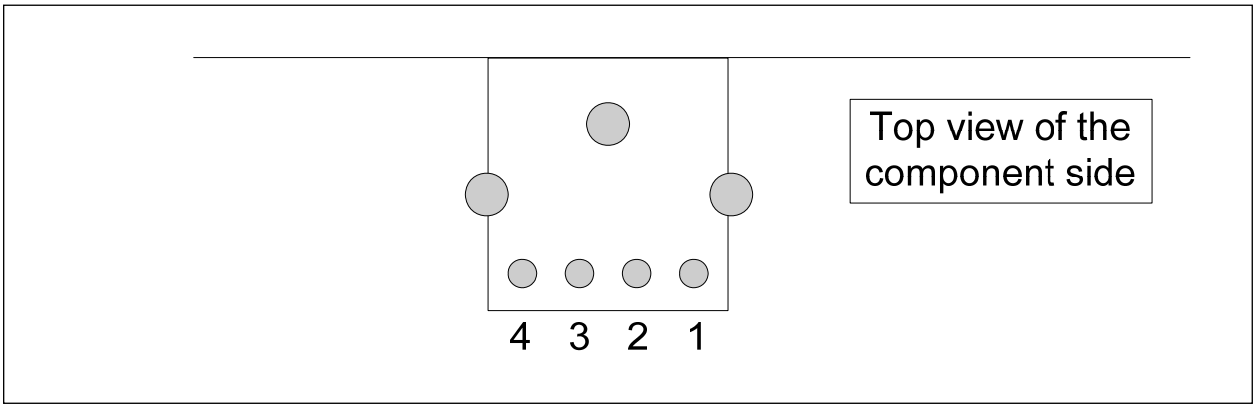


Figure 3.1.3 USB Connector Pin Assignments (J3)

Table 3.1.2 lists the USB connector pin assignments (J3).

Table 3.1.2 USB Connector Pin Assignments (J3)

Pin	Signal Name	Pin	Signal Name
1	VBUS	2	DM
3	DP	4	GND

3.1.3 Extension Connector (J5,J6,J8,J9,J11,J12, and J13)

The SH7670 CPU board has the through-holes for mounting extension connectors which I/O pin of SH7670 is connected. The MIL standard connector can be mounted on J5, J6, J8, J9, J11, J12, and J13 so that it can be used for the connection with extension board, the monitoring of SH7670 bus signal and so forth.

Figure 3.1.4 shows the extension connector pin assignments.

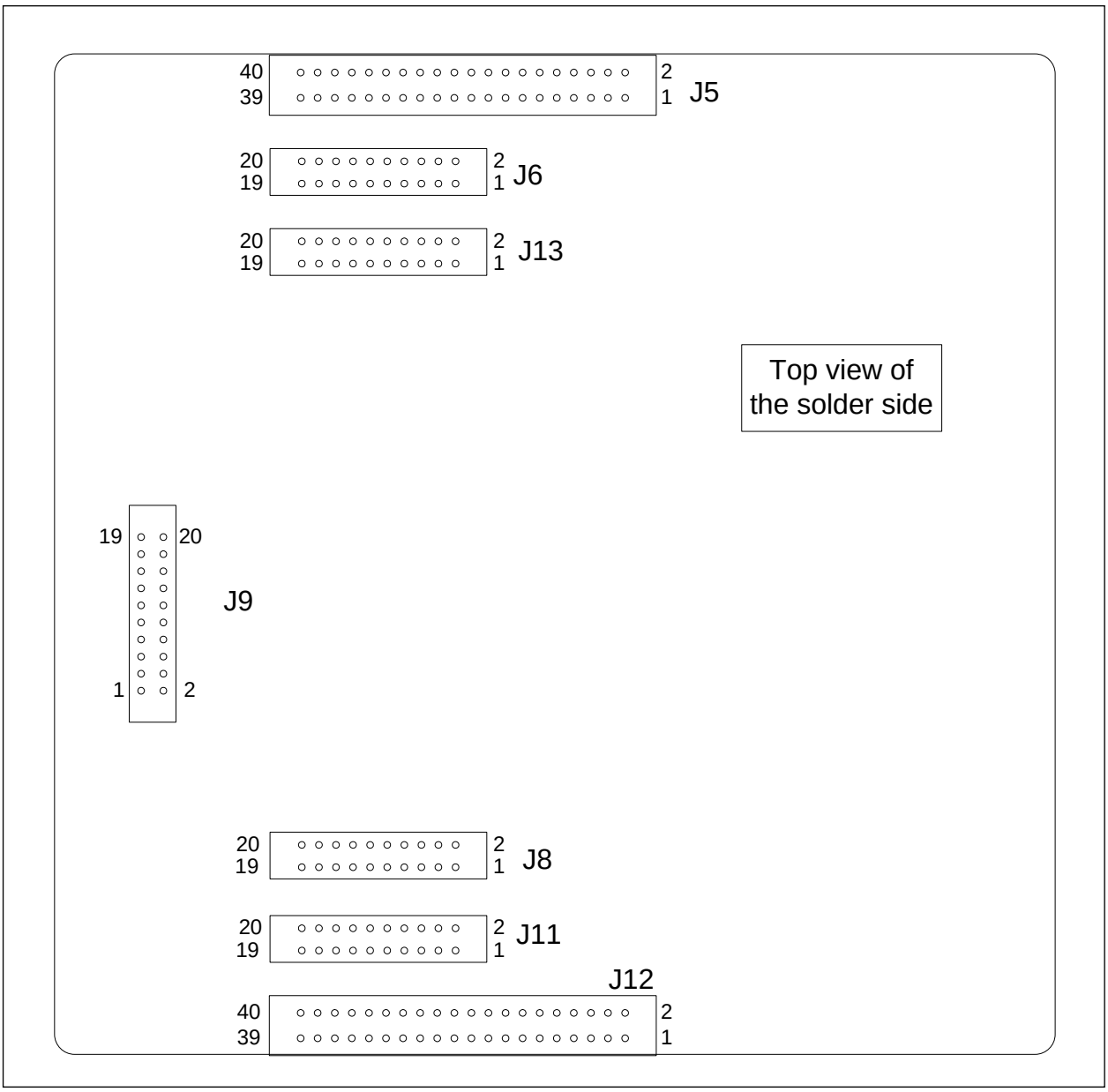


Figure 3.1.4 Extension Connector Pin Assignments

Table 3.1.3 to Table 3.1.9 list the extension connector pin assignments (J5,J6,J8,J9,J11,J12, and J13).

Table 3.1.3 Extension Connector Pin Assignments (J5)

Pin	Signal Name	Pin	Signal Name
1	+5V	2	+5V
3	NC	4	D31
5	D30	6	D29
7	D28	8	D27
9	D26	10	D25
11	D24	12	D23
13	D22	14	D21
15	D20	16	D19
17	D18	18	D17
19	D16	20	GND
21	+5V	22	+5V
23	NC	24	D15
25	D14	26	D13
27	D12	28	D11
29	D10	30	D09
31	D08	32	D07
33	D06	34	D05
35	D04	36	D03
37	D02	38	D01
39	D00	40	GND

Table 3.1.4 Extension Connector Pin Assignments (J6)

Pin	Signal Name	Pin	Signal Name
1	+1.2V	2	+1.2V
3	PC17/MDC	4	PC16/MDIO
5	PC15/CRS	6	PC14/COL
7	PC13/TX_CLK	8	PC12/TX_EN
9	PC10/RX_CLK	10	PC09/RX_ER
11	PC08/RX_DV	12	PC07/MII_TXD3
13	PC06/MII_TXD2	14	PC05/MII_TXD1
15	PC04/MII_TXD0	16	PC03/MII_RXD3
17	PC02/MII_RXD2	18	PC01/MII_RXD1
19	PC00/MII_RXD0	20	GND

Table 3.1.5 Extension Connector Pin Assignments (J8)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	PG23/HIFCS#	4	PG22/HIFRS
5	PG21/HIFWR#	6	PG19/HIFINT#
7	PG18/HIFDREQ	8	PG17/HIFRDY
9	PG16/HIFEBL	10	NC
11	PB05/CS5#/CE1A#/IRQ3/TEND1	12	PD07/IRQ7#/SDCLK
13	PD06/IRQ6#/SDCMD	14	PD05/IRQ5#/SDCD
15	PD04/IRQ4#/SDWP	16	PD03/IRQ3#/SDDAT3
17	PD02/IRQ2#/SDDAT2	18	PD01/IRQ1#/SDDAT1
19	PD00/IRQ0#/SDDAT0	20	GND

Table 3.1.6 Extension Connector Pin Assignments (J9)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	CKIO	4	PB07/BS#
5	PB06/CS4#	6	PB04/CE2A#/IRQ2/DACK1
7	PB03/CS6#/CE1B#/IRQ1/DREQ1	8	PB02/CE2B#/IRQ0
9	PB01/IOIS16#/SCL	10	PB00/WAIT#/SDA
11	CS3#	12	RAS#
13	CAS#	14	CKE
15	RD/WR#	16	WE3#/DQMUU/ICIOWR#
17	WE2#/DQMUL/ICIORD#	18	WE1#/DQMLU/WE#
19	WE0#/DQMLL	20	GND

Table 3.1.7 Extension Connector Pin Assignments (J11)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	PC20/WOL	4	PC18/LNKSTA
5	PC19/EXOUT	6	PC11/TX_ER
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	ST1_VCO_CLKIN/AUDIO_CLK	14	ST1_CLKIN/SSISCK1
15	ST0_CLKIN/SSISCK0	16	PE07/ST1_D7/SSIWS1
17	PF07/ST0_D7/SSIWS0	18	PE06/ST1_D6/SSIDATA1
19	PF06/ST0_D6/SSIDATA0	20	GND

Table 3.1.8 Extension Connector Pin Assignments (J12)

Pin	Signal Name	Pin	Signal Name
1	+3.3V	2	+3.3V
3	RES#	4	RESET_IN#
5	RD#	6	CS0#
7	WDTOVF#	8	NC
9	NC	10	NC
11	HIFMD/PA25/A25	12	PA24/A24
13	PA23/A23	14	PA22/A22
15	PA21/A21	16	PA20/A20
17	PA19/A19	18	PA18/A18
19	PA17/A17	20	GND
21	+3.3V	22	+3.3V
23	A16	24	A15
25	A14	26	A13
27	A12	28	A11
29	A10	30	A09
31	A08	32	A07
33	A06	34	A05
35	A04	36	A03
37	A02	38	A01
39	A00	40	GND

Table 3.1.9 Extension Connector Pin Assignments (J13)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	PG20/HIFRD#	4	PG15/HIFD15
5	PG14/HIFD14	6	PG13/HIFD13
7	PG12/HIFD12	8	PG11/HIFD11
9	PG10/HIFD10	10	PG09/HIFD09
11	PG08/HIFD08	12	PG07/HIFD07
13	PG06/HIFD06	14	PG05/HIFD05
15	PG04/HIFD04	16	PG03/HIFD03
17	PG02/HIFD02	18	PG01/HIFD01
19	PG00/HIFD00	20	GND

3.1.4 STIF Connector (J7,J10)

The SH7670 CPU board includes the STIF connector to which the SH7670 output pin is connected.

The MIL standard connector can be mounted on J7 and J10.

Figure 3.1.5 shows the pin assignments of STIF connector.

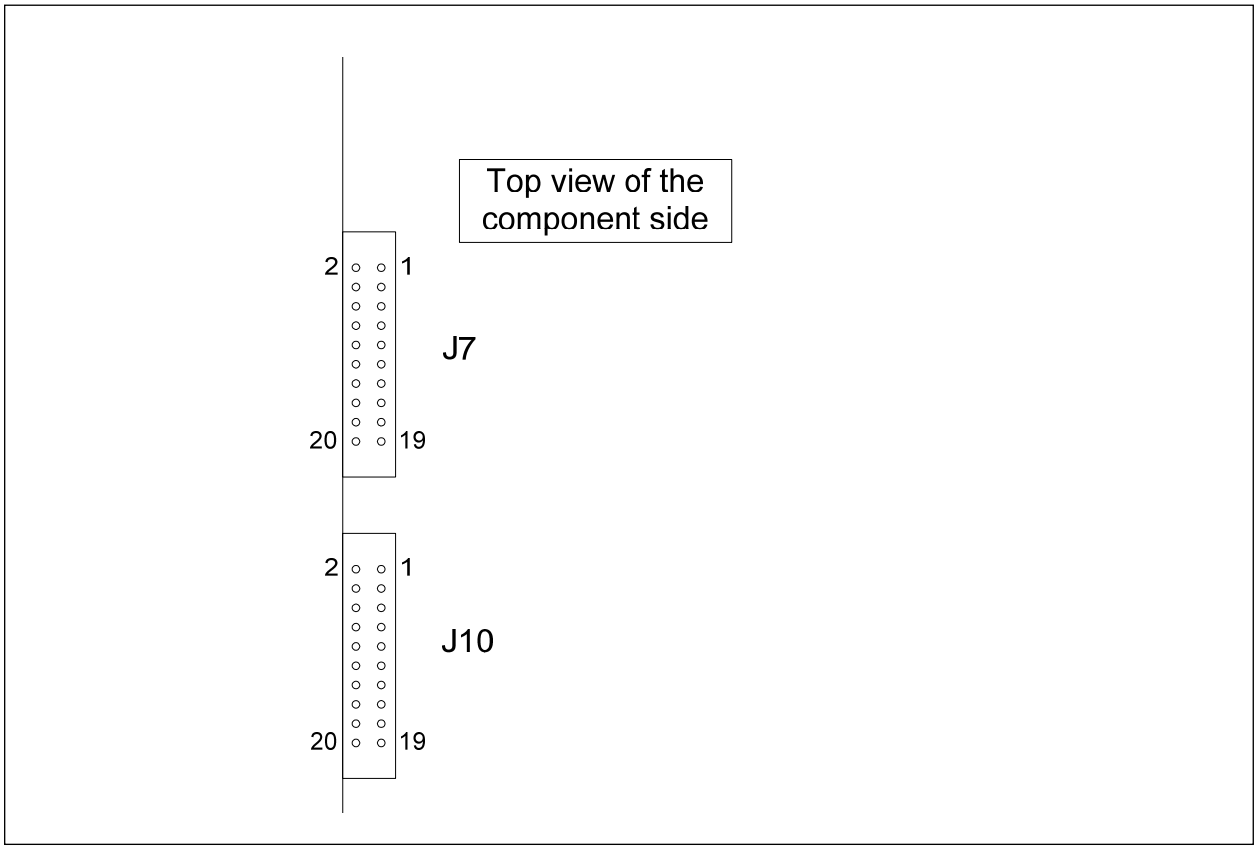


Figure 3.1.5 Pin Assignment of STIF Connector

Table 3.1.10 lists the pin assignments of STIF connector (J7).

Table 3.1.10 Pin Assignment of STIF Connector (J7)

Pin	Signal Name	Pin	Signal Name
1	ST0_CLKIN/SSISCK0	2	ST_CLKOUT
3	PF00/ST0_D0	4	PF02/ST0_D2/RxD0
5	PF04/ST0_D4/CTS0#	6	PF06/ST0_D6/SSIDATA0
7	NC	8	GND
9	GND	10	NC
11	PF07/ST0_D7/SSIWS0	12	PF05/ST0_D5/RTS0#
13	PF03/ST0_D3/SCK0	14	PF01/ST0_D1/TxD0
15	PF10/ST0_SYC/DACK0	16	PF09/ST0_VLD/DREQ0
17	PF11/ST0_PWM/TEND0	18	PF08/ST0_REQ
19	ST0_VCO_CLKIN	20	GND

Table 3.1.11 lists the pin assignments of STIF connector (J10).

Table 3.1.11 Pin Assignment of STIF Connector (J10)

Pin	Signal Name	Pin	Signal Name
1	ST1_CLKIN/SSISCK1	2	ST_CLKOUT
3	PE00/ST1_D0/RxD2	4	PE02/ST1_D2/RxD1
5	PE04/ST1_D4/CTS1#	6	PE06/ST1_D6/SSIDATA1
7	NC	8	GND
9	GND	10	NC
11	PE07/ST1_D7/SSIWS1	12	PE05/ST1_D5/RTS1#
13	PE03/ST1_D3/SCK1	14	PE01/ST1_D1/TxD1
15	PE10/ST1_SYC/CTS2#	16	PE09/ST1_VLD/SCK2
17	PE11/ST1_PWM/RTS2#	18	PE08/ST1_REQ/TxD2
19	ST1_VCO_CLKIN/AUDIO_CLK	20	GND

3.1.5 External Power Supply Connector (J14 and J18)

The SH7670 CPU board has the through-holes for the external power supply connector (J14: 3.3V supply, J18: 1.2V supply) for SH7670.

Figure 3.1.6 shows the pin assignments of external power supply connector (J14 and J18).

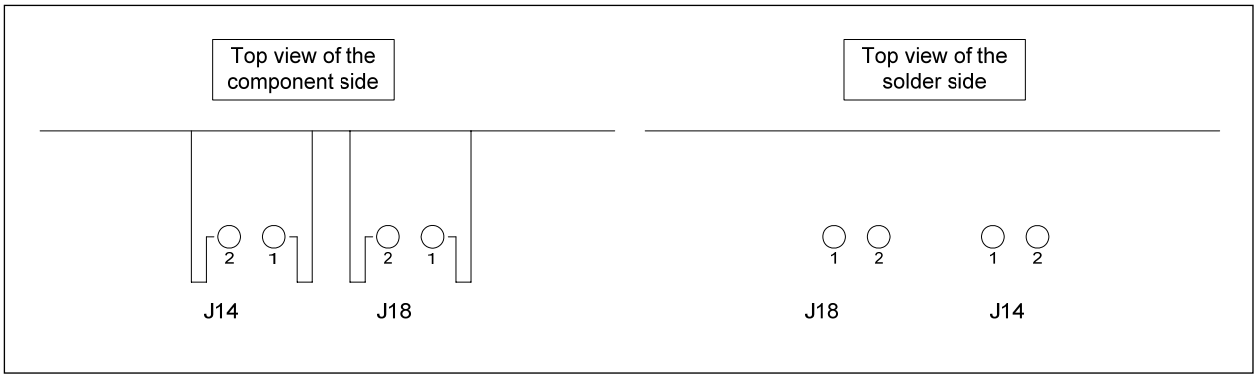


Figure 3.1.6 Pin Assignments of External Power Supply Connector (J14 and J18)

Table 3.1.12 and Table 3.1.13 list the pin assignments of external power supply connector (J14 and J18).

Table 3.1.12 Pin Assignments of External Power Supply Connector (J14)

Pin	Signal Name	Pin	Signal Name
1	+3.3V	2	GND

Table 3.1.13 Pin Assignments of External Power Supply Connector (J18)

Pin	Signal Name	Pin	Signal Name
1	+1.2V	2	GND

3.1.6 Power Supply Connector (J15)

The SH7670 CPU board includes the connector for power supply.

Figure 3.1.7 shows the pin assignment of power supply connector (J15).

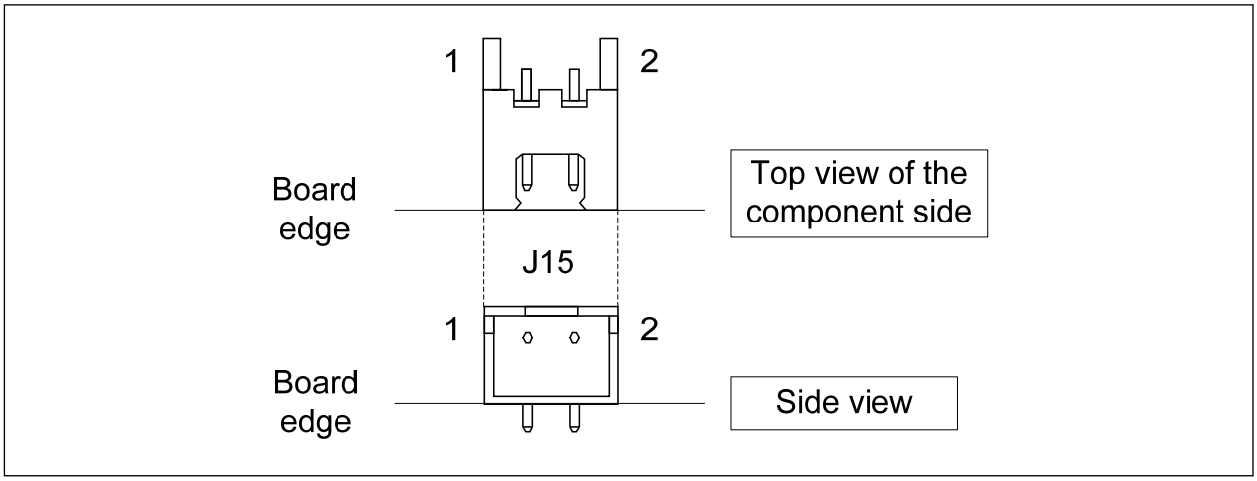


Figure 3.1.7 Pin Assignment of Power Supply Connector (J15)

Table 3.1.14 lists the pin assignment of power supply connector (J15).

Table 3.1.14 Pin Assignment of Power Supply Connector (J15)

Pin	Signal Name	Pin	Signal Name
1	+5V	2	GND

3.1.7 H-UDI Connector (J16)

The SH7670 CPU board includes the H-UDI (J16) connector for E10A-USB emulator connection.

Figure 3.1.8 shows the pin assignment of H-UDI connector (J16).

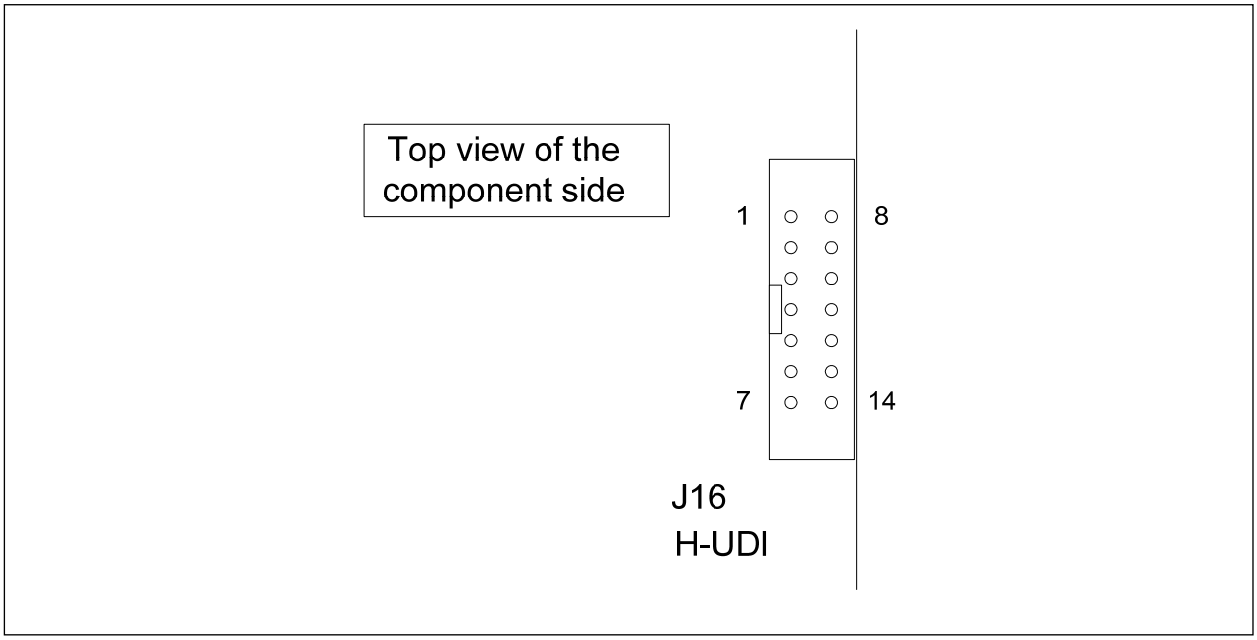


Figure 3.1.8 Pin Assignment of H-UDI Connector (J16)

Table 3.1.15 lists the pin assignment of H-UDI connector (J16).

Table 3.1.15 Pin Assignment of H-UDI Connector (J16)

Pin	Signal Name	Pin	Signal Name
1	TCK	2	TRST#
3	TDO	4	N.C.
5	TMS	6	TDI
7	RESET#	8	N.C.
9	(GND) ASEMD#	10	GND
11	UVCC	12	GND
13	GND	14	GND

3.1.8 UART Connector (J20)

The SH7670 CPU board includes the UART connector (J20).

Figure 3.1.9 shows the pin assignment of UART connector (J20).

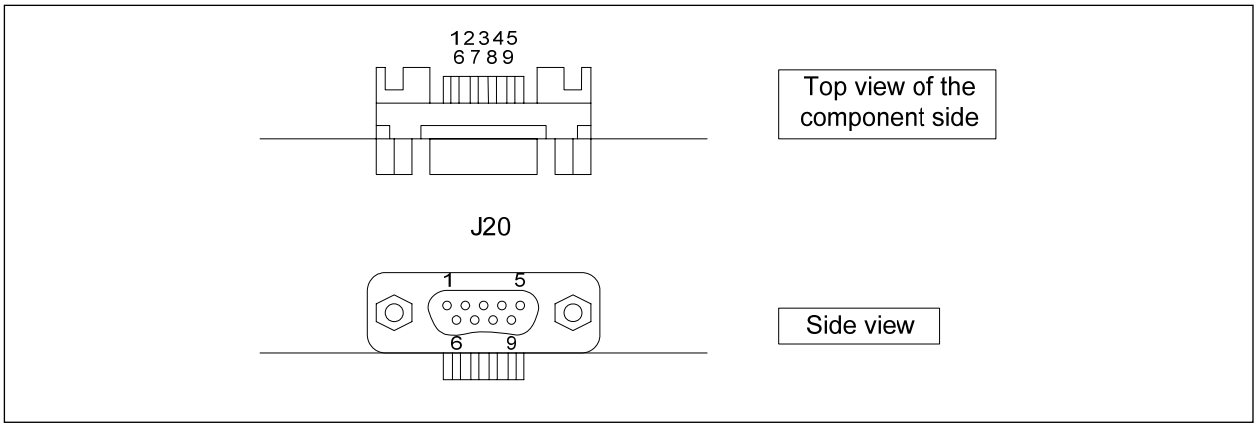


Figure 3.1.9 Pin Assignment of UART Connector (J20)

Table 3.1.16 lists the pin assignment of UART connector (J20).

Table 3.1.16 Pin Assignment of UART Connector (J20)

Pin	Signal Name	Pin	Signal Name
1	NC	2	RXD(PF02/ST0_D2/RXD0)
3	TXD(PF01/ST0_D1/TXD0)	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	NC		

Pins 4-6 are loop back-connected. Pins 7-8 are loop back-connected.

3.2 Switch and LED Outline

The SH7670 CPU board includes switches and LEDs as its operational components. Figure 3.2.1 shows the assignment of SH7670 CPU board operational components.

<Top view of the component side>

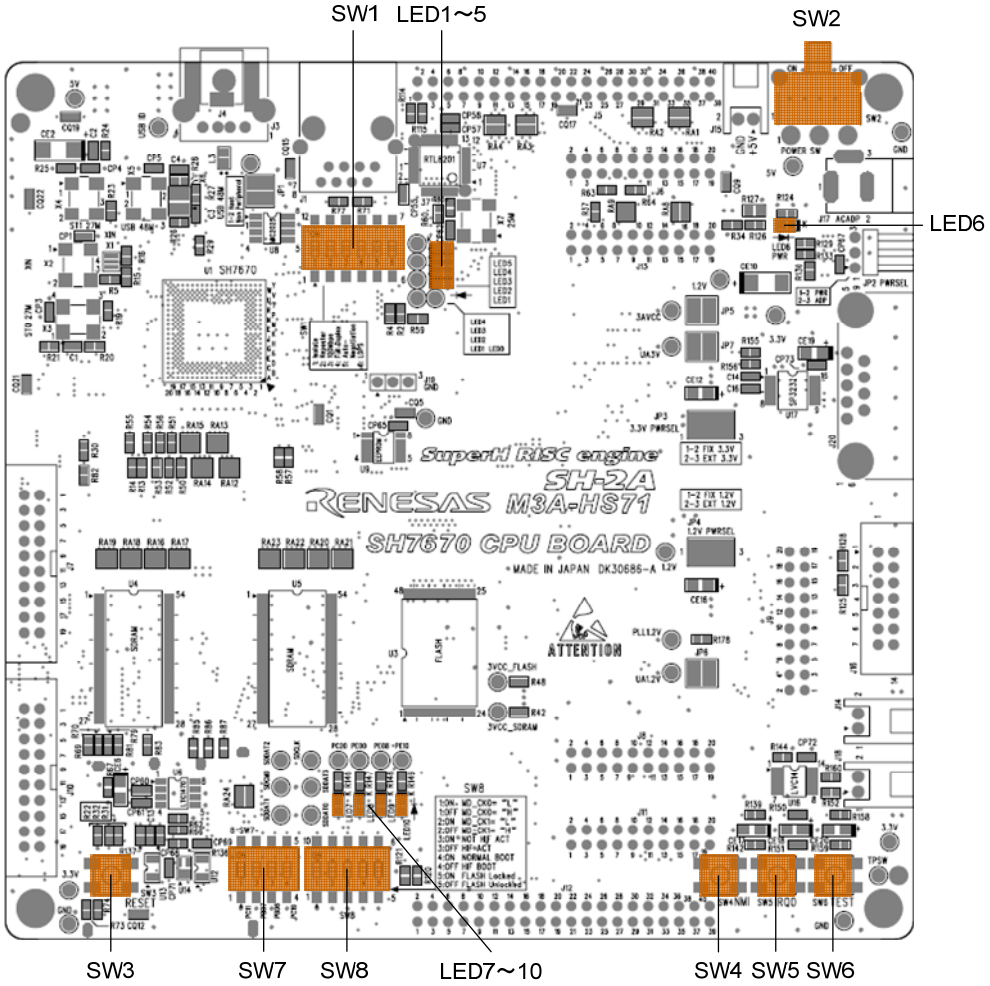


Figure 3.2.1 SH7670 CPU Board Operational Component Assignment

3.2.1 Jumper (JP1~JP7)

The SH7670 CPU board includes seven jumpers.

Figure 3.2.2 shows the assignment of SH7670 CPU board jumpers (JP1~JP7), and Table 3.2.1~Table 3.2.3 list the SH7670 CPU board jumper settings (JP1~JP7).

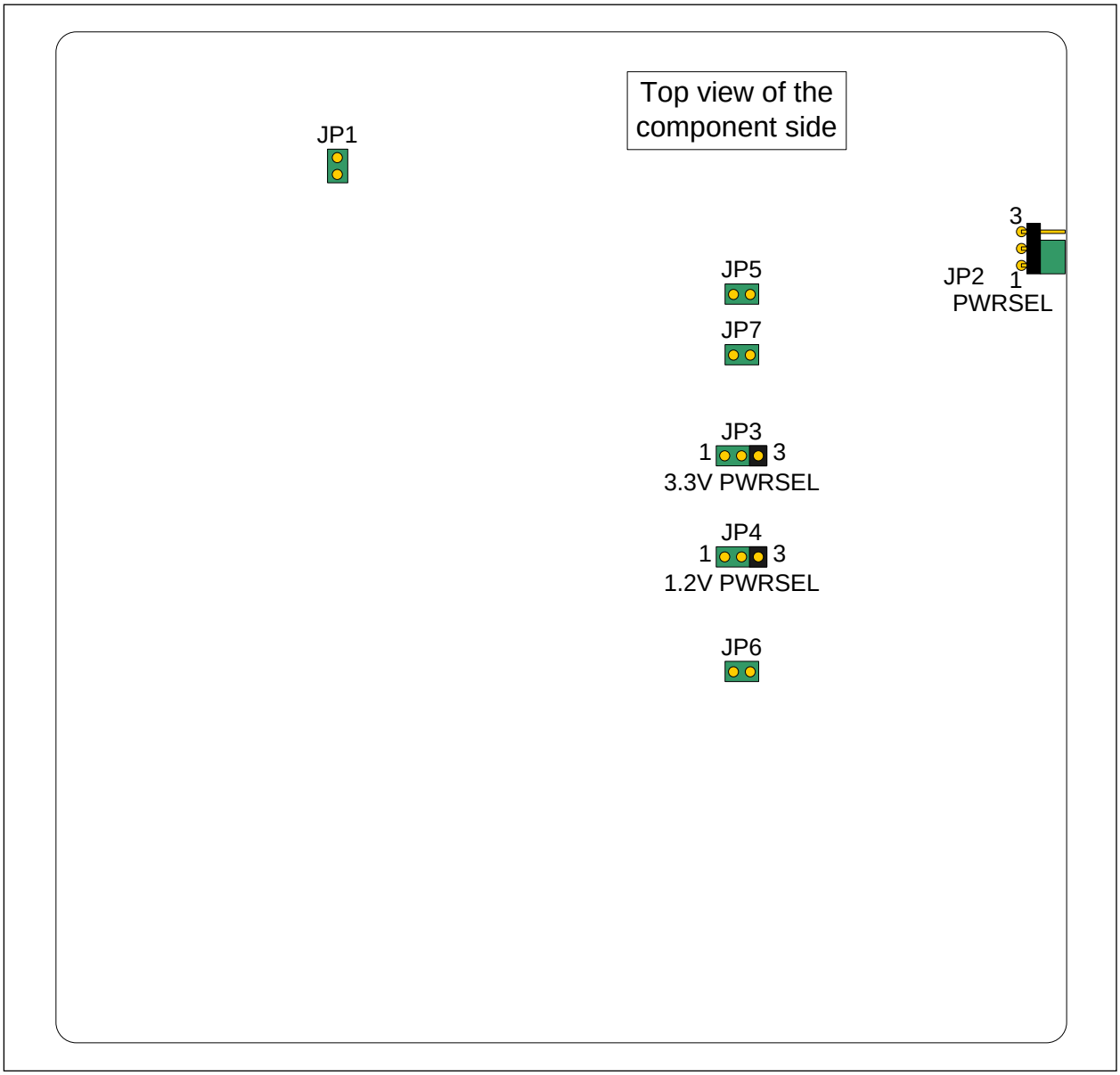


Figure 3.2.2 Assignment of SH7670 CPU board Jumpers (JP1~JP7)

Table 3.2.1 Jumper Setting for USB Module (JP1)

Jumper	Setting	Function
JP1	1-2	USB HOST mode [VBUS power is supplied]
	None (Open)	USB Function mode [VBUS power is not supplied]

Table 3.2.2 Jumper Setting for SH7670 Power Supply Switch (JP2,JP3,JP4)

Jumper	Setting	Function
JP2 PWRSEL	1-2	External power supply voltage (Supplied from J15)
	2-3	External power supply voltage (Supplied from J17)
JP3 3.3V PWRSEL	1-2	3.3V fixed power supply voltage (Supplied from U10)
	2-3	External power supply voltage (Supplied from J14)
JP4 1.2V PWRSEL	1-2	1.2V fixed power supply voltage (Supplied from U11)
	2-3	External power supply voltage (Supplied from J18)

Table 3.2.3 Jumper Setting for Analog Power Supply (JP5,JP6,JP7)

Jumper	Setting	Function
JP5	1-2	Power for PHY analog 3.3V (AVDD33) is supplied
	None (Open)	Power for PHY analog 3.3V (AVDD33) is not supplied
JP6	1-2	Power for USB analog 1.2V (AV12) is supplied
	None (Open)	Power for USB analog 1.2V (AV12) is not supplied
JP7	1-2	Power for USB analog 3.3V (AV33) is supplied
	None (Open)	Power for USB analog 3.3V (AV33) is not supplied

indicates the default.

Note: Do not change jumper settings during the operation of SH7670 CPU board. Ensure to turn off the power of the SH7670 CPU board before changing jumper settings.

3.2.2 Switch and LED Functions

The SH7670 CPU board includes eight switches and ten LEDs.

Figure 3.2.3 shows the pin assignment of switches and LEDs mounted on SH7670 CPU board, and Table 3.2.4 lists the switches mounted on SH7670 CPU board.

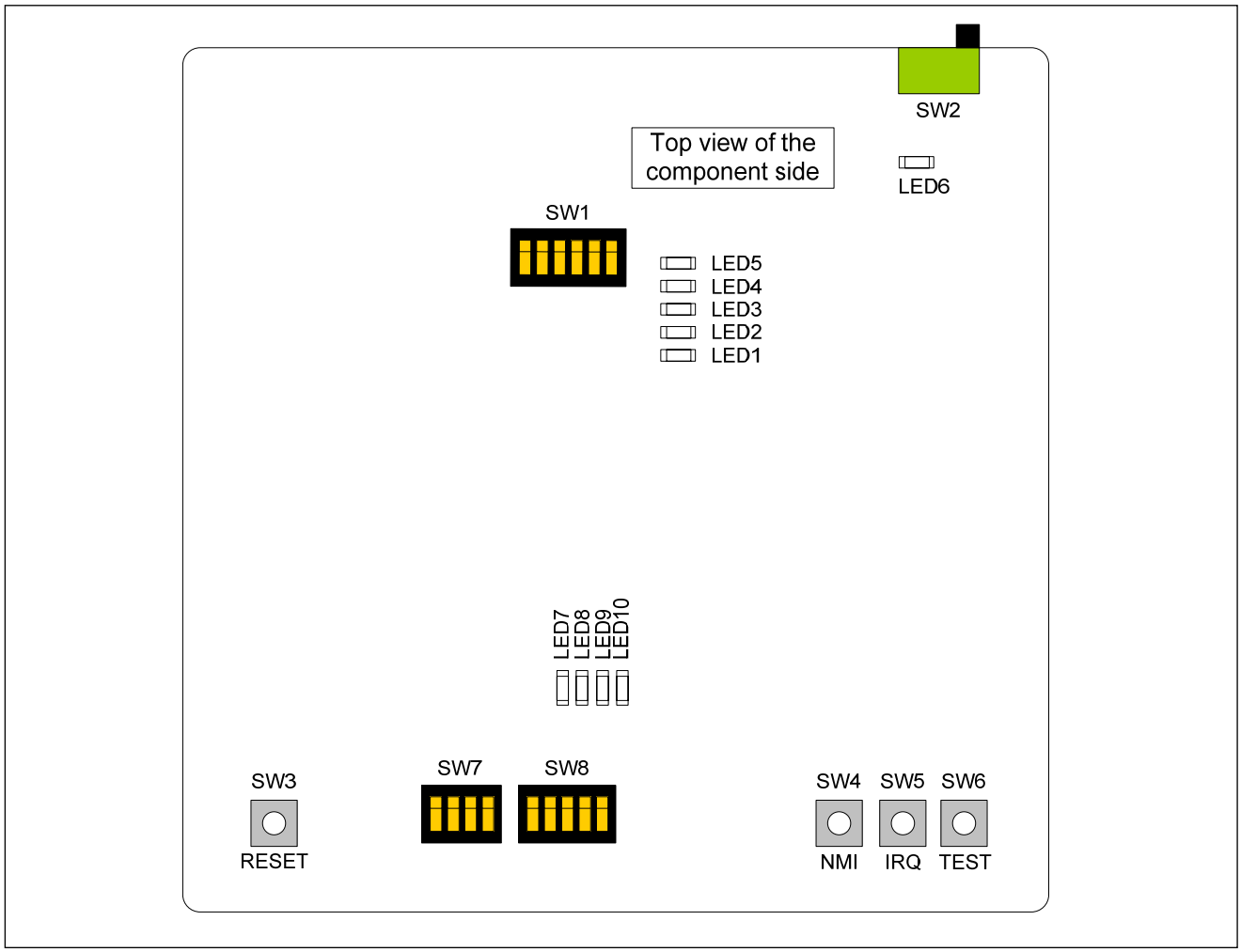


Figure 3.2.3 Pin Assignment of Switches and LEDs on SH7670 CPU board

Table 3.2.4 Switches on SH7670 CPU board

No.	Function	Remarks
SW1	Switch for PHY controller operation setting	Refer to Table 3.2.6 for the functions
SW2	System power on/off switch	-
SW3	System reset input switch	See section 2.12 for details.
SW4	NMI interrupt switch	See section 2.13 for details.
SW5	IRQ0 switch	See section 2.13 for details.
SW6	TEST switch	See section 2.13 for details.
SW7	DIP switch for user (4-pole) 1 PC11/TX_ER 2 PB07/BS# 3 PB06/CS4# 4 PC19/EXOUT OFF for all 4-pole: “H”, ON: ”L”	PB06,PB07,PC11, and PC19 are pulled up. See section 2.9 for details.
SW8	Switch for data mode setting	Refer to Table 3.2.5 for the functions

Table 3.2.5 lists the functions of switch SW8.

Table 3.2.6 lists the functions of switch SW1.

indicates the default.

Table 3.2.5 Data Mode Setting Switch Function

No.	Setting		Function
SW8-1 MD_CK0	OFF	MD_CK0 = “H”	Mode / MD_CK0 / MD_CK1 0 / L / L 1 / H / L 3 / H / H
	ON	MD_CK0 = “L”	
SW8-2 MD_CK1	OFF	MD_CK1 = “H”	
	ON	MD_CK1 = “L”	
SW8-3 HIFEBL	OFF	HIFEBL = “H”	Activation of HIF pin
	ON	HIFEBL = “L”	Cancel activation of HIF pin
SW8-4 HIFMD	OFF	HIFMD = “H”	Activate from host interface (HIF)
	ON	HIFMD = “L”	Not activate from host interface (HIF)
SW8-5 FLASH_WP#	OFF	FLASH_WP# = “H”	Cancel write protection for flash memory
	ON	FLASH_WP# = “L”	Write protection for flash memory

Table 3.2.6 PHY Controller Operation Mode Setting Switch Function

No.	Setting		Function
SW1-1 ISOLATE	ON	ISOLATE = “L”	Isolate Disable
	OFF	ISOLATE = “H”	Isolate Enable
SW1-2 RPTR	ON	RPTR = “L”	Repeater mode Disable
	OFF	RPTR = “H”	Repeater mode Enable
SW1-3 SPEED	ON	SPEED = “L”	100Mbps Disable
	OFF	SPEED = “H”	100Mbps Enable
SW1-4 DUPLEX	ON	DUPLEX = “L”	Full Duplex Disable
	OFF	DUPLEX = “H”	Full Duplex Enable
SW1-5 ANE	ON	ANE = “L”	Auto-negotiation Disable
	OFF	ANE = “H”	Auto-negotiation Enable
SW1-6 LDPS	ON	LDPS = “L”	LDPS mode Disable
	OFF	LDPS “H”	LDPS mode Enable

Table 3.2.7 lists the functions of LEDs mounted on SH7670 CPU board.

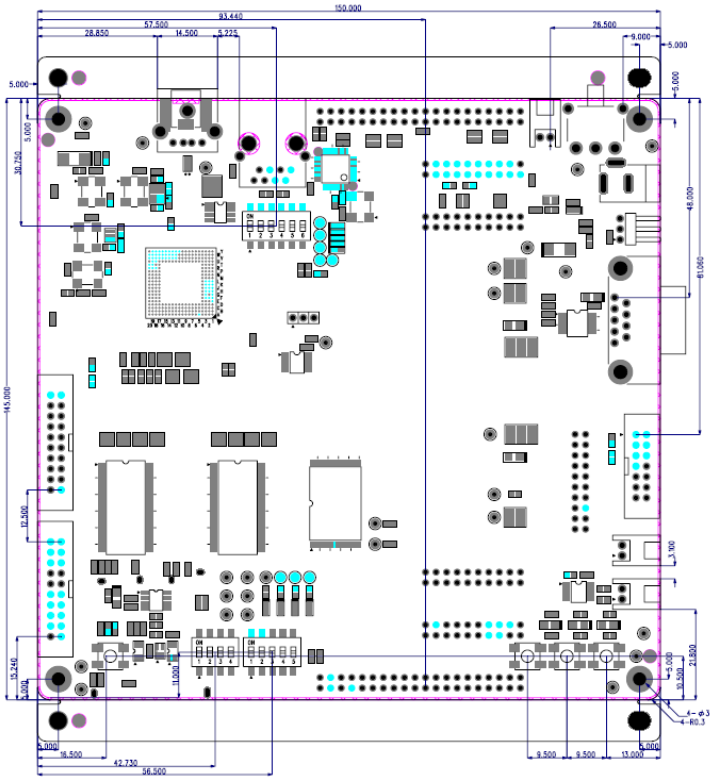
Table 3.2.7 LED Functions on SH7670 CPU Board

No.	Color	Functions
LED1	Yellow	LED for ETHER communication state (Lights on when PHYAD0/LED0 of PHY-LSI outputs "L")
LED2	Yellow	LED for ETHER communication state (Lights on when PHYAD1/LED1 of PHY-LSI outputs "L")
LED3	Yellow	LED for ETHER communication state (Lights on when PHYAD2/LED2 of PHY-LSI outputs "L")
LED4	Yellow	LED for ETHER communication state (Lights on when PHYAD3/LED3 of PHY-LSI outputs "L")
LED5	Yellow	LED for ETHER communication state (Lights on when PHYAD4/LED4 of PHY-LSI outputs "L")
LED6	Blue	LED for power supply (Lights on when 5V power is supplied)
LED7	Yellow	LED for user (Lights on when PC20/WOL outputs "L")
LED8	Yellow	LED for user (Lights on when PE00/ST1_D0/RxD2 outputs "L")
LED9	Yellow	LED for user (Lights on when PE08/ST1_REQ/TxD2 outputs "L")
LED10	Yellow	LED for user (Lights on when PE10/ST1_SYC/CTS2# outputs "L")

3.3 Board Dimensions of SH7670 CPU Board

Figure 3.3.1 shows board dimensions of SH7670 CPU board. Connectors can be mounted on J5-J13 so that the connection to an extension board can be easily enhanced.

<Top view of the component side>



< Top view of component side perspective >

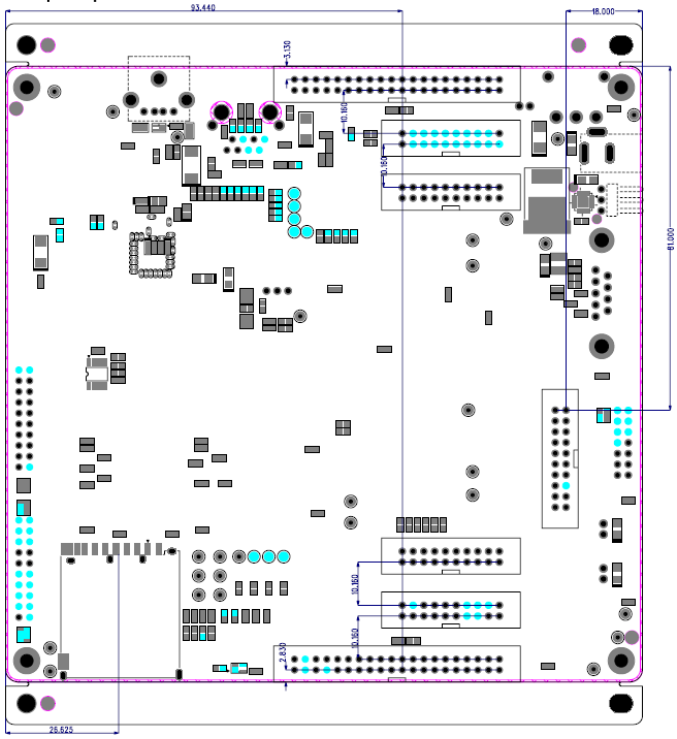


Figure 3.3.1 Board Dimensions of SH7670 CPU board

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Appendix
SCHEMATICS

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SH7670 CPU board M3A-HS71 SCHEMATICS

TITLE	PAGE
INDEX	1
SH7670	2
FLASH/SDRAM	3
Memory Card Slot,USB Ether,EEPROM	4
Other Connectors	5
H-UDI,Reset,Power	6
Switch,Holes	7

Note:

VCC = Digital 5V
3VCC = 3.3V
3VCC_CPU = 3.3V
SDVCC = 3.3V
1.2VCC = 1.2V
3AVCC = Analog 3.3V
UA3V = USB Analog 3.3V
UA1.2V = USB Analog 1.2V

R = Fixed Resistors
RA = Resister Array
VR = Resistor Potentiometers
C = Ceramic Caps
CE = Electrolytic Caps
CP = Decoupling Caps

: not mounted

CHANGE						
Ver.1.00	SCALE		RENESAS SOLUTIONS CORPORATION			M3A-HS71
	DATE	07-12-18	DRAWN	CHECKED	DESIGNED / APPROVED	INDEX (1 / 7)
						DK30686-A

MD_BW	BUS Size
"1"	32bit Bus
"0"	16bit Bus

MD_BW pin is fixed to "L"
CS0# = 16bit

[16.67MHz:CPU] SOP Type

[16.67MHz:CPU]CERALOCK Type

[27MHz:STIF]

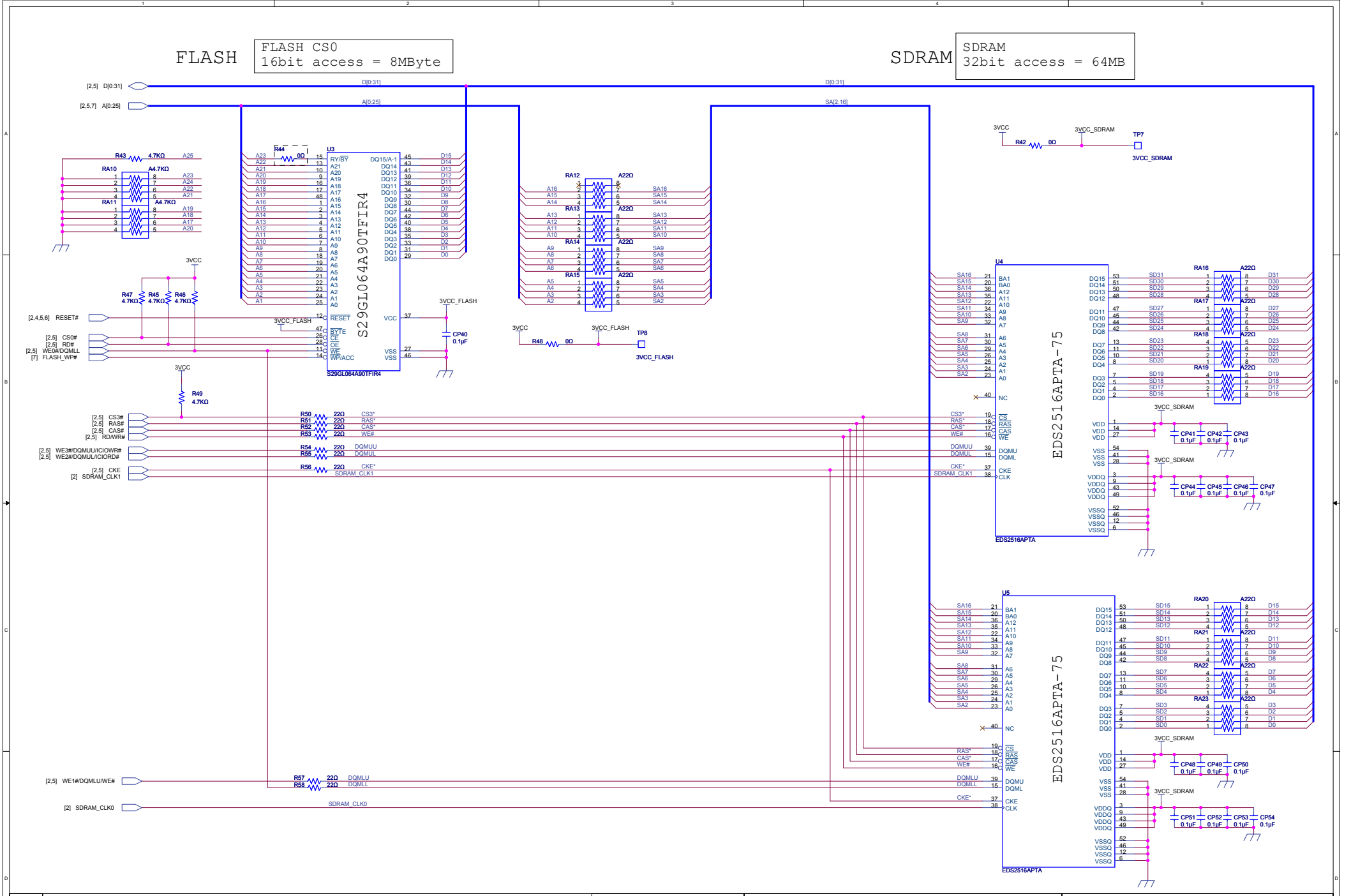
[48MHz:USB] SOP Type

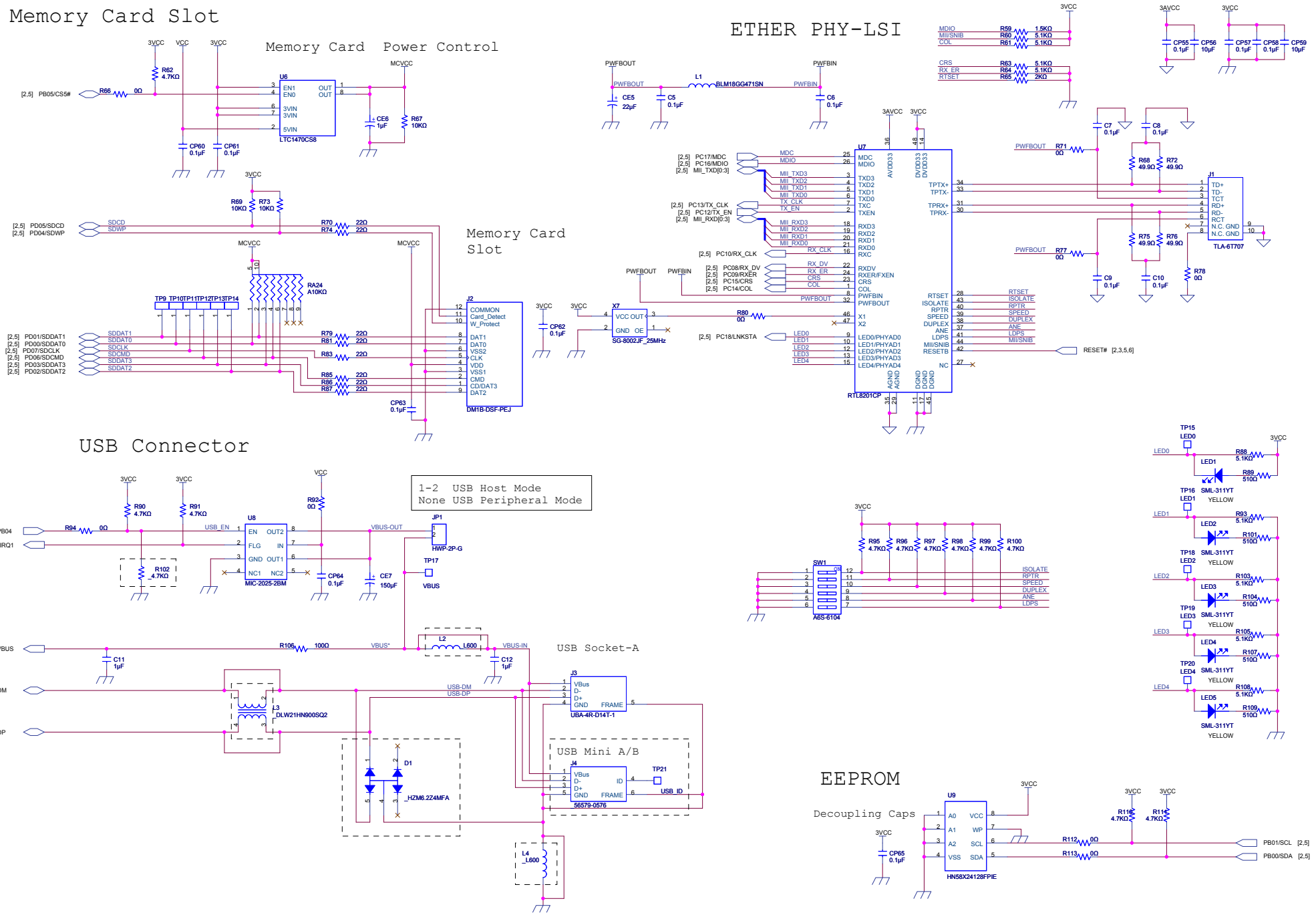
Decoupling Caps

SH7670

SH7671

CHANGE		RENESAS SOLUTIONS CORPORATION				M3A-HS71 SH7670 (2 / 7)
Delete R11,R6,R7,R8,R9,R17 Add JP5,JP6,JP7,R178,CP77,CP78,CP79,CP80,CP81 Add R82,R84		DRAWN	CHECKED	DESIGNED	APPROVED	
Ver.1.00	SCALE					DK30686-A
	DATE 07-12-18					

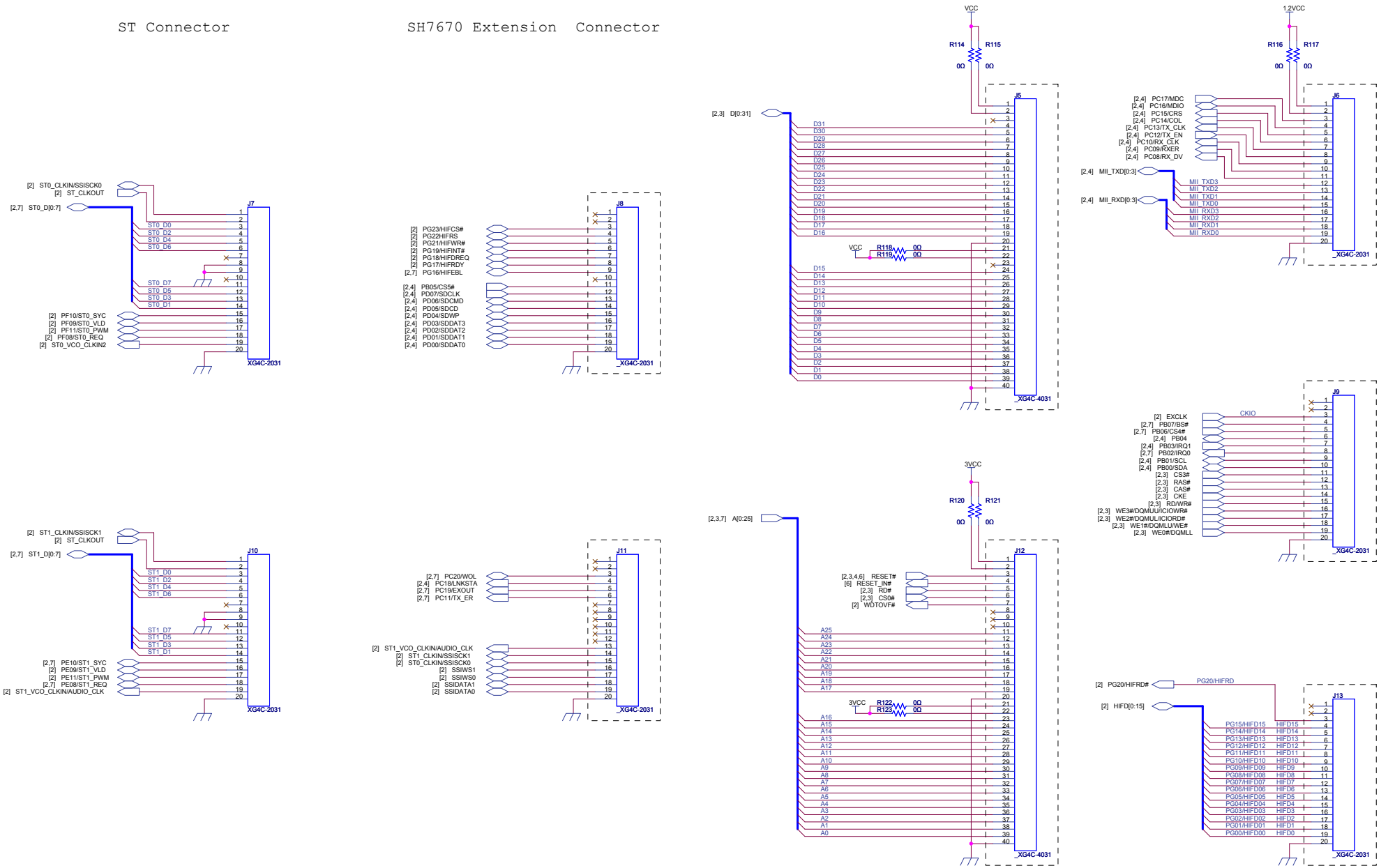

FLASH
FLASH CS0
16bit access = 8MByte
SDRAM
SDRAM
32bit access = 64MB
S29GL064A90TFIR4
EDS2516APTA-75
EDS2516APTA
3VCC
3VCC_FLASH
3VCC_SDRAM
RESET#
CS0#
RD#
WE0#/DQMLL
FLASH_WP#
CS3#
RAS#
CAS#
RD/WR#
WE3#/DQMUU/ICIOWR#
WE2#/DQMUL/ICIORD#
CKE
SDRAM_CLK1
WE1#/DQMLU/WE#
SDRAM_CLK0
D[0:31]
A[0:25]
SA[2:16]
CHANGE
Ver.1.00
SCALE
DATE
07-12-18
RENESAS SOLUTIONS CORPORATION
M3A-HS71
DRAWN
CHECKED
DESIGNED
APPROVED
FLASH/SDRAM
(3 / 7)
DK30686-A



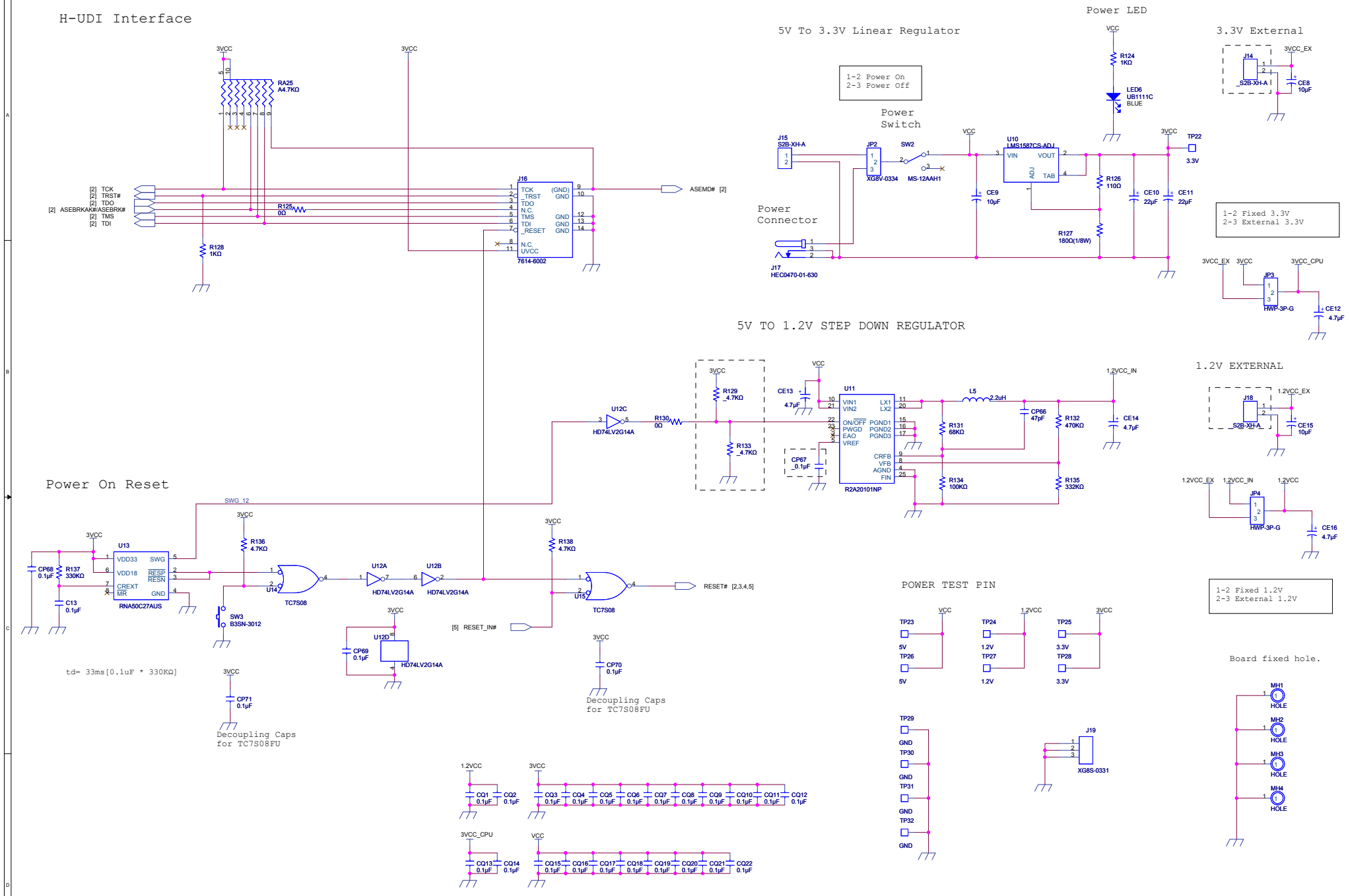
CHANGE	Delete R82,R84		RENESAS SOLUTIONS CORPORATION		M3A-HS71
			DRAWN / CHECKED / DESIGNED / APPROVED		Memory Card Slot USB Ether EEPROM (4 / 7)
	Ver.1.00	SCALE			DK30686-A
		DATE	07-12-18		

ST Connector

SH7670 Extension Connector

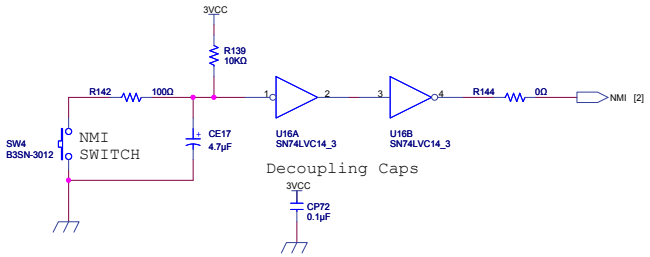


CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS71
			DRAWN / CHECKED / DESIGNED / APPROVED		Connectors2 (5 / 7)
Ver.1.00		SCALE			DK30686-A
		DATE	07-12-18		

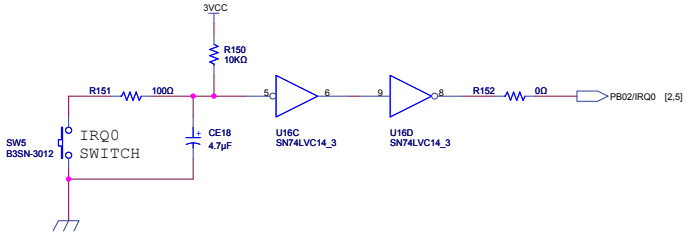


CHANGE	R127 1/10W -> 1/8W (size:1608 -> 2012) R137 33KR -> 330KR Add CQ1 ~ CQ22 Ver.1.00	SCALE		RENESAS SOLUTIONS CORPORATION	M3A-HS71
		DATE	07-12-18	DRAWN / CHECKED / DESIGNED / APPROVED	H-UDI,Power, Reset (6 / 7)
					DK30686-A

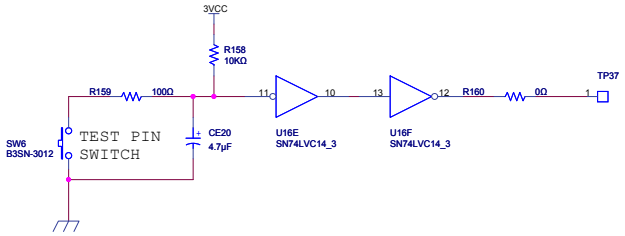
NMI SWITCH CIRCUIT



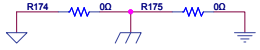
IRQ SWITCH CIRCUIT



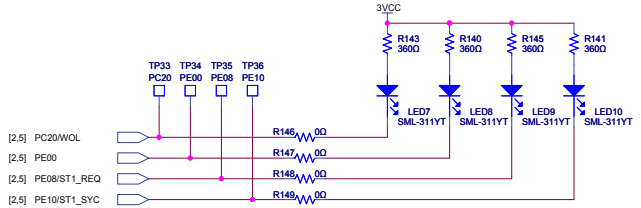
TEST PIN SWITCH CIRCUIT



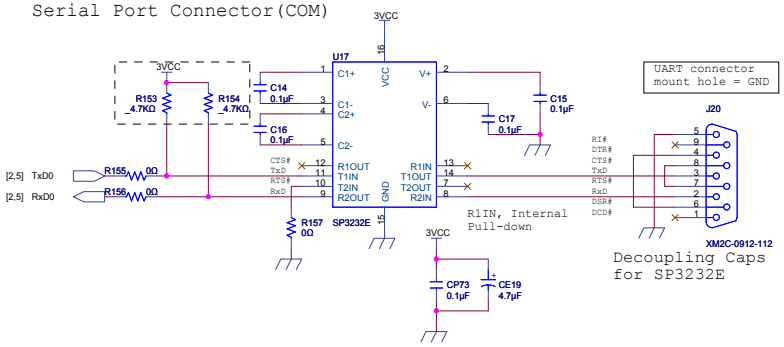
AGND-GND



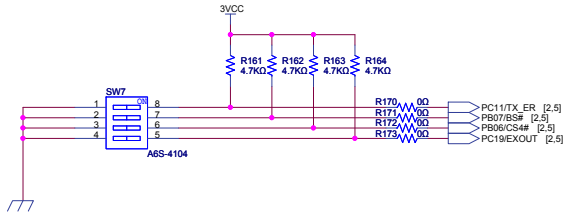
User Port



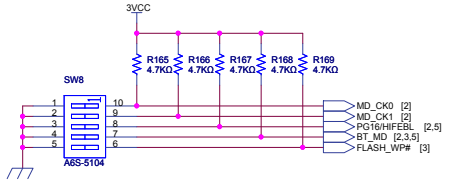
Serial Port Connector(COM)



UserSwitch



Mode Switch



CHANGE	R144, R140, R145, R141 : 330R -> 360R		RENESAS SOLUTIONS CORPORATION		M3A-HS71
			DRAWN / CHECKED / DESIGNED / APPROVED		Switch, Holes (7 / 7)
Ver.1.00		SCALE			DK30686-A
		DATE	07-12-18		

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Revision History	SH7670 CPU Board M3A-HS71User's Manual

Rev.	Date of Issue	Content of Revision	
		Page	Page
1.00	08/01/09	—	First edition issued
1.01	08/05/07	—	Revision history page location was changed. Colophon was changed from ©2007 to ©2008.

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User's Manual
M3A-HS71

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