



## Device Overview

The 89HPES12N3A, a 12 lane 3-port PCI Express® switch, is a member of the IDT PRECISE™ family of PCI Express switching solutions. The PES12N3A is a peripheral chip that performs PCI Express Packet switching with a feature set optimized for high performance applications such as servers and storage. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

The 89HPES12N3A offers an enhanced architecture and feature set in a package that is pin-compatible with the first generation 89HPES12N3 12-lane, 3-port PCIe switch.

## Features

- ◆ **High Performance PCI Express Switch**
  - Twelve 2.5Gbps PCI Express lanes
  - Three switch ports
  - Upstream port configurable up to x4
  - Downstream ports configurable up to x4
  - Low-latency cut-through switch architecture
  - Support for Max Payload Sizes up to 2048 bytes
  - One virtual channel
  - Eight traffic classes
  - PCI Express Base Specification Revision 1.1 compliant

- ◆ **Flexible Architecture with Numerous Configuration Options**
  - Automatic per port link width negotiation to x4, x2 or x1
  - Automatic lane reversal on all ports
  - Automatic polarity inversion on all lanes
  - Ability to load device configuration from serial EEPROM
- ◆ **Legacy Support**
  - PCI compatible INTx emulation
  - Bus locking
- ◆ **Highly Integrated Solution**
  - Requires no external components
  - Incorporates on-chip internal memory for packet buffering and queueing
  - Integrates twelve 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)
- ◆ **Reliability, Availability, and Serviceability (RAS) Features**
  - Supports ECRC and Advanced Error Reporting
  - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  - Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O
  - Compatible with Hot-Plug I/O expanders used on PC and server motherboards

## Block Diagram

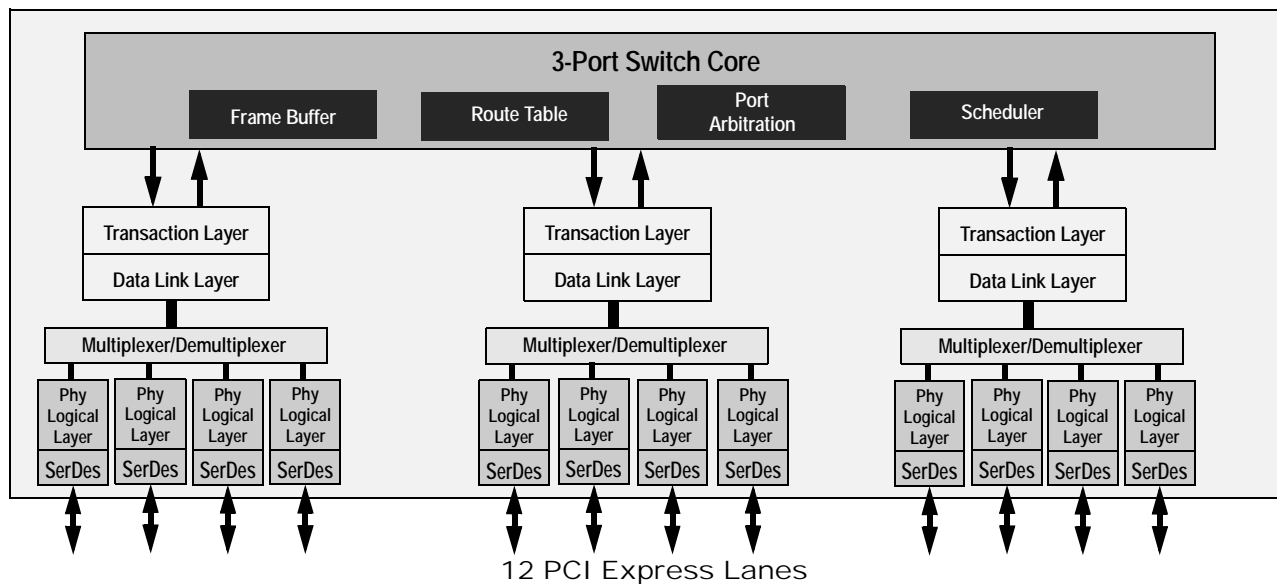


Figure 1 Internal Block Diagram

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- ◆ **Power Management**
  - Utilizes advanced low-power design techniques to achieve low typical power consumption
  - Supports PCI Power Management Interface specification (PCI-PM 1.1)
    - Supports device power management states: D0, D3<sub>hot</sub> and D3<sub>cold</sub>
  - Unused SerDes are disabled
- ◆ **Testability and Debug Features**
  - Ability to read and write any internal register via the SMBus
- ◆ **Eight General Purpose Input/Output Pins**
  - Each pin may be individually configured as an input or output
  - Each pin may be individually configured as an interrupt input
  - Some pins have selectable alternate functions
- ◆ **Packaged in 19x19mm 324-ball BGA with 1mm ball spacing**

## Product Description

Utilizing standard PCI Express interconnect the PES12N3A provides the most efficient high-performance I/O connectivity device for applications requiring high throughput, low latency and simple board layout. It provides 6 GBps (48 Gbps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES12N3A is based on a flexible and efficient layered architecture. The PCI Express layers consist of SerDes, Physical, Data Link and Transaction layers. The PES12N3A can operate either as a store and forward switch or a cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes system selectable algorithms such as round robin, weighted round-robin, and strict priority schemes guaranteeing bandwidth allocation and/or latency for critical traffic classes.

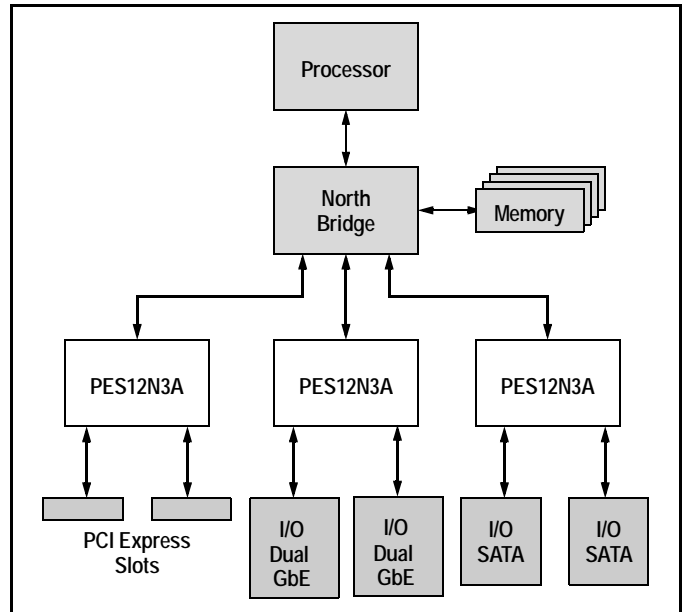


Figure 2 I/O Expansion Application



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
email: [ssdhelp@idt.com](mailto:ssdhelp@idt.com)  
phone: 408-284-8208