Application Note

8-bit SISO, SIPO, PISO, PIPO Shift Registers

AN-CM-303

Abstract

This application note shows how to implement various 8-bit shift registers within the GreenPAK IC. Serial in serial out, Serial in parallel out, Parallel in serial out, and Parallel in parallel out shift registers have been designed in the examples.

The application note comes complete with a design file which can be found in the Reference section.

Contents

Figures

Tables

1 Terms and Definitions

DFF	D-Flipflop
GPIO	General purpose input/output
PIPO	Parallel in parallel out
PISO	Parallel in serial out
SIPO	Serial in parallel out
SISO	Serial in serial out

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK™ Designer software [1] to open the .gp files [1] and view the proposed circuit design. Use the GreenPAK development tools [2] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [3] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure™ Software Hub | Renesas
[2] AN-CM-303, 8-bit SISO, SIPO, PISO, PIPO Shift Registers.gp, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG46533, Datasheet

3 Introduction

Registers are sequential circuits made with flipflops to store and transfer binary information. Shift registers are primarily made with D flipflops in a daisy chain structure. These flipflops can each store one bit of binary information, all of which are controlled by a shared input clock. DFF's can read and store the value of the input signal at every rising edge of the clock. This property of the DFF can be used to build various registers. Different forms of registers like SISO, SIPO, PISO, PIPO are differentiated by the way data is loaded and retrieved.

The implementation shown in this application note consists of 8-bit shift registers which are designed with GreenPAK SLG46533 IC [5]. The number of bits in a shift register corresponds to the number of flipflops present; in this design eight DFFs are used.

4 SISO Shift Register

SISO is one of the most basic forms of the shift registers. The data is loaded serially and retrieved serially. The output of the first DFF is fed into the input of the next DFF at each clock cycle, eventually reaching the last DFF / Output. This Shift register output is delayed from the input. The shift register shifts, or streams, one-bit data per clock cycle.

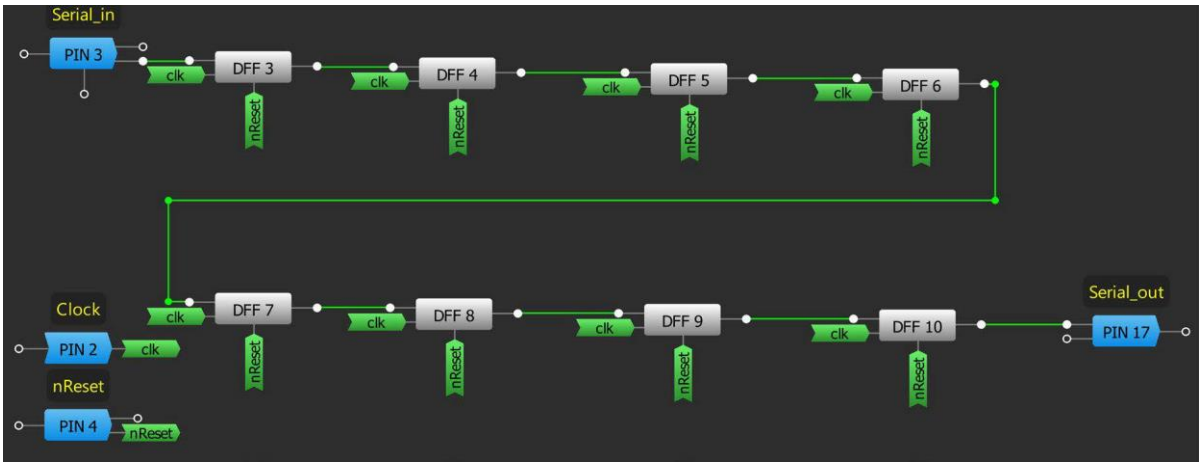


Figure 1: 8-bit Serial In Serial Out Shift Register

As shown in the design above, DFF3 is fed with the input data bits serially and the output is taken from DFF10 serially. All the DFFs share the same clock. nReset is set high to ensure that all DFF's are enabled for normal operation.

The timing diagram shown below has clock and input data stream as first and second waveforms. The rest of the waveforms show how the output of each DFF shifts serially. If we consider the first 8 input bits which are 10011010, we can clearly observe that these 8 bits appear one after another by the 8th rising edge clock at the output of DFF10

One of the main applications of the SISO register is to act as a delay element. The delay can be controlled by the number of stages in the register and the frequency of the clock. In the design below the clock is at 1kHz, so the delay that is observed is 7 ms.

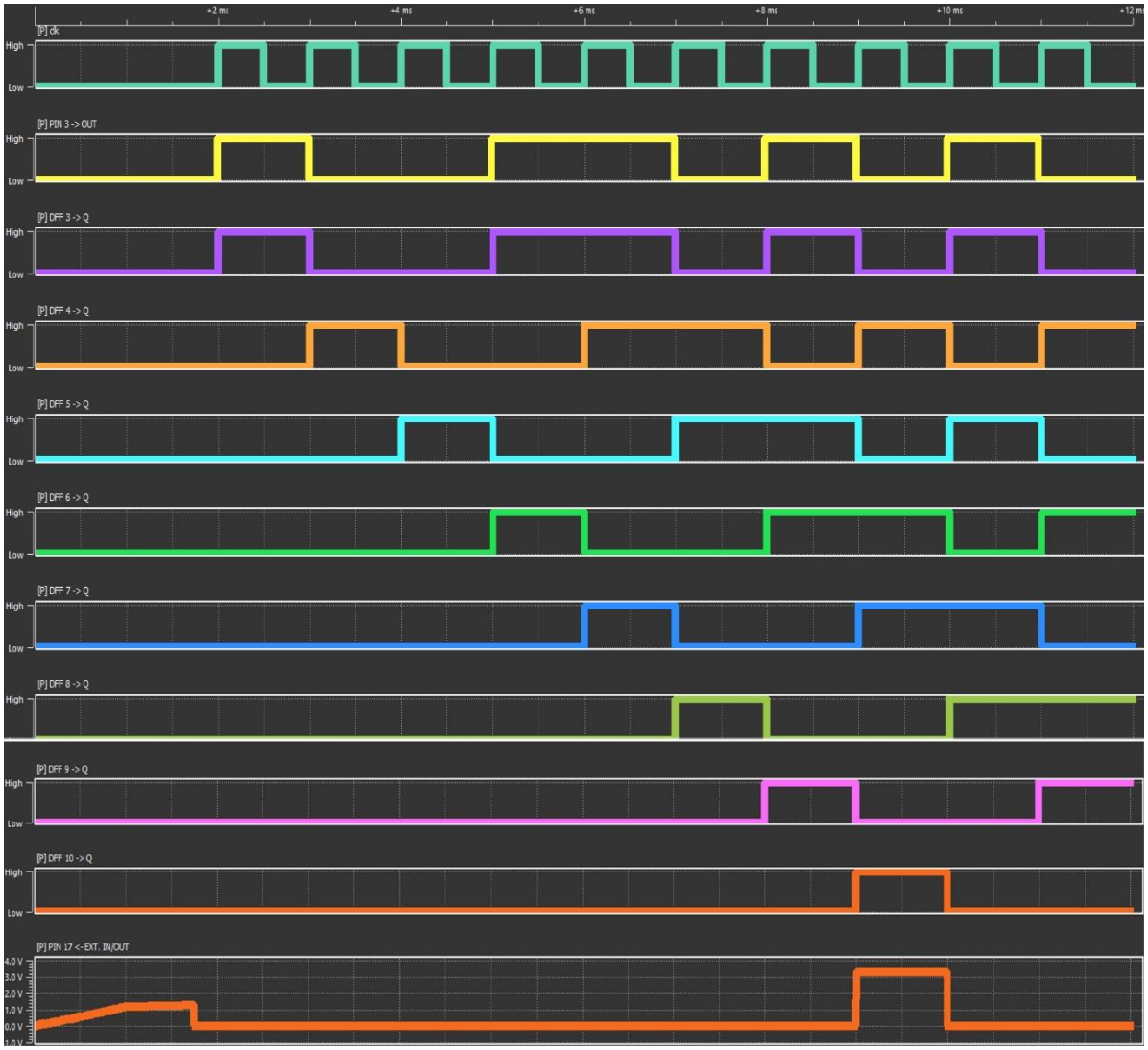


Figure 2: Timing Diagram of 8-bit Serial In Serial Out Shift Register

5 SIPO Shift Register

In this type of shift register, the data is sent serially and retrieved in parallel. All the DFF's are clocked by the same clock and nReset is used to ensure that all the DFF's are enabled for normal operation. The data is fed serially into DFF3. All the parallel outputs are from the outputs of the DFF that are present in the shift register. The output of each intermediate DFF is fed as input to the next DFF. All 8 input serial bits will be available at the parallel outputs after 8 rising edges of the clock.

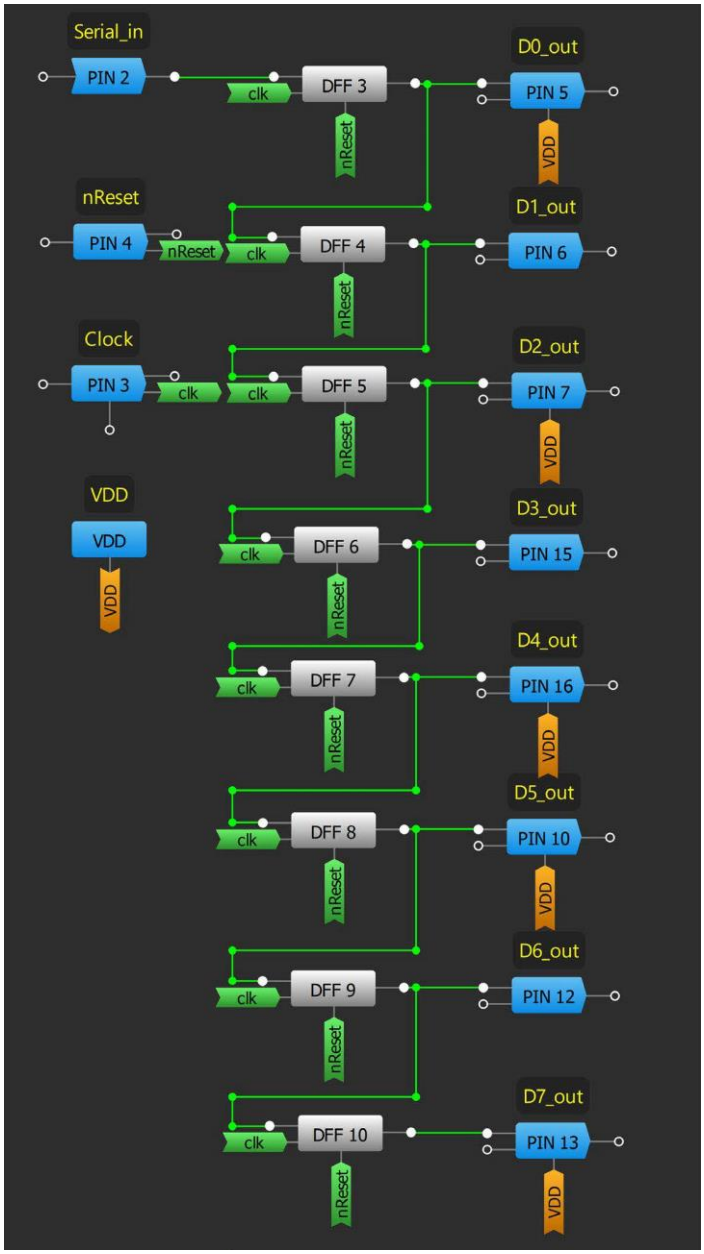
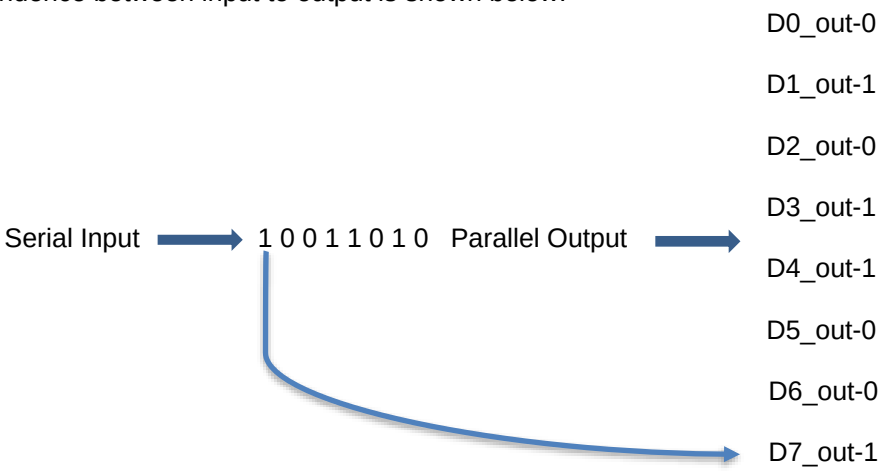


Figure 3: 8-bit Serial In Parallel Out Shift Register

The timing diagram of the SIPO shift register is shown in Fig 4. It has a clock and Serial Data-in as the first two waveforms, and all other waveforms are the outputs of the DFF's. It can be observed that after the 8th rising edge of the clock, the entire input data bits are visible at the output of each DFF.

The first bit which is transmitted serially is observed at the last DFF's output. The main application of the SIPO shift register is data conversion in many digital applications. Sometimes the SIPO shift register is connected to the output of a microprocessor when more GPIO pins are required. In the above design, the clock frequency is 1 kHz and the time taken to convert the 8 serial bits to parallel bits is 8 ms.

The correspondence between input to output is shown below:



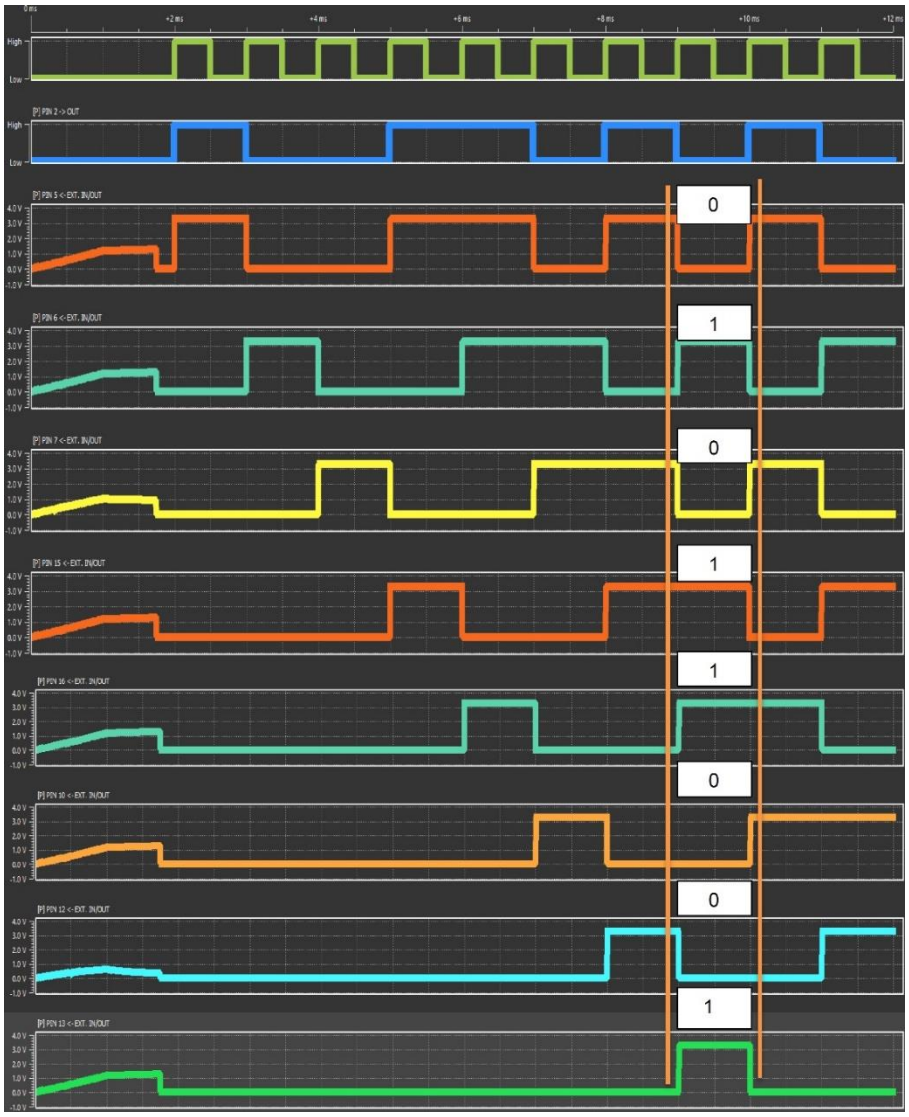


Figure 4: Timing Diagram of 8-bit Serial In Parallel Out Shift Register

6 PISO Shift Register

The PISO shift register is the converse of the SIPO shift register. The inputs are presented simultaneously in parallel, and the output is retrieved serially. The data is taken out one bit per clock cycle. The main point to note in this shift register is that a clock is not required to load the data in the shift register, whereas a clock is required to unload the data.

Similar to the other shift registers, all the DFF's are clocked by the same clock and have the nReset set high for normal operation. 2-bit lookup tables provided in the IC are used as OR gates to provide parallel input to the DFF's as well as transmit the output of one DFF as the input to the next DFF. The output is retrieved serially from the output of DFF10.

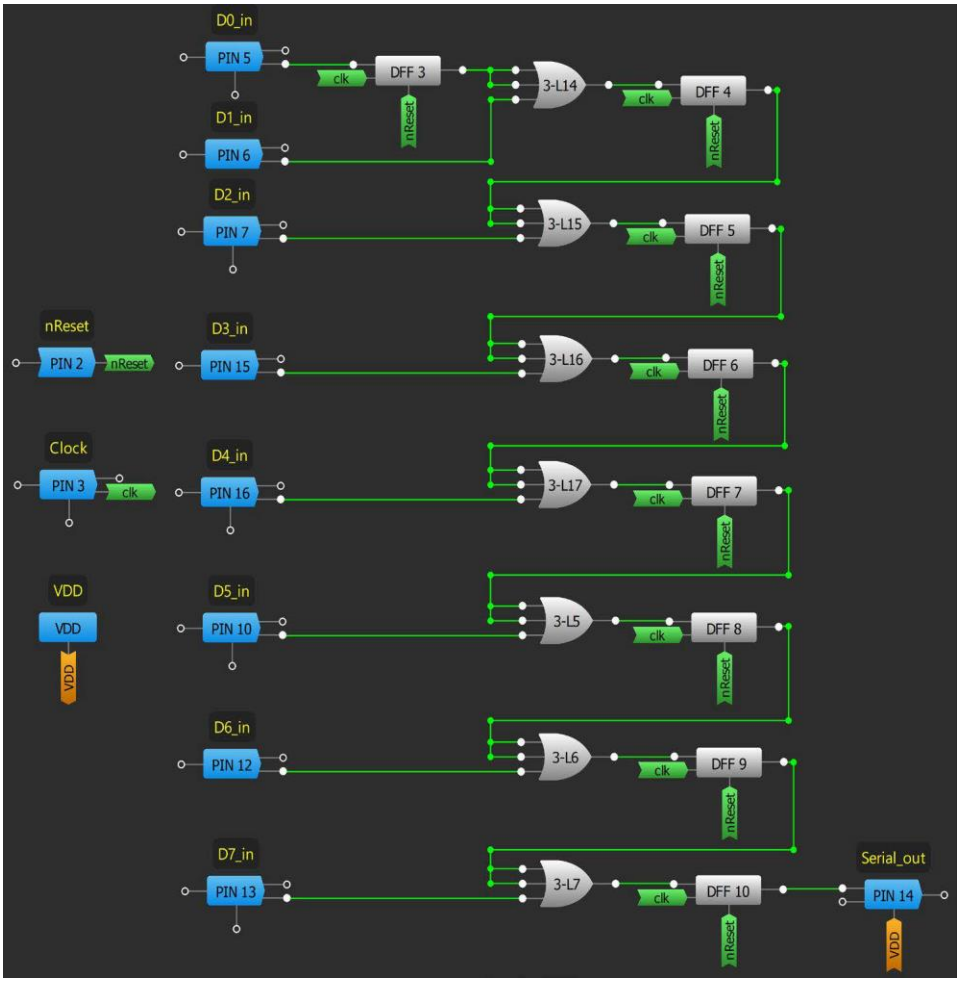
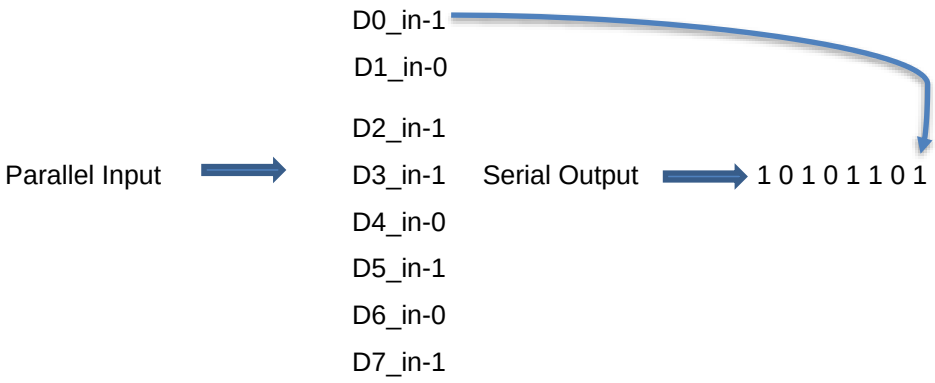


Figure 5: 8-bit Parallel In Serial Out Shift Register

This type of shift register is typically used for data conversion from parallel to serial. All the parallel bits with the data are serially transmitted to the single input of a microprocessor which helps in using fewer input pins of the microprocessor.

The timing diagram shown in Fig. 6 depicts the clock and all parallel inputs, highlighted between two vertical orange lines. The last waveform is the serial data out which shows how all the parallel inputs are converted into a serial bitstream.

The way how inputs correspond to output is shown below.



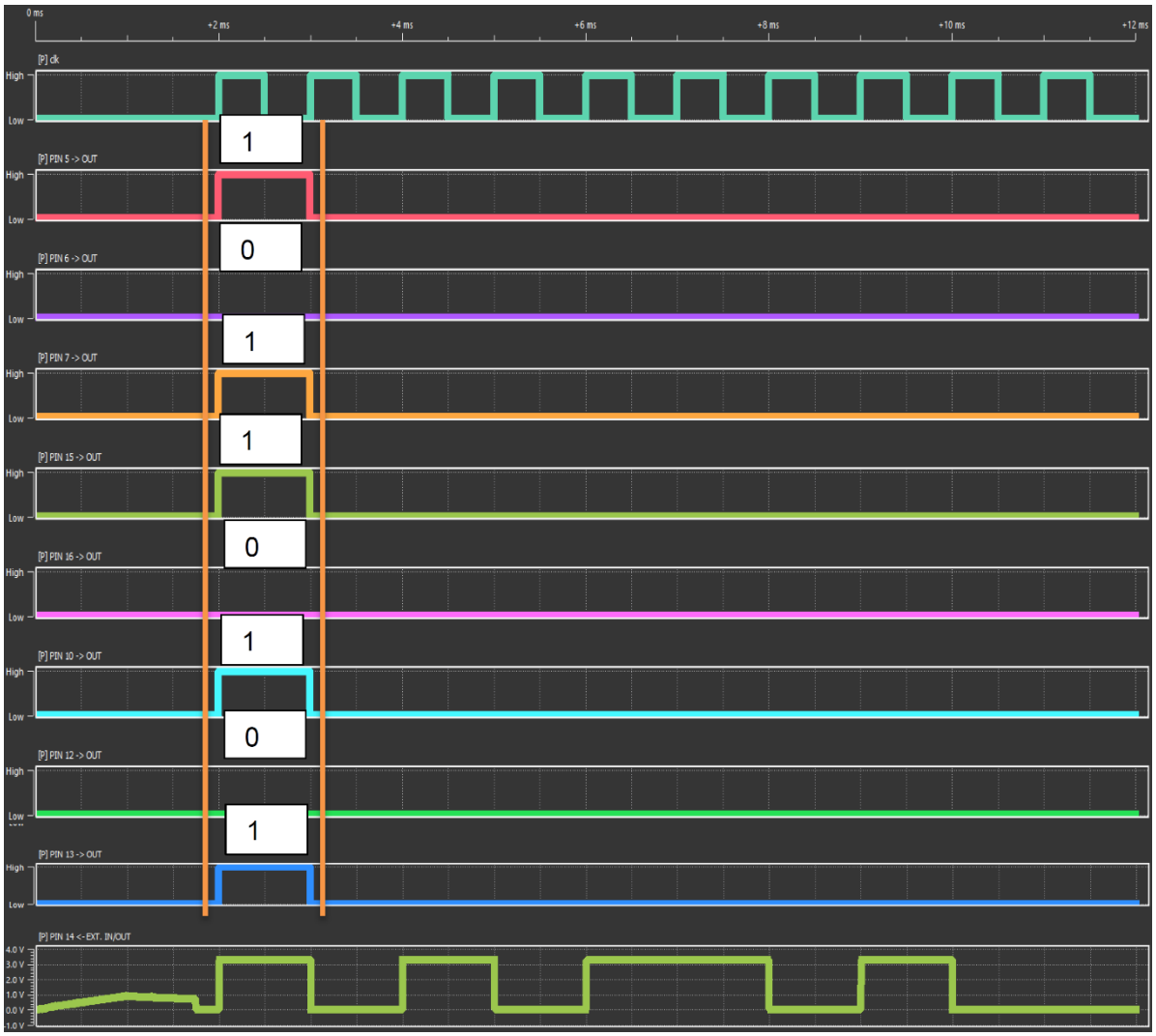


Figure 6: Timing Diagram of 8-bit Parallel In Serial Out Shift Register

7 PIPO Shift Register

This shift register is the converse of the SISO shift register. The input data is given and retrieved in parallel. The output changes with respect to the input within the same clock cycle. Similar to the PISO shift register, a clock is not required to load data into the flipflops, but to latch and transfer out. Hence a PIPO shift register can be used as a temporary storage device, though in practice other GreenPAK capabilities are often included within the design. Whenever new data output is required, a rising edge clock presents the DFF content to the output. One note about this shift register is that there is no connection between individual DFFs. Similar to other shift registers, the same clock and nReset are applied to all the DFF's.

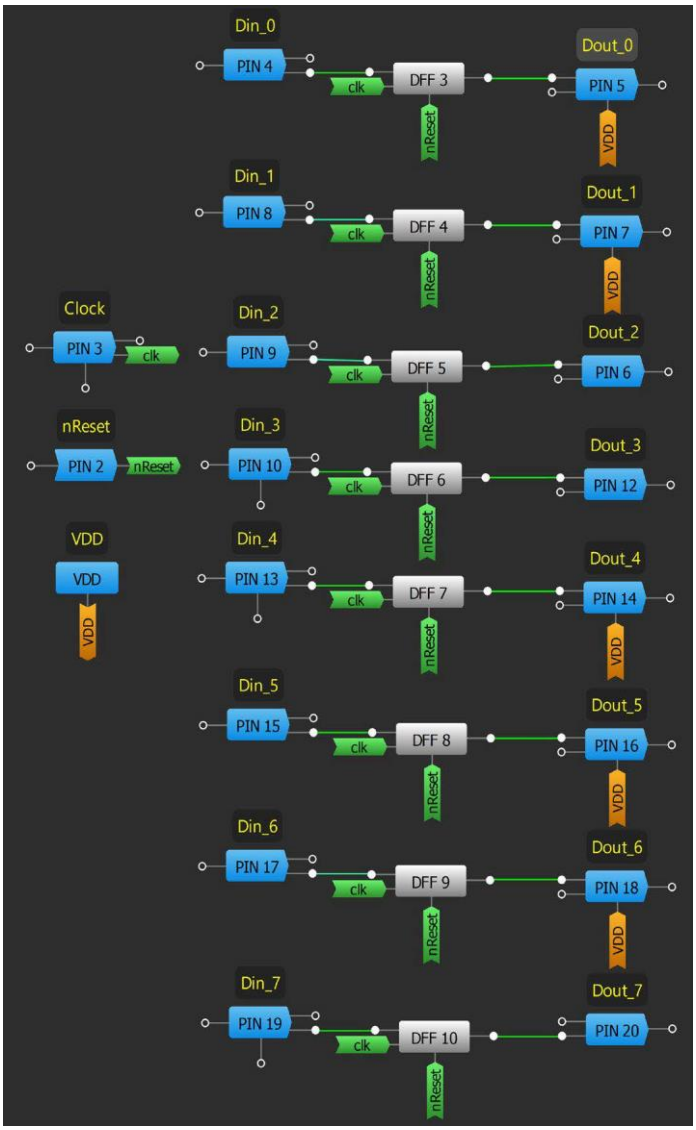


Figure 7: 8-bit Parallel In Parallel Out Shift Register

The timing diagram of the PIPO shift register is shown in Fig. 8. As all the inputs and outputs are loaded and unloaded separately, it results in a large number of waveforms to show. The yellow highlighted line in the waveforms separates the input and the output. All the top waveforms are inputs and the bottom waveforms are outputs. It's clearly visible from the waveforms that the loaded data can be retrieved with a single clock pulse.

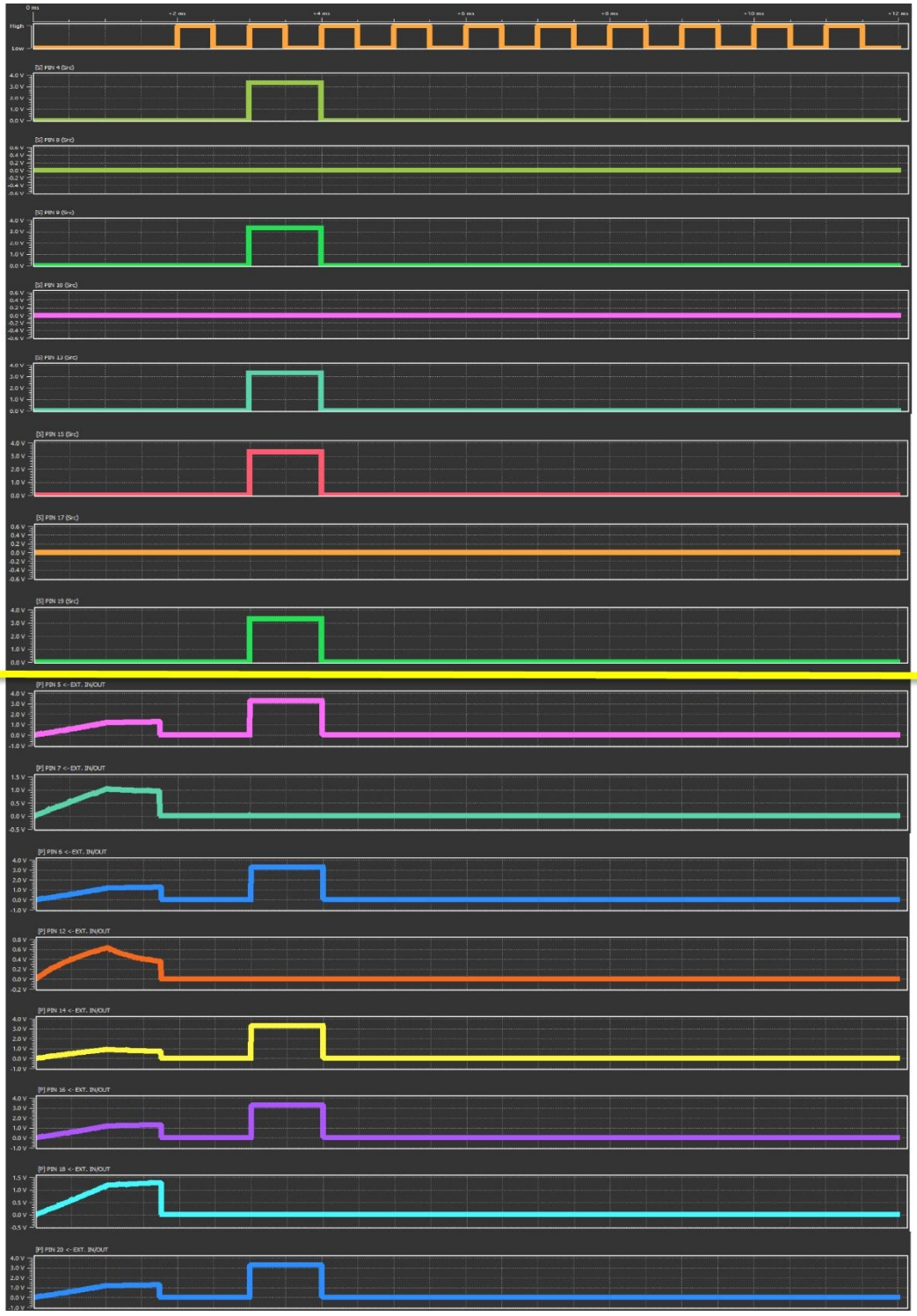


Figure 8: Timing Diagram of 8-bit Parallel In Parallel Out Shift Register

8 GreenPAK Cost Advantage

The GreenPAK SLG46533 IC is a very versatile Programmable Mixed-Signal ASIC. Many applications have been implemented with this IC. Table 1 shows some of the competing IC's that are available in the market for shift register applications.

Table 1: Comparison of Other ICs Available in Market

IC	Quantity	Price	Package/Size
TPIC6C596PWR	1	$ 1.10	TSSOP (16) 5.00 mm × 4.40 mm
MM74HC595MX	1	$ 0.58	TSSOP (16) 5.00 mm x 4.40 mm
SN74HC595	1	$ 0.95	TSSOP (16) 5.00 mm × 4.40 mm

Note 1 All the prices of the ICs are referred from Digi-Key on 08-05-2020.

GreenPAK SLG46533 IC is of size 2.00 mm x 3.00 mm and costs less than $ 0.50. It is clearly visible that the GreenPAK IC is one of the best solutions that are available in the market. Moreover, the user has control over the configuration of the IC in GreenPAK, which increases its value.

9 Conclusions

Shift registers are an integral part of any digital system. In this application note, four types of shift registers, SISO, SIPO, PISO, PIPO have been configured within the GreenPAK SLG46533 IC. The 8-bit shift registers in this application note form a viable alternative to other shift registers available on the market. The GreenPAK SLG46533 IC has the advantage of low PCB area footprint, more circuitry available, and lower cost.

Revision History

Revision	Date	Description
1.0	11-Sep-2020	Initial version.

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