RENESAS

QUAD NON-PROGRAMMABLE PCM CODEC

821004J

FEATURES

- 4 channel CODEC with on-chip digital filters
- Selectable A-law or μ-law companding
- Master clock frequency selection: 2.048 MHz, 4.096 MHz or 8.192 MHz
  - Internal timing automatically adjusted based on MCLK and frame sync signal
- Separate PCM and master clocks
- Single PCM port with up to 8.192 MHz data rate (128 time slots)
- Transhybrid balance impedance hardware adjustable via external components
- Transmit gains hardware adjustable via external components
- Low power +5.0 V CMOS technology
- +5.0 V single power supply
- Package available: 32 pin PLCC

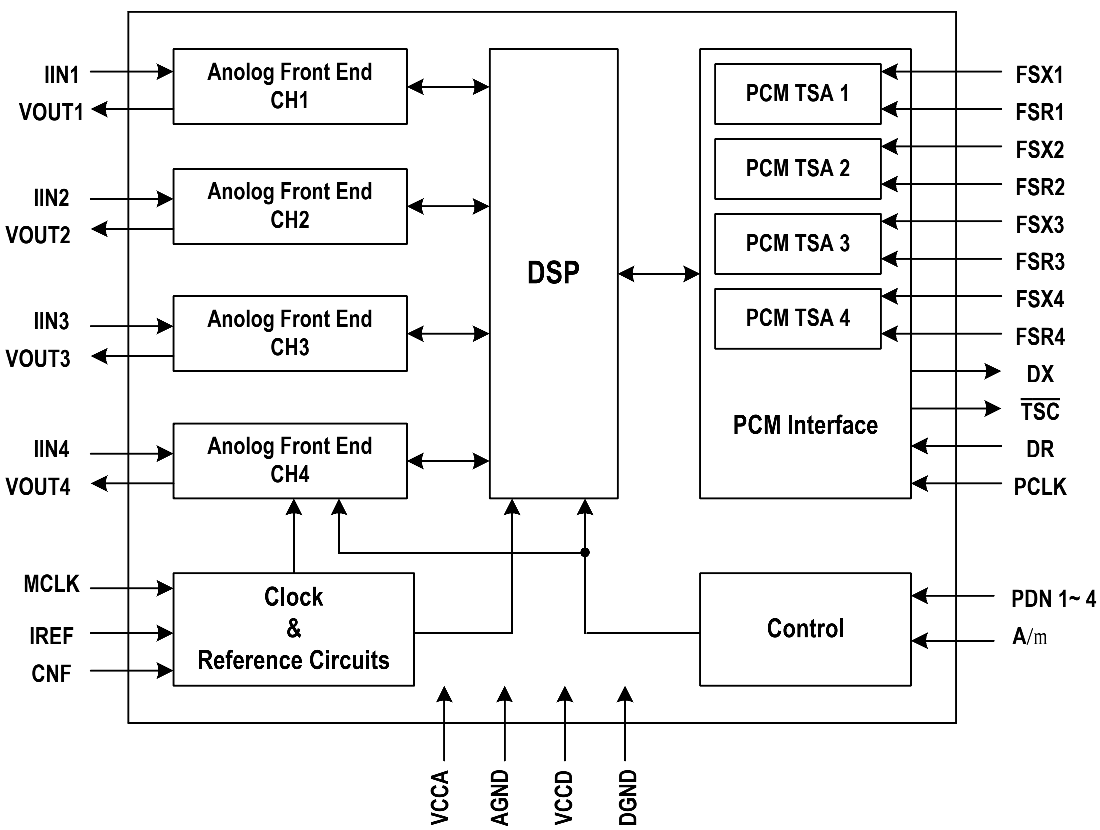
DESCRIPTION

The 821004J is a single-chip, four channel PCM CODEC with on-chip filters. The device provides analog-to-digital and digital-to-analog conversions and supports both a-law and μ–law companding. The digital filters in 821004J provides the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. All of the digital filters are performed in digital signal processors operating from an internal clock, which is derived from MCLK. The fixed filters set the transmit and receive gain and frequency response.

In the 821004J the PCM data is transmitted to and received from the PCM highway in time slots determined by the individual Frame Sync signals (FSR_n and FSX_n, where n = 1-4) at rates from 256 KHz to 8.192 MHz. Both Long and Short Frame Sync modes are available in the 821004J.

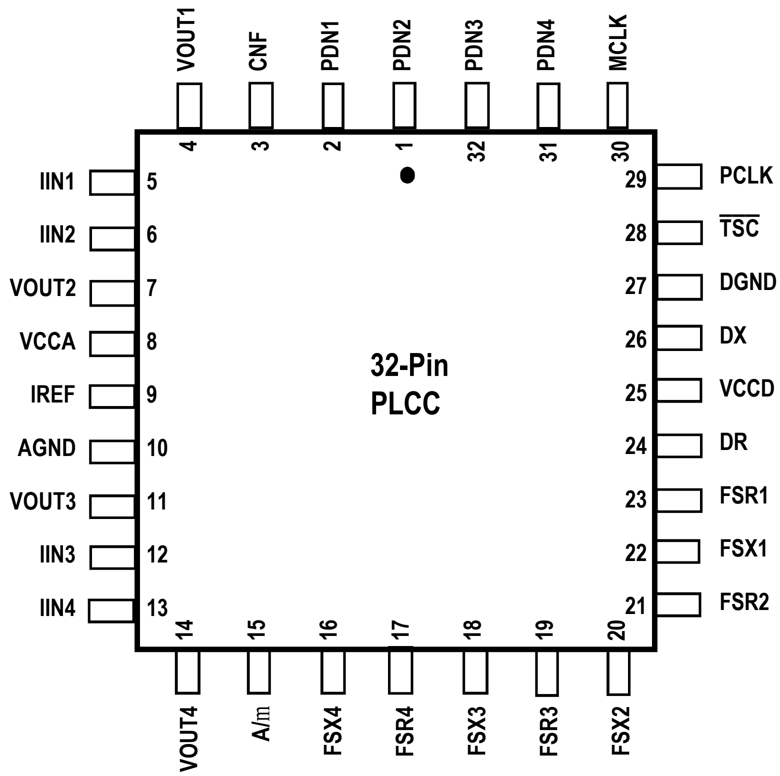
The 821004J can be used in digital telecommunication applications such as PBX, Central Office Switch, Digital Telephone and Integrated Voice/ Data Access Unit.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE **NOVEMBER 2020**

PIN CONFIGURATIONS



PIN DESCRIPTION

Name	I/O	Pin Number	Description
AGND	--	10	**Analog Ground.** All ground pins should be connected to the ground plane of the circuit board.
VCCA	--	8	**+5 V Analog Power Supply.** All power supply pins should be connected to the power plane of the circuit board.
DGND	--	27	**Digital Ground.** All ground pins should be connected to the ground plane of the circuit board.
VCCD	--	25	**+5 V Digital Power Supply.** All power supply pins should be connected to the power plane of the circuit board.
DR	I	24	**Receive PCM Data Input.** The PCM data for Channel 1, 2, 3 and 4 is shifted serially into DR pin by the Receive Frame Sync Signal (FSR) with MSB first. A byte of data for each channel is received every 125 μs at the PCLK rate.
DX	O	26	**Transmit PCM Data Output.** The PCM data for Channel 1, 2, 3 and 4 is shifted serially out to the DX pin by the Transmit Frame Sync Signal (FSX) with MSB first. A byte of data for each channel is transmitted every 125 μs at the PCLK rate. DX is high impedance between time slots.
FSR1 FSR2 FSR3 FSR4	I	23 21 19 17	**Receive Frame Sync Input for Channel 1/2/3/4** This 8kHz signal pulse identifies the receive time slot for Channel N on a system's receive PCM frame. It must be synchronized to PCLK.
FSX1 FSX2 FSX3 FSX4	I	22 20 18 16	**Transmit Frame Sync Input for Channel 1/2/3/4** This 8 kHz signal pulse identifies the transmit time slot for Channel N on a system's transmit PCM frame. It must be synchronized to PCLK.
IREF	O	9	**Reference Current.** The IREF output is biased at the internal reference voltage. A resistor placed from IREF to ground sets the reference current used by the analog-to-digital converter to encode the signal current present on IINn pin (n is channel number, n = 1 to 4) into digital form.
VOUT1 VOUT2 VOUT3 VOUT4	O	4 7 11 14	**Voice Frequency Receiver Output for Channel 1/2/3/4** This is the output of receiver amplifier for Channel N. The received digital data from DR is processed and converted to an analog signal at this pin.
IIN1 IIN2 IIN3 IIN4	I	5 6 12 13	**Voice Frequency Transmitter Input for Channel 1/2/3/4** This is the input to the gain setting amplifier in the transmit path for Channel N. The analog voice band voltage signal is applied to this pin through a resistor. This input is a virtual AC ground input, which is biased at the IREF pin.
MCLK	I	30	**Master Clock.** The Master Clock provides the clock for the DSP. It can be either 2.048 MHz or 4.096 MHz. The 821004J determines the MCLK frequency via the FSX inputs and makes the necessary internal adjustments automatically. The MCLK frequency must be an integer multiple of the FSX frequency.
PCLK	I	29	**PCM Clock.** The PCM Clock shifts out the PCM data to the DX pin and shifts in PCM data from the DR pin. The PCM clock frequency is an integer multiple of the frame sync frequency. When PCLK is connected to MCLK, the PCM clock can generate the DSP clock as well.
$\overline{\text{TSC}}$	O	28	**Time Slot Control.** This open drain output is low active. When the PCM data is transmitted to the DX pin for any of the four channels, this pin will be pulled low.
A/μ	I	15	**A/μ-Law Selection.** When this pin is low, μ-Law is selected; when this pin is high, A-Law is selected. This pin can be connected to VCCD or DGND pin directly.

PIN DESCRIPTION (cont'd)

Name	I/O	Pin Number	Description
PDN1 PDN2 PDN3 PDN4	I	2 1 32 31	**Channel 1/2/3/4 Power Down.** When this pin is high, Channel N is powered down.
CNF	O	3	**Capacitor For Noise Filter.** This pin should be connected to AGND through a 0.1µF capacitor.
NC	--		No connection

FUNCTIONAL DESCRIPTION

The 821004J contains four channel PCM CODEC with on chip digital filters. It provides the four-wire solution for the subscriber line circuitry in digital switches. The device converts analog voice signal to digital PCM data, and converts digital PCM data back to analog signal. Digital filters are used to bandlimit the voice signals during the conversion. Either A-law or μ-law is supported by the 821004J. The law selection is performed by A/μ pin.

The frequency of the master clock (MCLK) can be 2.048 MHz, 4.096 MHz, or 8.192 MHz. Internal circuitry determines the master clock frequency automatically.

The serial PCM data for four channels are time multiplexed via two pins, DX and DR. The time slots of the four channels are determined by the individual Frame Sync signals at rates from 256 kHz to 8.192 MHz. For each channel, the 821004J provides a transmit Frame Sync signal and a receive Frame Sync signal.

Each channel of the 821004J can be powered down independently to save power consumption. The Channel Power Down Pins PDN1-4 configure channels to be active (power-on) or standby (power-down) separately.

Signal Processing

High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) are used in the 821004J to provide the required conversion accuracy. The associated decimation and interpolation filtering are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering and sample rate conversion.

Transmit Signal Processing

In the transmit path, the analog input signal is received by the ADC and converted into digital data. The digital output of the oversampling ADC is decimated and sent to the DSP. The transmit filter is implemented in the DSP as a digital bandpass filter. The filtered signal is further decimated and compressed to PCM format.

Transmit PCM Interface

The transmit PCM interface clocks out 1 byte (8 bits) PCM data out of DX pin every 125 μs. The transmit logic, synchronized by the Transmit Frame Sync signal (FSXn), controls the data transmission. The FSXn pulse identifies the transmit time slot of the PCM frame for Channel N. The PCM Data is transmitted serially on DX pin with the Most Significant Bit (MSB) first. When the PCM data is being output on DX pin, the $\overline{\text{TSC}}$ signal will be pulled low.

Receive Signal Processing

In the receive path, the PCM code is received at the rate of 8,000 samples per second. The PCM code is expanded and sent to the DSP for interpolation. A receive filter is implemented in the DSP as a digital lowpass filter. The filtered signal is then sent to an oversampling DAC. The DAC output is post-filtered and delivered at VOUT pin by an amplifier. The amplifier can drive resistive load higher than 2 KΩ.

Receive PCM Interface

The receive PCM interface clocks 1 byte (8 bits) PCM data into DR pin every 125 μs. The receive logic, synchronized by the Receive Frame Sync signal (FSRn), controls the data receiving process. The FSRn pulse identifies the receive time slot of the PCM frame for Channel N. The PCM Data is received serially on DR pin with the Most Significant Bit (MSB) first.

Hardware Gain Setting In Transmit Path

The transmit gain of the 821004J for each channel can be set by 2 resistors, R_{REF} and R_{TXn} (as shown in Figure 1), according to the following equation:

$$G_t = \frac{3 \times R_{REF}}{R_{TXn}}$$

The receive gain of 821004J is fixed and equal to 1.

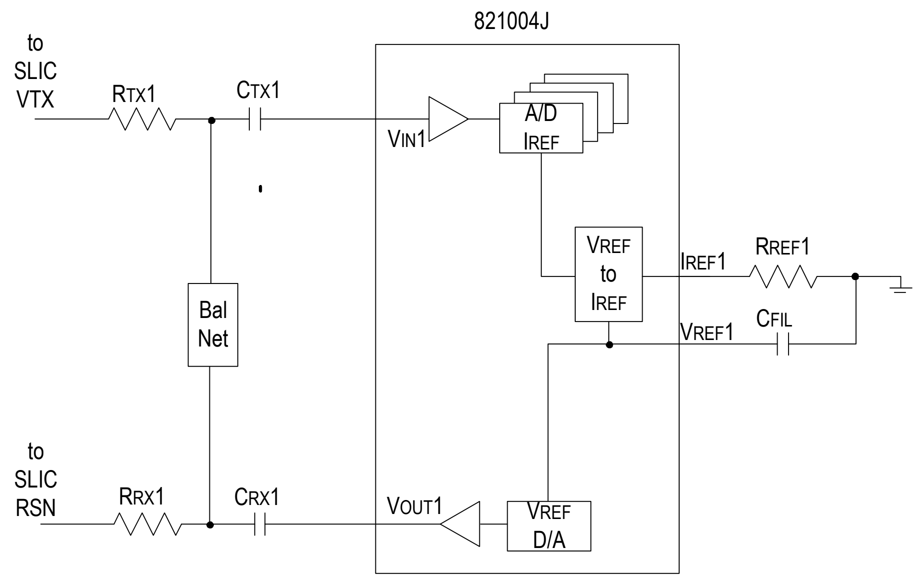


Figure 1. 821004J Transmit Gain Setting for Channel 1

OPERATING THE 821004J

The following descriptions about operation applies to all four channels of the 821004J.

Power-on Sequence and Master Clock Configuration

To power on the 821004J users should follow this sequence:

1. Apply ground;
2. Apply VCC, finish signal connections;
3. Set PDN1-4 pins high, thus all of the 4 channels are powered down;

The master clock (MCLK) frequency of 821004J can be configured as 2.048 MHz, 4.096 MHz or 8.192 MHz. Using the Transmit Frame Sync (FSX) inputs, the device determines the MCLK frequency and makes the necessary internal adjustments automatically. The MCLK frequency must be an integer multiple of the Frame Sync frequency.

Operating Modes

There are two operating modes for each transmit or receive channel: standby mode (when the channel is powered down) and normal mode (when the channel is powered on). The mode selection of each channel is done by its corresponding PDN pin. When PDNn is 1, Channel N is in standby mode; when PDNn is 0, Channel N is in normal mode.

In standby mode, all circuits are powered down with the analog outputs placed in high impedance state.

In normal mode, each channel of the 821004J is able to transmit and receive both PCM and analog information. The normal mode is used when a telephone call is in progress.

Companding Law Selection

An A/μ pin is provided by 821004J for the companding law selection. When this pin is low, μ-law is selected; when the pin is high, A-law is selected.

ABSOLUTE MAXIMUM RATINGS

Rating	Com'l & Ind'l	Unit
Power Supply Voltage	≤ 6.5	V
Voltage on Any Pin with Respect to Ground	-0.5 to 5.5	V
Package Power Dissipation	≤ 600	mW
Storage Temperature	-65 to +150	°C

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	4.75		5.25	V

NOTE: MCLK: 2.048 MHz, 4.096 MHz or 8.192 MHz with tolerance of ± 50 ppm

ELECTRICAL CHARACTERISTICS

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.4	V	DX, $\overline{TSC}$, I_L = 14mA
				0.8	V	All other digital outputs, I_L = 4mA.
				0.2	V	All digital pins, I_L = 14mA
V_{OH}	Output High Voltage	VDD-0.6			V	DX, I_H = -7 mA, all other outputs, I_H = -4 mA
		VDD-0.2			V	All digital pins, I_H = -1mA
I_I	Input Current	-10		10	µA	Any digital inputs GND<V_{IN}<V_{DD}
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Note: Total current must not exceed absolute maximum ratings.

Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Test Conditions
PD2	Operating Power Dissipation 1		180	240	mW	All channels are active
PD1	Operating Power Dissipation 1		60	90	mW	Only one channel is active
PD0	Standby Power Dissipation		4	10	mW	All channels are powered down,with only MCLK present

Note: Power measurements are made at MCLK = 4.096 MHz, outputs unloaded

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{OUT1}	Output Voltage	2.25	2.4	2.6	V	Alternating±zero µ-law PCM code applied to DR.
V_{OUT2}	Output Voltage Swing	3.25			V P-P	R_L=2000Ω
R_O	Output Resistance		1	4	Ω	0dBm0, 1020Hz PCM code applied to DR
R_L	Load Resistance	2000			Ω	External loading
I_{IR}	Analog Input Current Range		±40		µA	R_{REF} = 13kΩ
I_{IOS}	Offset Current Allowed on IIN	-1.6		+1.6	µA	
I_{OUT}	VOUT Output Current (F< 3400Hz)	-5		5	mA	
I_Z	Output Leakage Current	-10		10	µA	Power down
C_L	Load Capacitance			100	pF	External loading

TRANSMISSION CHARACTERISTICS

0dBm0 is defined as 0.6832Vrms for A-law and 0.6778 Vrms for µ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected. Typical value are tested at V_{DD} = 5V and T_A = 25°C.

Absolute Gain

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XA}	Transmit Gain, Absolute					Signal input of 0 dBm0, µ-law or A-law
	0°C to 85°C	-0.30		0.30	dB	
	-40°C	-0.40		0.40	dB	
G_{RA}	Receive Gain, Absolute					Measured relative to 0 dBm0, µ-law or A-law, PCM input of 0 dBm0 1020 Hz, R_L = 10 kΩ
	0°C to 85°C	-0.30		0.30	dB	
	-40°C	-0.40		0.40	dB	

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain Tracking					Tested by sinusoidal method, A-law or µ-law
	+3 dBm0 to -37 dBm0 (exclude -37 dBm0)	-0.25		0.25	dB	
	-37 dBm0 to -50 dBm0 (exclude -50 dBm0)	-0.50		0.50	dB	
	-50 dBm0 to -55 dBm0	-1.40		1.40	dB	
GT_R	Receive Gain Tracking					Tested by sinusoidal method, A-law or µ-law
	+3 dBm0 to -40 dBm0 (exclude -40 dBm0)	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0 (exclude -50 dBm0)	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XR}	Transmit Gain, Relative to G_{XA}					
	f = 50 Hz			-30	dB	
	f = 60 Hz			-30	dB	
	f = 300 Hz to 3000 Hz	-0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	-0.4		0.15	dB	
	f = 3600 Hz			-0.1	dB	
	f ≥ 4600 Hz			-35	dB	
G_{RR}	Receive Gain, Relative to G_{RA}					
	f < 300 Hz			0	dB	
	f = 300 Hz to 3000 Hz	-0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	-0.4		0.15	dB	
	f = 3600 Hz			-0.2	dB	
	f ≥ 4600 Hz			-35	dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
D_{XA}	Transmit Delay, Absolute *			340	µs	
D_{XR}	Transmit Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			280	µs	
	f = 600 Hz –1000 Hz			150	µs	
	f = 1000 Hz – 2600 Hz			80	µs	
	f = 2600 Hz – 2800 Hz			280	µs	
D_{RA}	Receive Delay, Absolute *			260	µs	
D_{RR}	Receive Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			50	µs	
	f = 600 Hz –1000 Hz			80	µs	
	f = 1000 Hz – 2600 Hz			120	µs	
	f = 2600 Hz – 2800 Hz			150	µs	

Note*: Minimum value in transmit and receive path.

Distortion

Parameter	Description	Min	Typ	Max	Units	Test Conditions
STDX	Transmit Signal to Total Distortion Ratio A-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0 µ-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0	 36 36 30 24 36 36 31 27			 dB dB dB dB dB dB dB dB	ITU-T O.132 Sine Wave Method,Psophometric Weighted for A-law, C Message Weighted for µ-law.
STDR	Receive Signal to Total Distortion Ratio A-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0 µ-law : Input level = 0 dBm0 Input level = -30 dBm0 Input level = -40 dBm0 Input level = -45 dBm0	 36 36 30 24 36 36 31 27			 dB dB dB dB dB dB dB dB	ITU-T O.132 Sine Wave Method,Psophometric Weighted for A-law;Sine Wave Method,C Message Weighted for µ-law;
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation Distortion			-42	dBm0	Transmit or receive,two frequencies in the range (300 Hz– 3400 Hz) at –6 dBm0

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise, C Message Weighted for µ-law			16	dBrnC0	
NXP	Transmit Noise, Psophometric Weighted for A-law			-68	dBm0p	
NRC	Receive Noise, C Message Weighted for µ-law			12	dBrnC0	
NRP	Receive Noise, Psophometric Weighted for A-law			-78	dBm0p	
NRS	Noise, Single Frequency f = 0 kHz – 100 kHz			-53	dBm0	IIN = 0 A, tested at VOUT
PSRX	Power Supply Rejection Transmit f = 300 Hz – 3.4 kHz f = 3.4 kHz – 20 kHz	 40 25			 dB dB	VDD = 5.0 VDC + 100 mVrms
PSRR	Power Supply Rejection Receive f = 300 Hz – 3.4 kHz f = 3.4 kHz – 20 kHz	 40 25			 dB dB	PCM code is positive one LSB, VDD = 5.0 VDC + 100 mVrms
SOS	Spurious Out-of-Band Signals at VOUT Relative to Input PCM code applied: 4600 Hz – 20 kHz 20 kHz – 50 kHz			 -40 -30	 dB dB	0 dBm0, 300 Hz – 3400 Hz input

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into IIN of interfering channel. Idle PCM code into channel under test.
XT_{R-X}	Receive to Transmit Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. IIN = 0 A for channel under test.
XT_{X-X}	Transmit to Transmit Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into IIN of interfering channel. IIN = 0 A for channel under test.
XT_{R-R}	Receive to Receive Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 signal into IIN. Idle PCM code into DR.
XT_{R-X}	Receive to Transmit Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into DR. IIN = 0 A.

TIMING CHARACTERISTICS

Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t1	PCLK Duty Cycle	40		60	%	PCLK=512kHz to 8.192MHz
t2	PCLK Rise and Fall Time			25	ns	PCLK=512kHz to 8.192MHz
t3	MCLK Duty Cycle	40		60	%	MCLK=2.048Hz,4.096MHz or 8.192MHz
t4	MCLK Rise and Fall Time			15	ns	MCLK=2.048Hz,4.096MHz or 8.192MHz
t5	PCLK Clock Period	244			ns	PCLK=512kHz to 8.192MHz

Transmit

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t11	Data Output Delay Time (for Short Frame Sync Mode)	5		70	ns	
t12	Data Hold Time	5		70	ns	
t13	Data Delay to High-Z	50		220 t5+70	ns	
t14	Frame sync Hold Time	50			ns	
t15	Frame sync High Setup Time	55		t5-50	ns	
t16	$\overline{\text{TSC}}$ Enable Delay Time(for Short Frame Sync Mode)	5		80	ns	
t17	$\overline{\text{TSC}}$ Disable Delay Time	50		220 t5+70	ns	
t18	Data Output Delay Time(for Long Frame Sync Mode)	5		40	ns	
t19	$\overline{\text{TSC}}$ Enable Delay Time(for Long Frame Sync Mode)	5		40	ns	
t21	Receive Data Setup Time	25			ns	
t22	Receive Data Hold Time	5			ns	

Note: Timing parameter t13 is referenced to a high-impedance state.

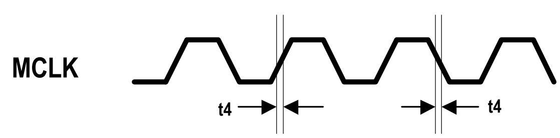


Figure 2. MCLK Timing

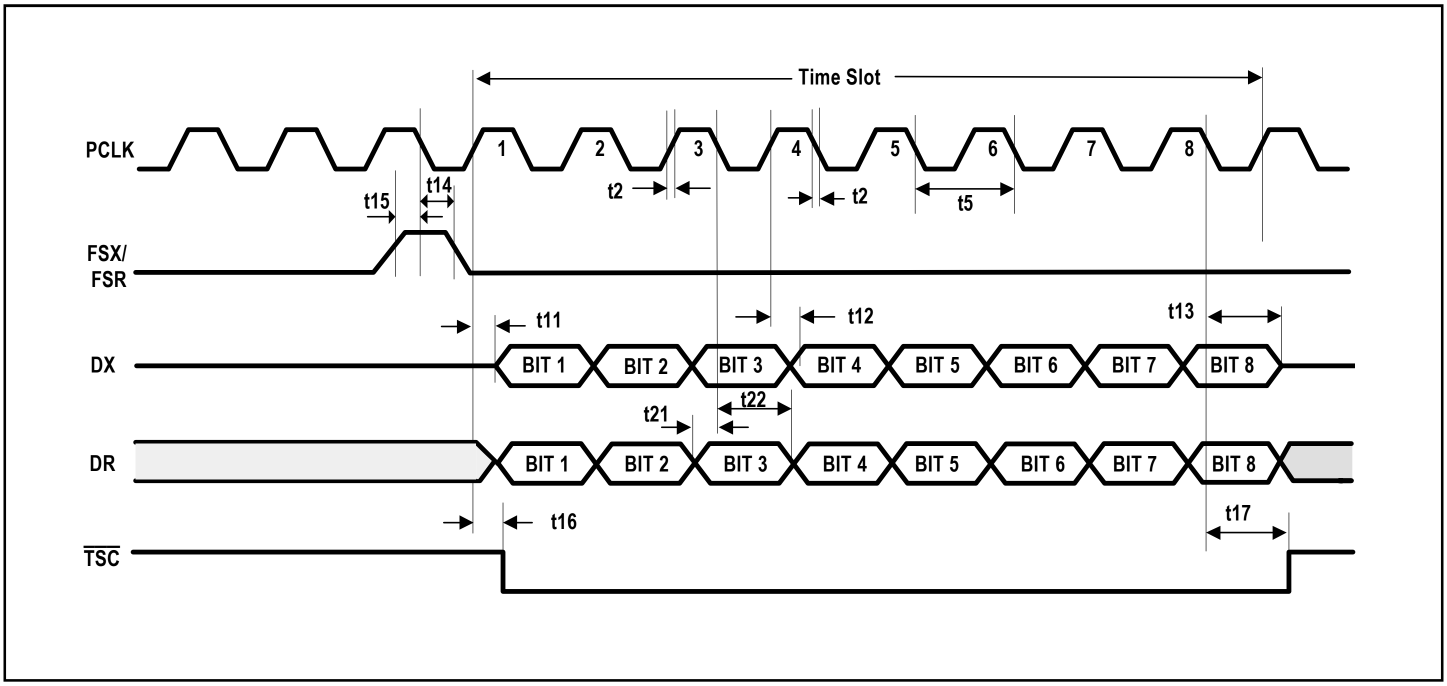


Figure 3. PCM Interface Timing for Short Frame Mode

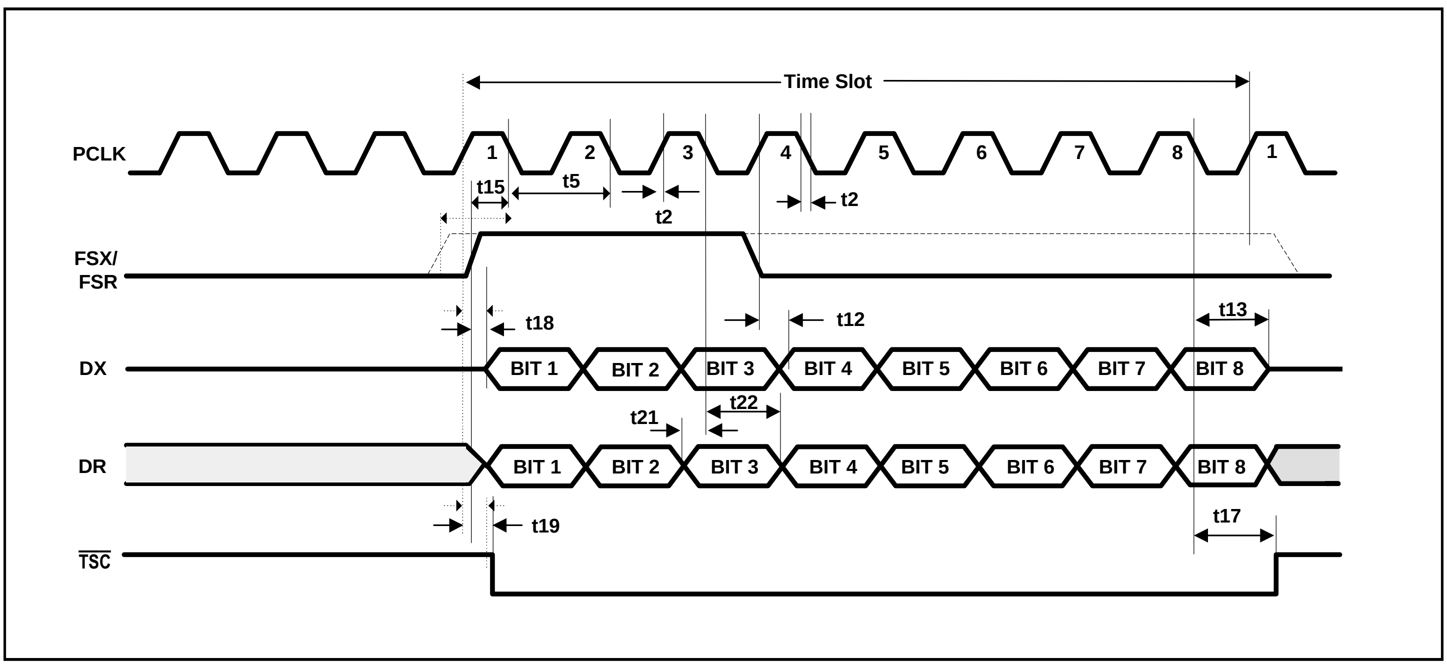


Figure 4. PCM Interface Timing for Long Frame Mode

ORDERING INFORMATION

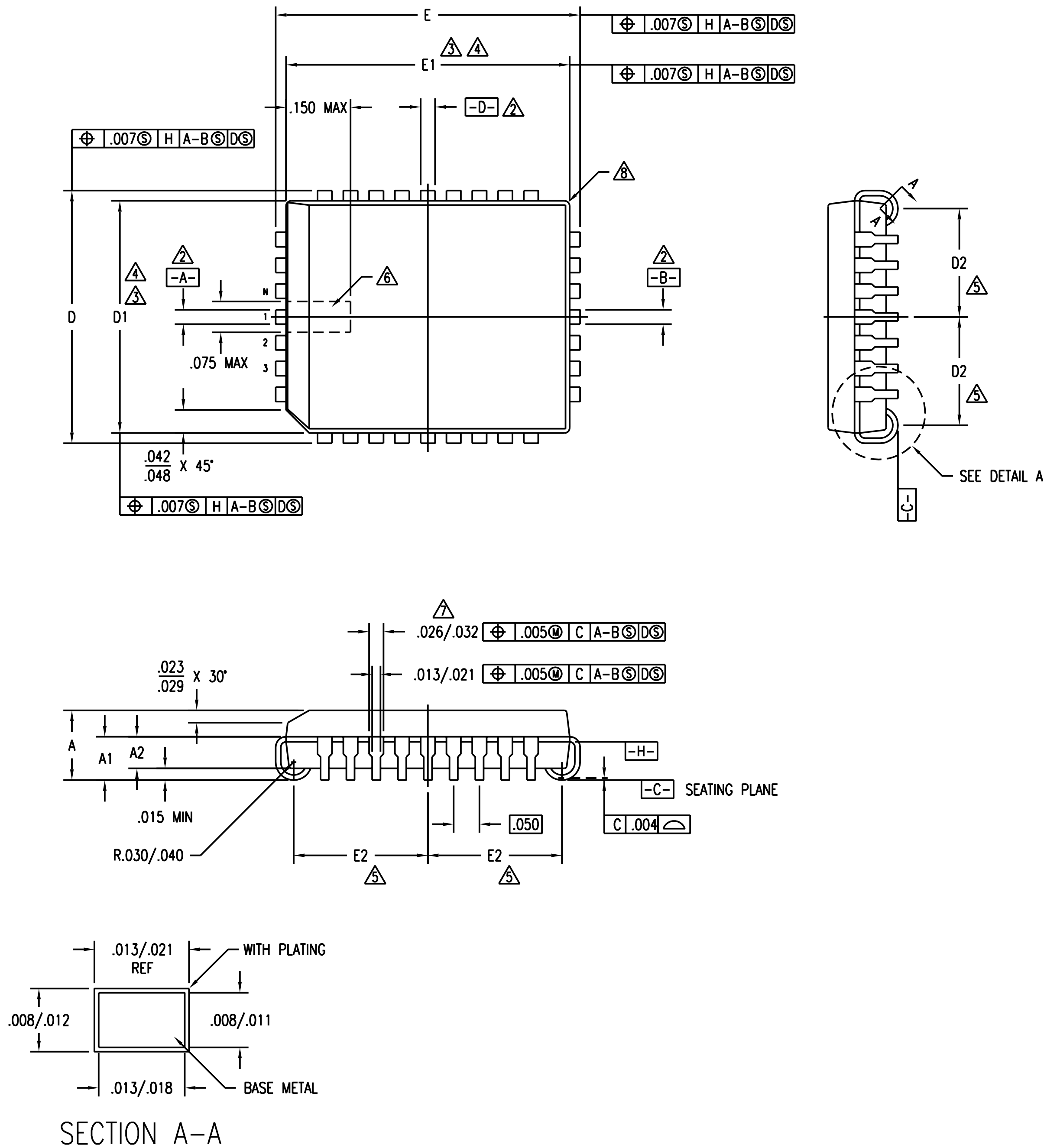
Device Type	Package	X Process/ Temperature Range	X

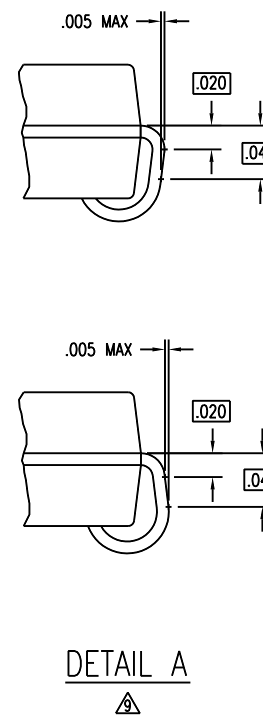
Blank	Tube	
8	Tape and Reel	
Blank	Industrial (-40 °C to +85 °C)	
JG	Green Plastic Leaded Chip Carrier (PLCC, PL32)	
821004J	Quad Non-Programmable PCM CODEC	

Data Sheet Document History

7/31/2014 Removed leaded device and added green. PDN CQ-13-01
11/02/2020 Updated adding Tape and Reel

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27646	07	REDRAW TO JEDEC FORMAT	03/15/95	
	08	ADD "GREEN" PL/PLG NOMENCLATURE	10/08/04	TU VU



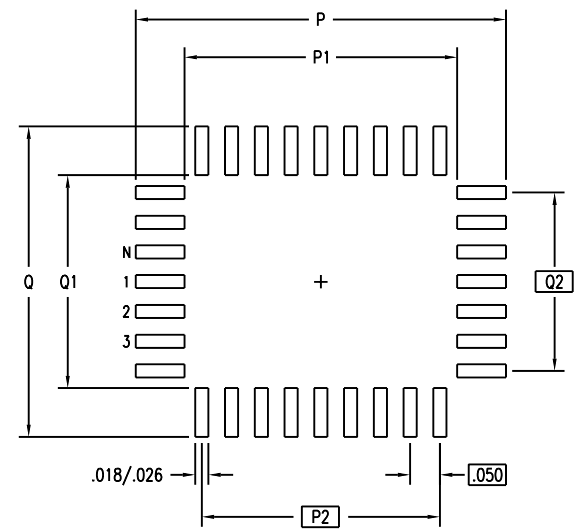


TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	IDT Integrated Device Technology, Inc. www.IDT.com 2975 Stender Way, Santa Clara, Ca. 95054 Phone: (408) 727-6116 Fax: (408) 492-8674 TWX: 910-338-2070	
APPROVALS / DATE	TITLE PL/PLG PACKAGE OUTLINE RECTANGULAR PLCC .050 PITCH	
DRAWN	SIZE C	DRAWING No. PSC-4013 / REV 08
CHECKED	DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27646	07	REDRAW TO JEDEC FORMAT	03/15/95	
	08	ADD "GREEN" PLG NOMENCLATURE	10/08/04	TU VU

SYMBOL	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX	
A	.125	.132	.140	
A1	.075	.078	.095	
A2	.053	–	.068	
D	.485	.490	.495	
D1	.449	.451	.453	3,4
D2	.195	.205	.215	5
E	.585	.590	.595	
E1	.549	.551	.553	3,4
E2	.245	.255	.265	5
ND	7			
NE	9			
N	32			

LAND PATTERN DIMENSIONS



	MIN	MAX
P	.620	.628
P1	.454	.462
P2	.400 BSC	
Q	.520	.562
Q1	.354	.362
Q2	.300 BSC	
N	32	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

5 DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE -C- CONTACT POINT

6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-016, VARIATION AE

TOLERANCES UNLESS SPECIFIED	
DECIMAL XX± XXX± XXXX±	ANGULAR ±
APPROVALS	DATE
DRAWN AA	08/15/90
CHECKED	

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TITLE PL/PLG PACKAGE OUTLINE RECTANGULAR PLCC .050 PITCH

SIZE	DRAWING No.	REV
C	PSC-4013	08

DO NOT SCALE DRAWING

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