8V9705x

High-Resolution Wideband RF Synthesizer / PLL

The 8V9705x evaluation board is designed to help the customer evaluate the Renesas 8V97051, 8V97051L, 8V97052, 8V97053, and 8V97053L wideband RF synthesizers.

When the board is connected to a PC running Timing Commander Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Features

- Develop configurations with Renesas RICBox software and upload to the EVB through USB
- Can be powered from the USB connection
- EVB is a combined evaluation with Renesas low-noise RF synthesizer and low-noise power supply regulators
- Clock output pairs are AC coupled and can be connected directly to test equipment through coax cables

PC Requirements

- IDT (Renesas) Timing Commander Software Installed
- USB 2.0 or USB 3.0 interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space: Min 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system

Board Contents

The 8V9705x evaluation board contains the following:

- 8V9705x Evaluation Board
- USB Cable

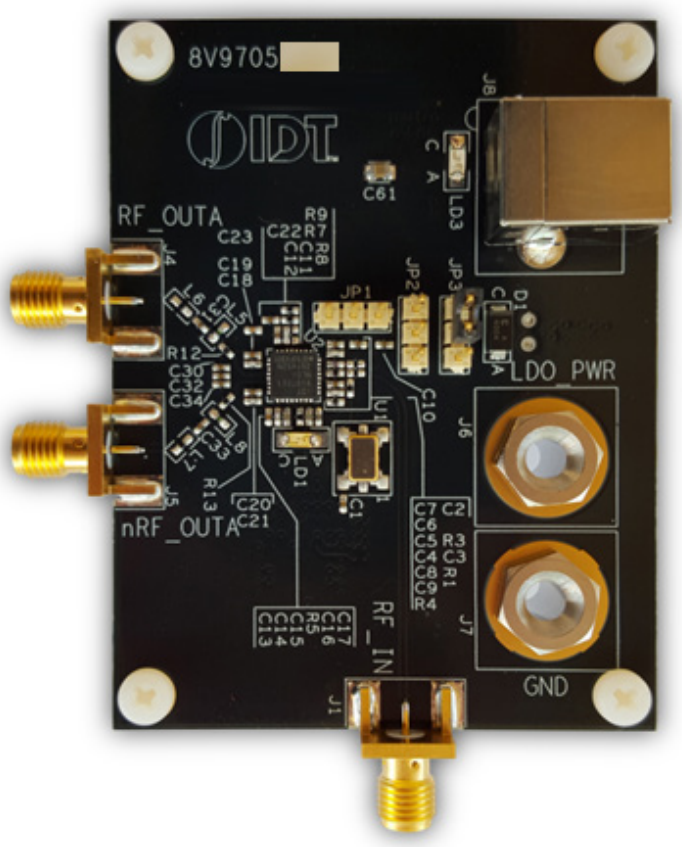

Figure 1. Block Diagram or Labeled Board Image

Contents

Figures

1. Functional Description

1.1 Setup and Configuration

The board ships with a 25MHz TXCO and is configured to power from the USB. No external reference is required and no external power source, aside from the USB connection, is required. Outputs are disabled by default. The device must be configured using Timing Commander in order to activate the output.

The 8V97052 can also accept an external RF input reference. As a result, there are three pins that are defined differently in the 8V97052 from the rest of 8V9705x devices. The following table summaries the differences.

Table 1. Functions of Pin 14, 15, and 16 in 8V97052 and Other 8V9705x Devices

Pins	14	15	16
8V9705x (except 8V97052)	RF_OUTB	nRF_OUTB	REF_IN
8V97052	Vvco	RF_IN	nRF_IN

The 8V9705x evaluation board supports an on-board VCO device (U9) that provides a RF input reference (2.4-2.5GHz) to Pin 16 of the 8V97052. Other 8V9705x variants have the second RF outputs (RF_OUTB/nRF_OUTB) that is not routed out on the evaluation board.

2. Board Design

The following diagram identifies the power supply jacks, USB connector, input and output SMA connectors, TCXO, etc., on the evaluation board.

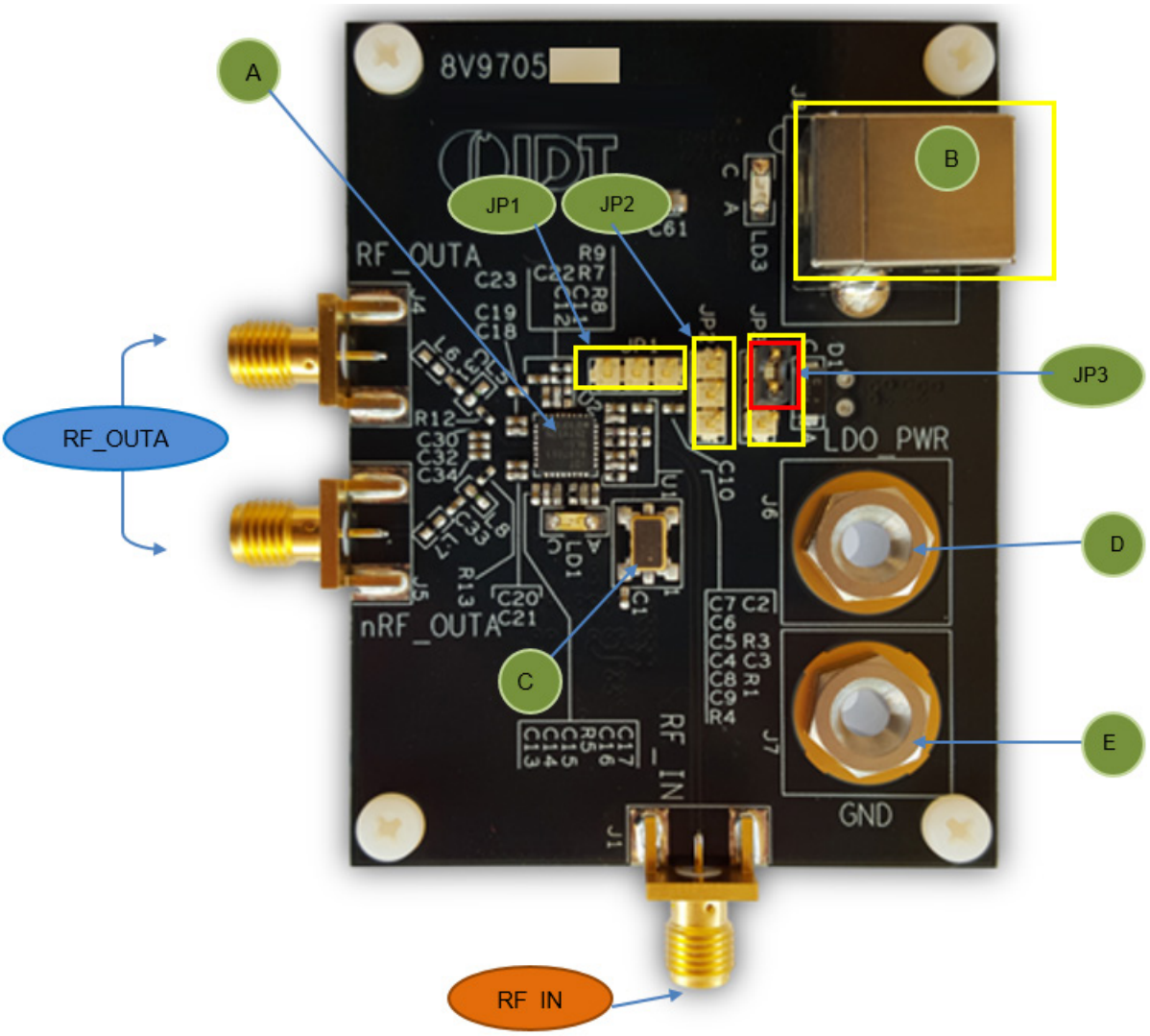

Figure 2. 8V9750x Evaluation Board – Top View

Legend

- Inputs – RF_IN: Reference input (the board requires re-work to enable this option.)
- Outputs – RF_OUTA: Open-drain, ac-coupled output.
- Other:
  - A – 8V9705x - the device to be evaluated
  - B – USB connector (also powers the board)
  - C – 25MHz TXCO (default reference source)
  - D – External LDO_POWER (alternate power source)
  - E – GND
  - JP1 – MUTE control (can be left floating)
  - JP2 – CE control (can be left floating)
  - JP3 – Power Source selector (USB vs LDO_PWR power source)

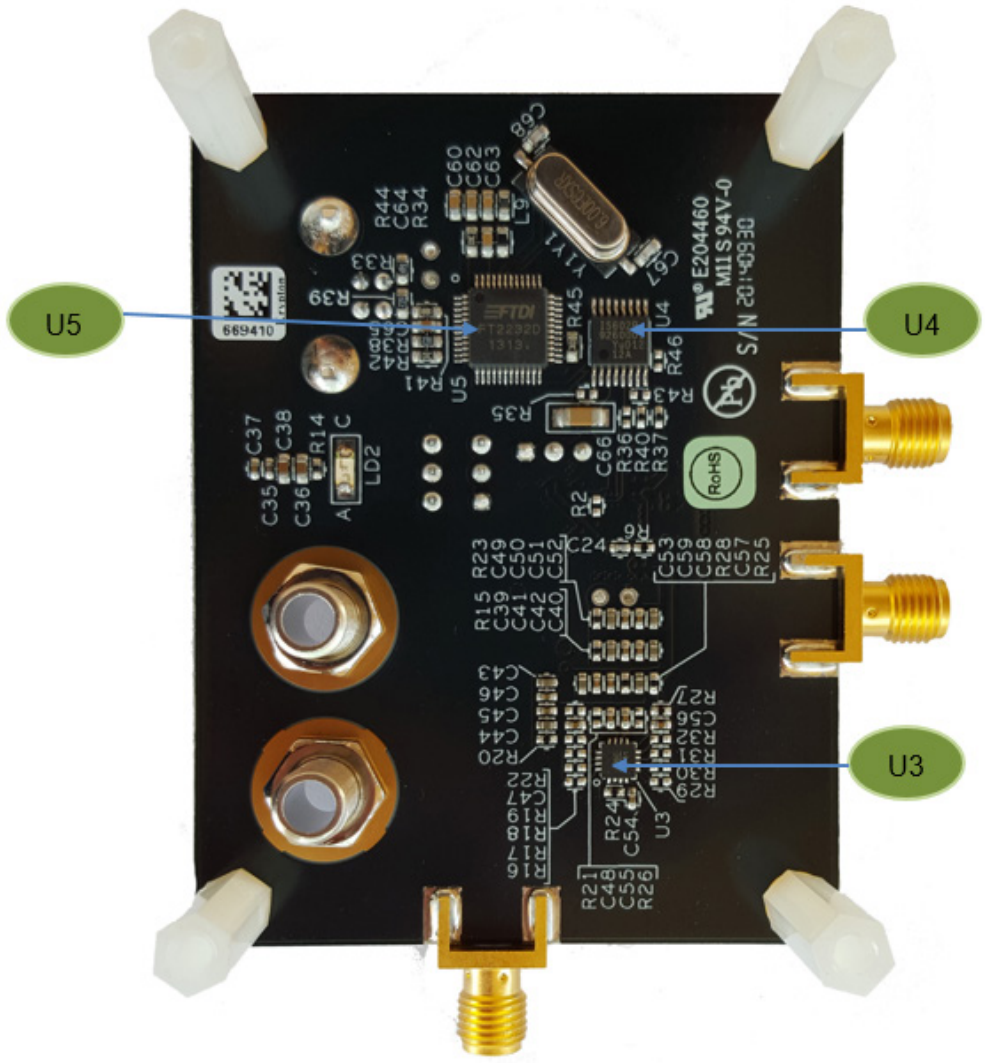

Figure 3. 8V9750x Evaluation Board – Bottom View

Legend

- U5 – FTDI USB-to-I2C chip
- U4 – USB-to-SPI translator
- U3 – LDO

2.1 Powering from an External Supply

The evaluation board is by default configured to power through the USB (see JP3 jumper position in Figure 4). To power the device from an external supply:

1. Set JP3 to the position shown in Figure 9.
2. Connect an external 4V supply to LDO_PWR (J6).
3. Connect the external supply Ground to GND (J7).

Figure 4. External Power Configuration

2.2 External Signal Reference Configuration

An on-board 25MHz TXCO provides the default source for RF_IN. In order to evaluate the device using an external signal reference, complete the following changes:

1. Remove R20. This powers down the TXCO.
2. Remove R1. This disconnects the TXCO from the input path.
3. If the external signal can be ac-coupled, then populate C3 = 0.1uF. For dc termination to ground, C3 = 0ohm.
4. Populate R3 = 50ohm. This provides a termination for the input signal.
5. Replace C4 = 0.1uF. The input is ac-coupled into the device, which provides its own internal re-bias.
6. Connect the external signal reference to J1 using a 50ohm cable.

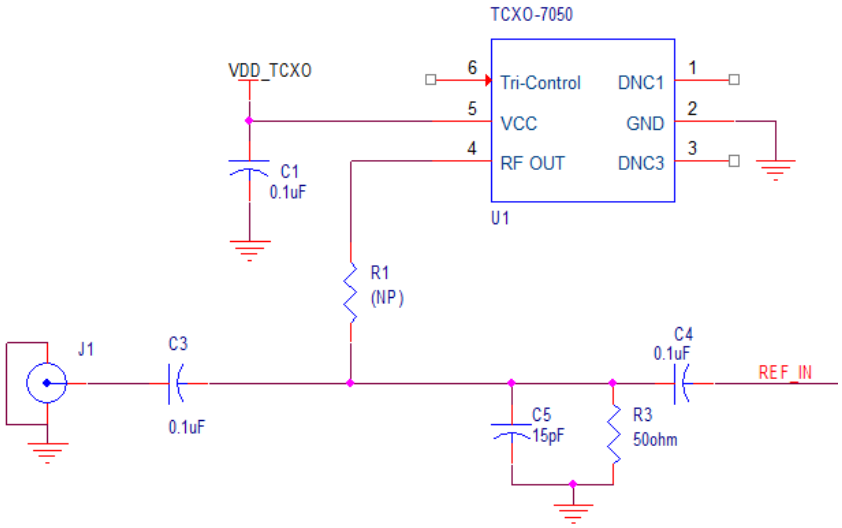

Figure 5. External Signal Reference Configuration

2.3 DC Controls

- JP1 – MUTE control: RF_OUTA and RF_OUTB Power-Down. A logic low on this pin mutes the RF_OUT outputs and puts them in high-impedance. This function is also SPI controllable and in this case also allows the power down of either RF_OUTA or RF_OUTB. This jumper can be left floating for normal operation.
- JP2 – Chip Enable: Powers down the device on logic Low, with charge pump put into a High-Impedance mode. Powers up the device on logic High. This jumper can be left floating for normal operation.

2.4 Schematic Diagrams

The following figures are schematics that are applicable to specific sections of this manual. The complete schematics are available in a separate document.

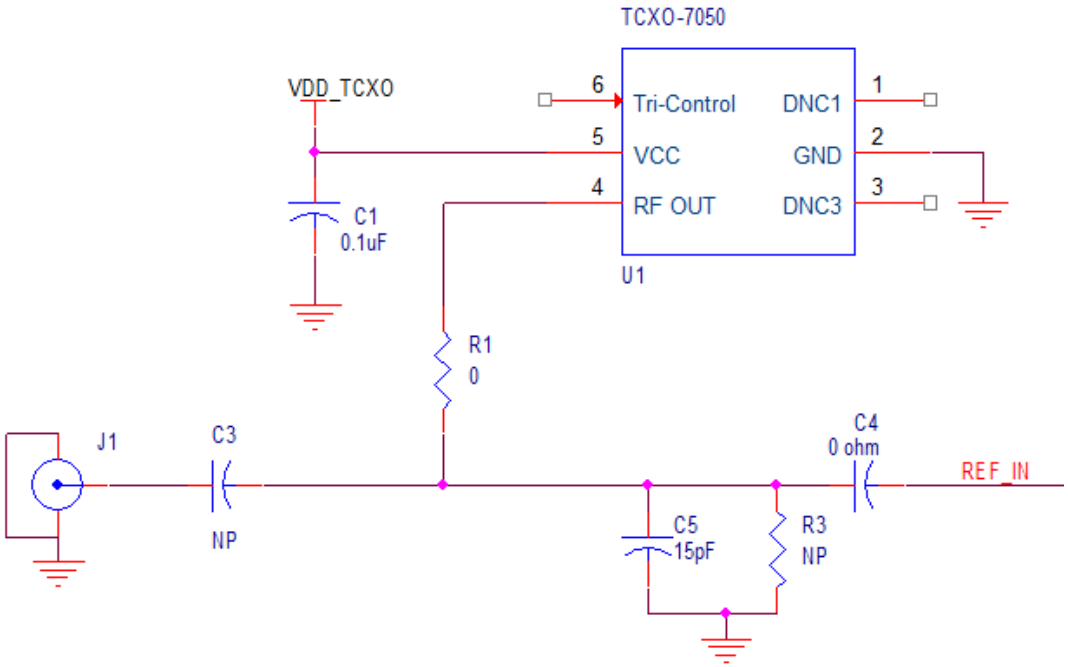

Figure 6. Input Schematic

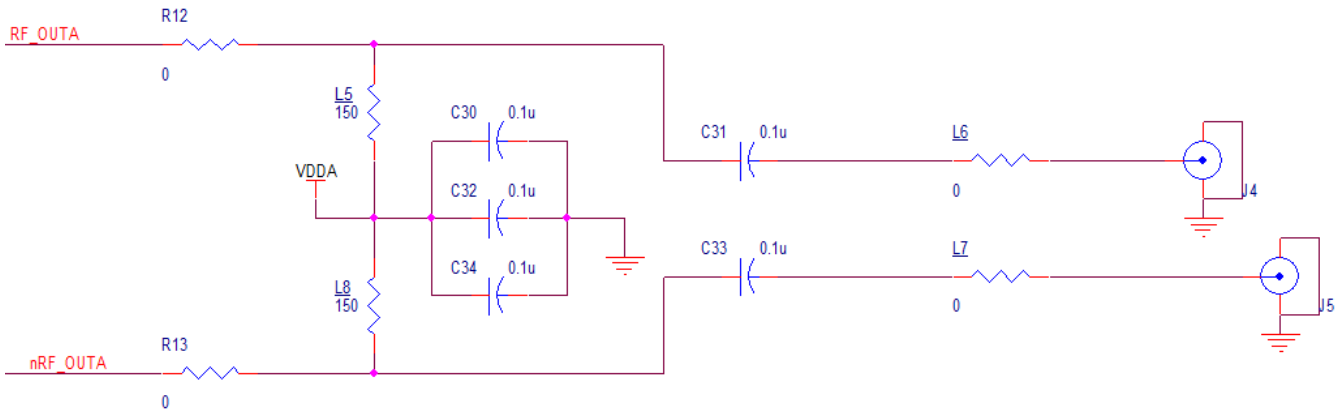

Figure 7. Output Termination Schematic

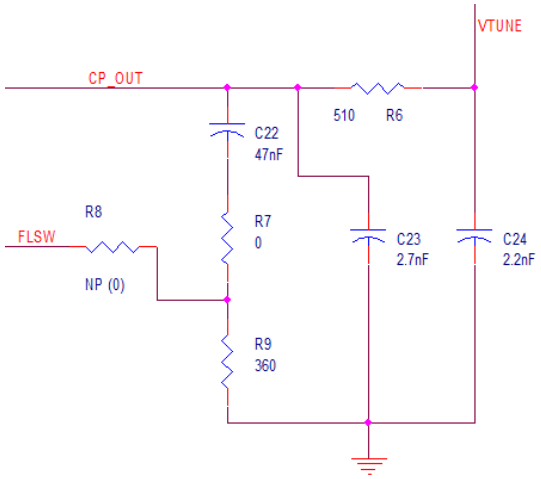

Figure 8. Loop Filter Schematic

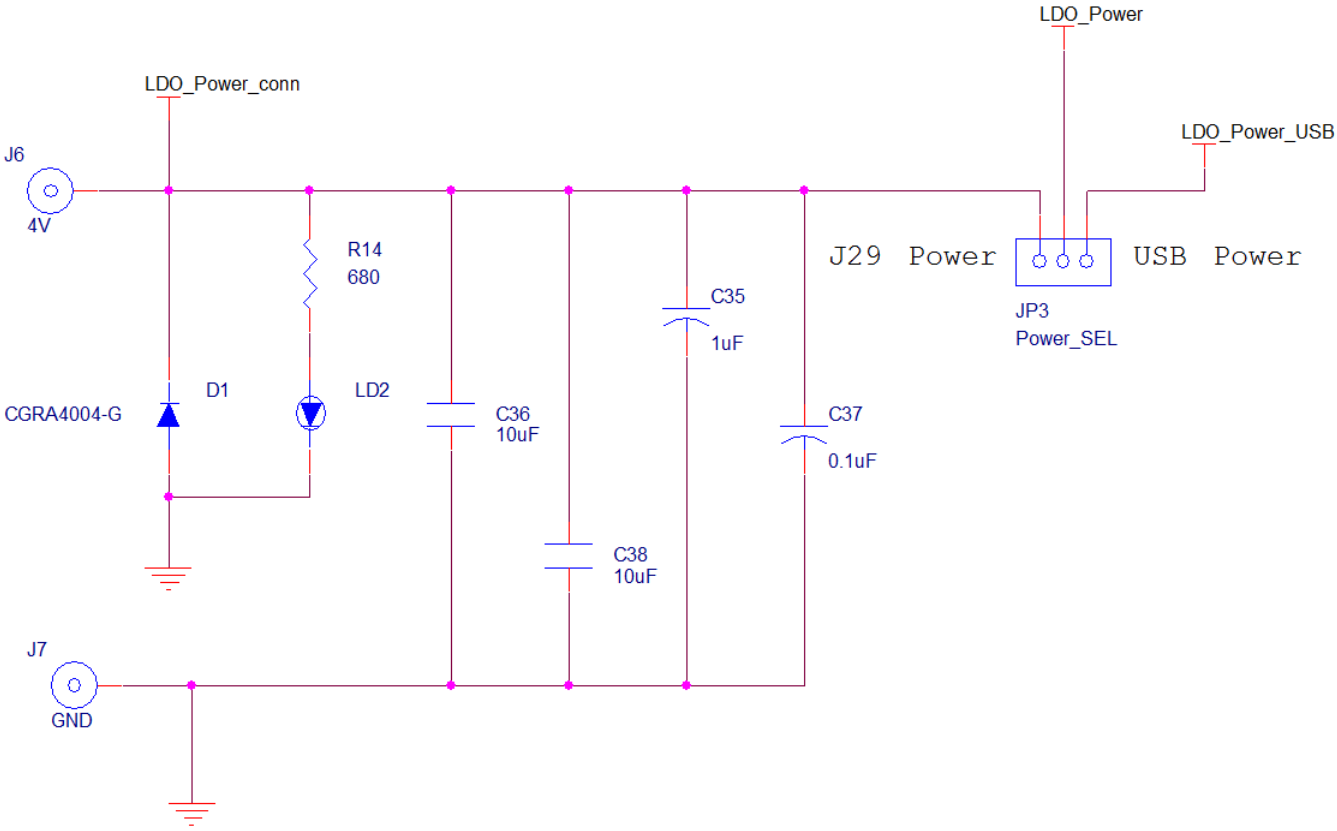

Figure 9. Power Source Selection Schematic

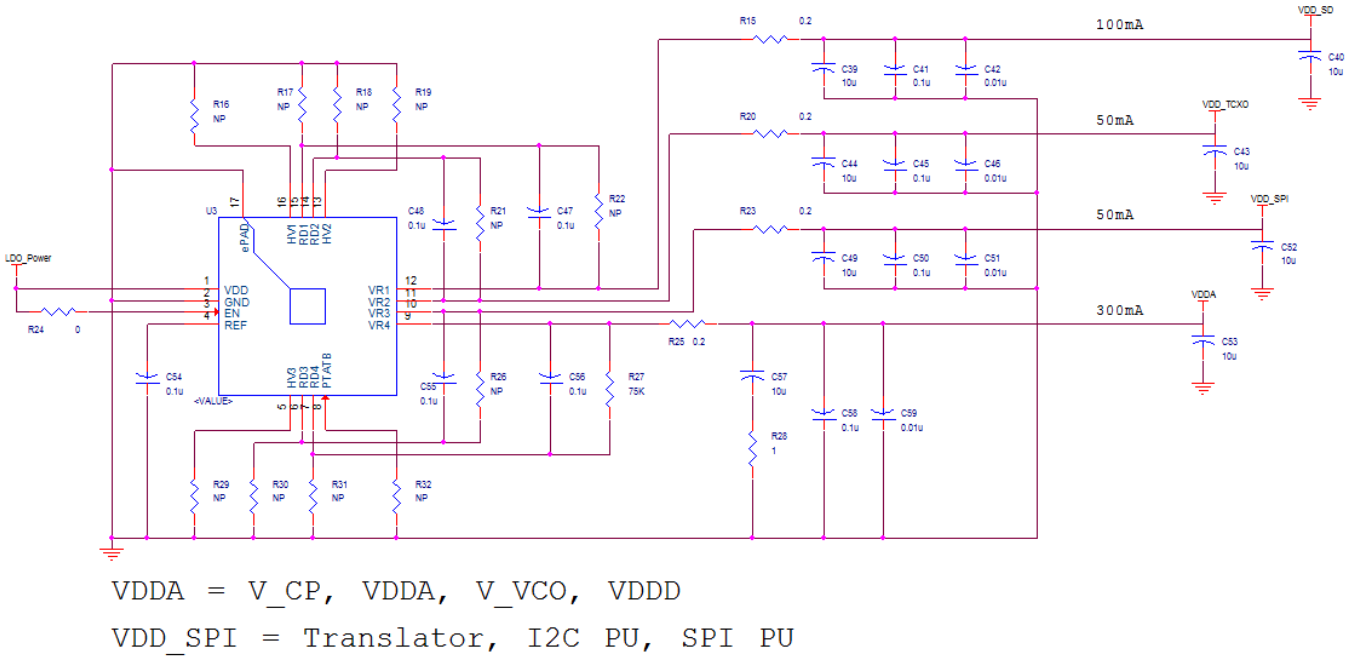

Figure 10. LDO Power Schematic

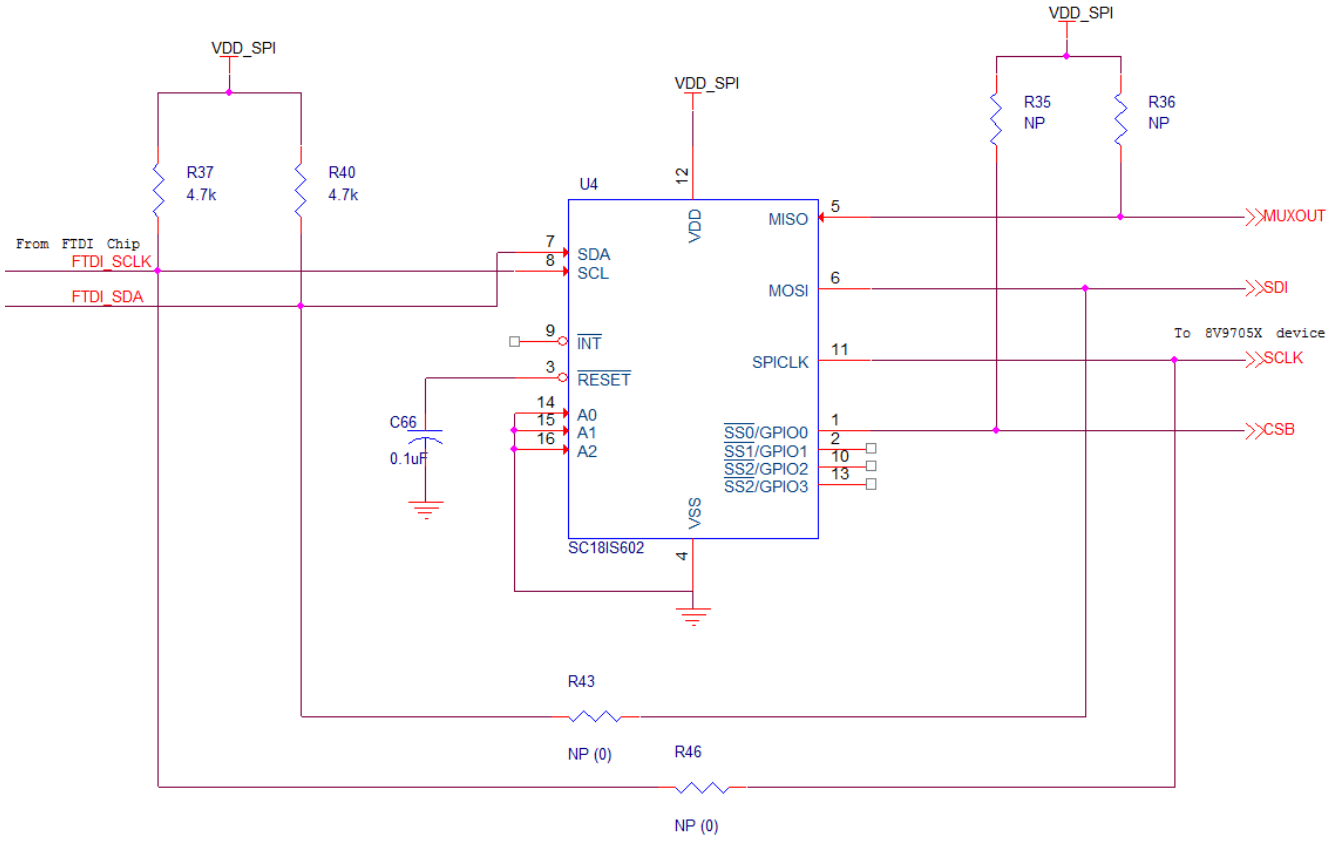

Figure 11. I2C-to-SPI Translation Schematic

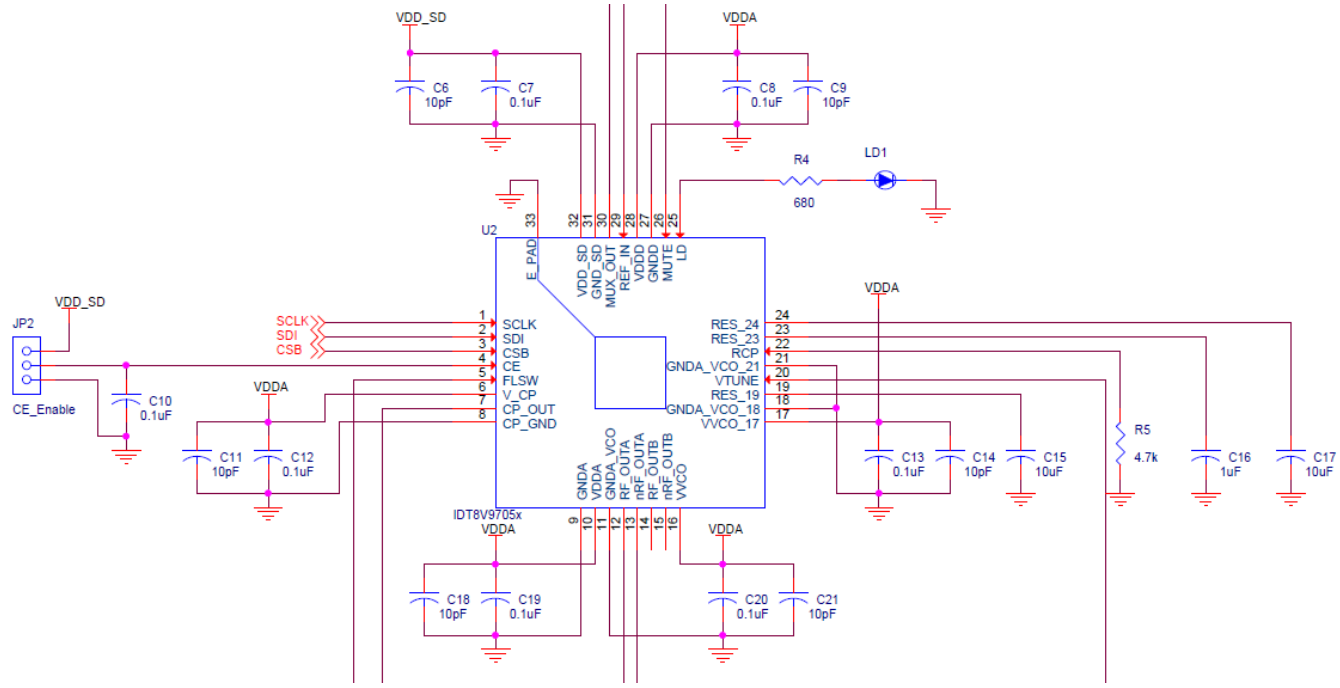

Figure 12. 8V9705x DUT Schematic

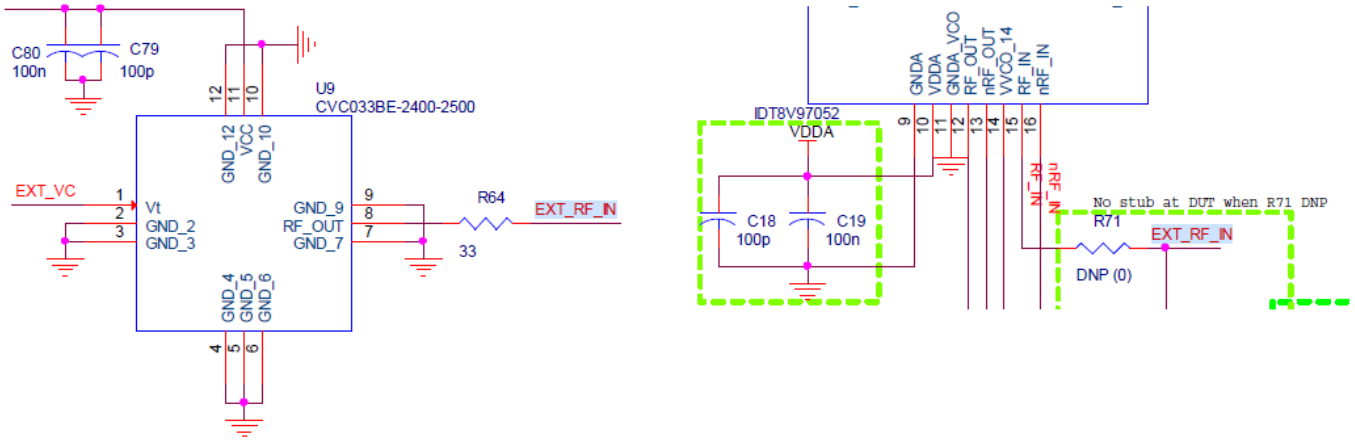

Figure 10. 8V97052 External RF Input Reference

3. Ordering Information

Part Number	Description
8V97052-EVK	8V9705x Evaluation Board

4. Revision History

Revision	Date	Description
1.0	May 20, 2021	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.