Auxiliary Smartphone Battery Power Management Circuit

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Introduction

Many smartphone users have the need for prolonged battery life and employ the use of auxiliary power banks. These allow extended use of their smartphones by up to 6 times (depending on the capacity of the power bank). Power banks are usually mounted on back of the smartphone and they are connected via a charging connector (lightning or USB). For enhanced user experience, they are allowed to be charged using the same smartphone charger and the user doesn't have to worry about charging it separately. Circuit design of these devices include LiPo battery power bank, charging circuit for the power bank, the power distribution switch, power management control and the DC-DC boost converter (used to provide the phone with the required voltage (5V).

Figure 1 depicts the functional hardware design of an auxiliary smartphone battery power management circuit. It is composed of the following segments:

- *Power management control (PMC) unit* – this is the main logic unit of the device. It decides whether to route power to the smartphone or to the additional power bank. It decides when to turn the boost DC-DC converter on, in order to stop the internal battery power to smartphone.
- *Power distribution switch (PDS): It* is composed of MOSFETs that are controlled by the PMC unit.
- *LiPo battery* – For this design, a single cell 3.7V 1000mAh battery is selected as the power bank unit.
- *LiPo charger* – A controllable DC-DC buck converter design is used as a LiPo charger.

Boost DC-DC Converter – boost DC-DC converter is required to boost the LiPo battery 3.7V voltage to 5V required by the smartphone.

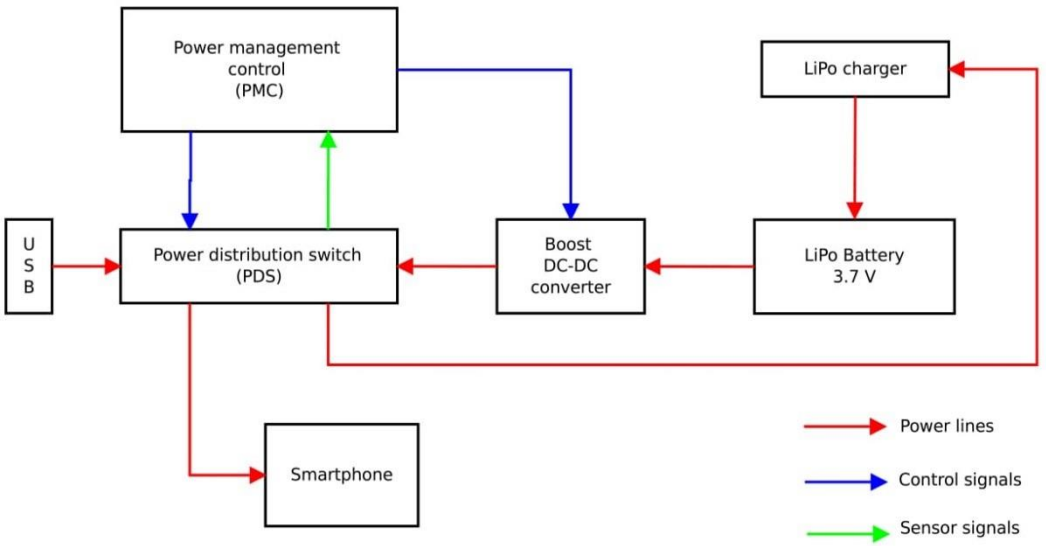

Figure 1. Functional diagram

Power management control (PMC) unit design and implementation

The power management control (PMC) unit uses inputs from the rest of the device to make power routing decisions. PMC controls the PDS and the DC-DC boost converter.

Inputs to PMC are:

- Charger present indicator *(CHG_IN)*.
- Device power consumption *(CUR_SENSE)* indicator. This indicator will be implemented using the current sensing method. In case the smartphone is drawing current below the determined threshold, the PMC will route power from the input to LiPo charger as well, so that the power bank can be charged. If the current is above the determined threshold, power from the input will be routed to the smartphone only.
- Power bank voltage indicator *(VBAT)*. This indicator is used so that PMC can determine whether to turn the DC-DC boost converter on (to step up voltage from the power bank and provide it to smartphone) or not.

Outputs from PMC are:

- LiPo charger control *(LiPO_CHG)* – this output will send signal to the PDS to route power to the LiPo charger.
- Smartphone power control *(S_PWR)* – this output will send signal to the PDS to route power from input to the smartphone.
- Boost control *(BOOST_CTRL)* – this output will turn the boost converter on and send a signal to the PDS to route power from the boost to the smartphone.

PMC is a digital logic circuit with 3 inputs and 3 outputs. This can be easily implemented using LUT tables. Three 3-bit LUT tables are used for implementation of PMC using GreenPAK4.

Figure 2 shows the functional table for the PMC input and outputs.

INPUTS			OUTPUTS		
VBAT	CHG_IN	CUR_SENSE	LIPO_CHG	S_PWR	BOOST_CTRL
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	1	1	0
1	1	1	0	1	0

Figure 2. LUT Tables

Each output is implemented using one 3bit GreenPAK4 LUT unit. Inputs from the pins are routed to each LUT table.

Figure 3 explains the implementation of the PMC using GreenPAK4.

Power distribution switch design and implementation

The power distribution switch is controlled by the PMC outputs *LIPO_CHG, S_PWR, BOOST_CTRL.*

Figure 4 depicts block schematics of the PDS. Control signals are provided by the PMC. PDS provides sensor signals to the PMC: *CHG_IN* and *CUR_SENSE*.

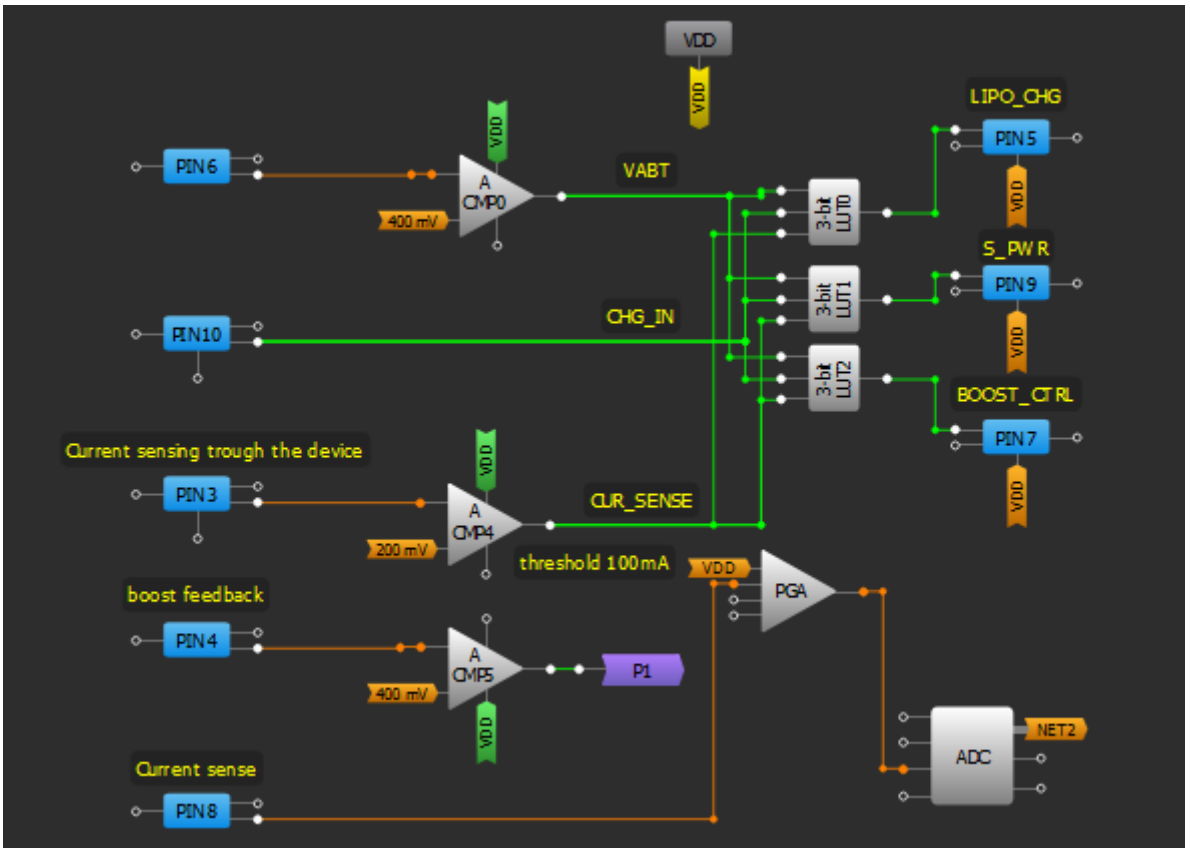

Figure 3. LUT tables implementation using GreenPAK4

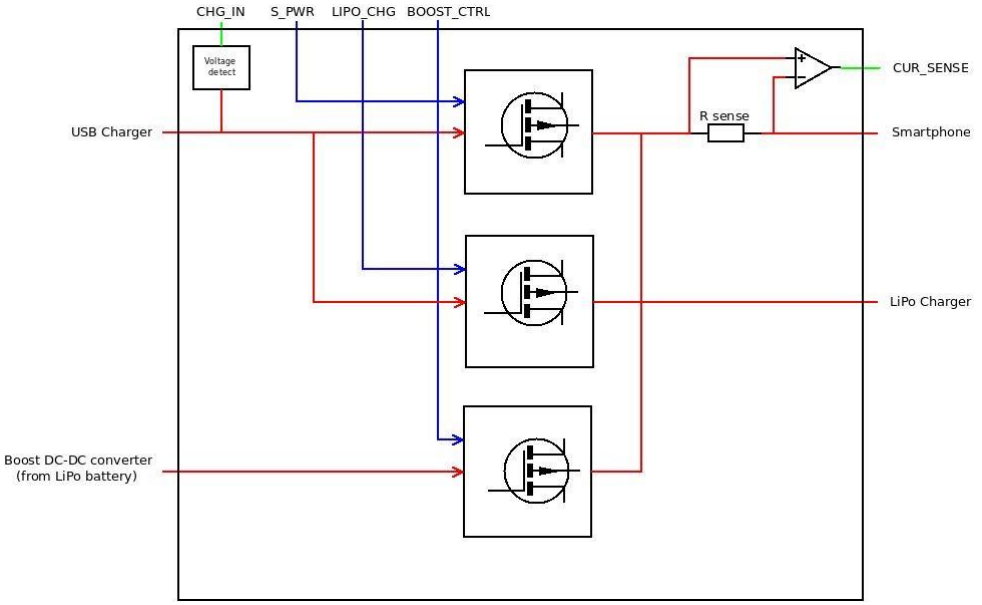

Figure 4. Power distribution switch design

Current sensing is used at two places in the design and Figure 5 shows the schematic used for this task. The SLG88101 OP-AMP is used to make the current sensing circuit, and as it is dual OP-AMP, only one IC is used.

Figure 6 depicts the PDS implementation schematic. A GreenFET Load Switch is used for PDS implementation. The SLG59M1709 is a perfect match for load switching since it features maximum continuous current of 4A, which is 2-3 times more than the required charging current for most of smartphones on market.

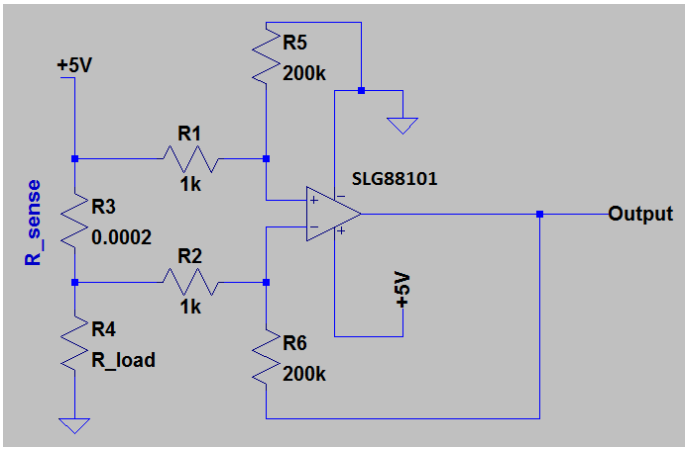

Figure 5. Current sensing circuit

LiPo charger design and implementation

The LiPo charger is implemented using a controllable buck DC-DC converter. Constant current (CC) and Constant Voltage (CV) modes are used to charge the LiPo battery.

CC mode is used when battery voltage is below 4.2V, and CV mode is used when battery voltage is above 4.15V. Figure 7 shows the charging curve for the LiPo battery using both CC and CV modes. In order to implement this charging method, the charging current and LiPo battery voltage are monitored.

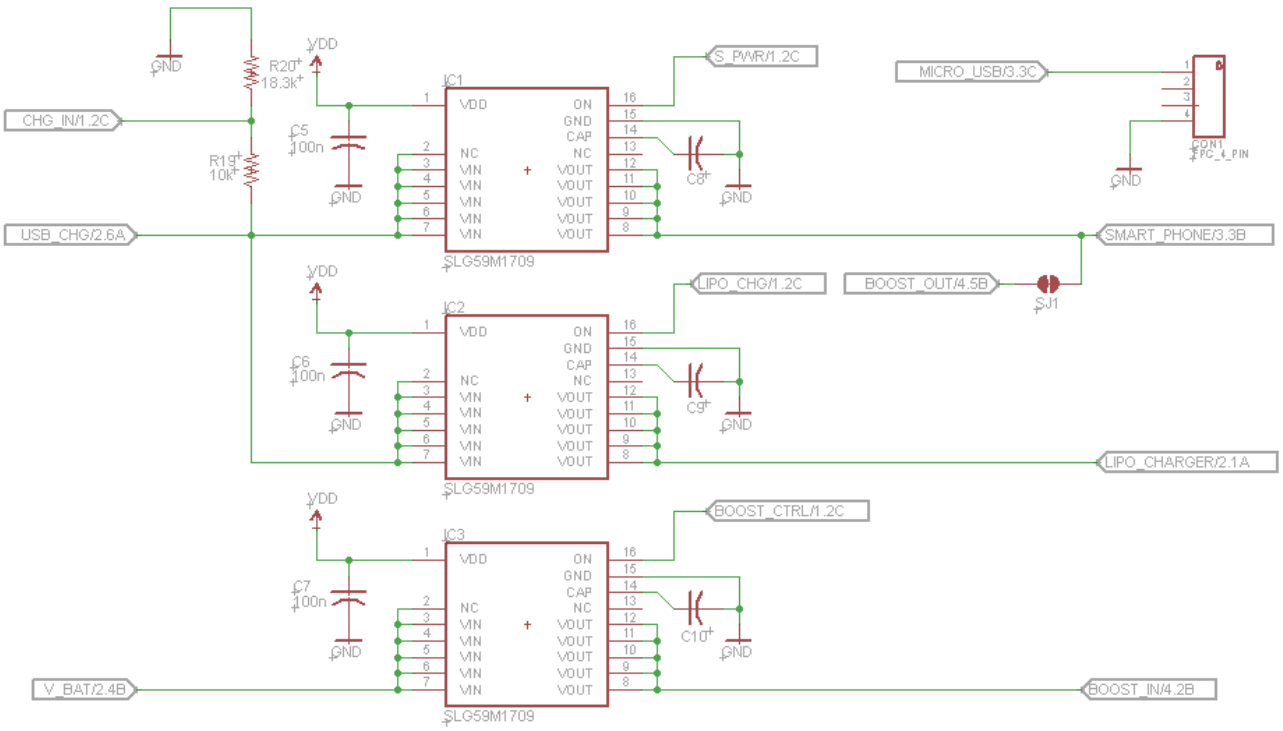

Figure 6. Power distribution switch implementation

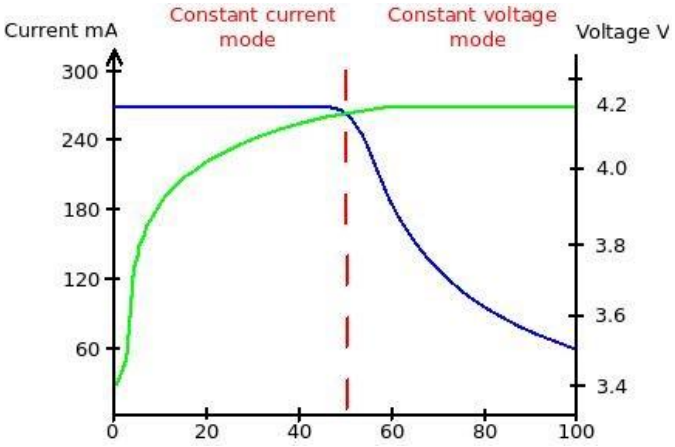

Figure 7. LiPo battery charging modes

The input from the USB charger is stepped down using a buck DC-DC converter that provides a 4.2V output. In order to achieve the constant current (CC) mode, the average voltage on the battery must be variable. Current is tracked using the current resistor and the OP-AMP. Output from the OP-AMP is compared with a specific voltage threshold. When the current through the battery goes above the specified current, output from the PWM is simply disabled. When it goes back under the threshold, output from the PWM is enabled again.

When battery voltage reaches 4.15V, the LiPo charger goes into CV mode and it provides a constant 4.2V output.

Current is sensed again and it is compared with different thresholds. When it reaches 10% of the maximum charging current, it sends a signal to terminate the charging and the PWM output. Current sensing is implemented using approach described in Figure 5 and the SLG88101 OP-AMP.

Figure 8 depicts the buck DC-DC converter analog design.

Following are parameters used for the buck converter design:

- $V_{in(max)}$=5.1V, max voltage input
- V_{out}=4.2V, output voltage
- I_{out}=1.2A, max output current
- f_s=62.5kHz, minimum switching frequency
- ΔV_{out}=50mV,output voltage ripple
- n=0.85, efficiency

Above are set parameters that are used for calculation of the next parameters for buck:

- $D_{max}=\frac{Vout*n}{Vin(max)}=0.7\rightarrow 70\%$, max duty cycle
- ΔI_L=(0.2 to 0.4)*I_{out}=0.24A, current ripple
- L=(Vout*(Vin(max)-Vout))/(ΔIL*fs*Vin(max))=49.41uH, minimum inductor
- IF=Iout*(1-D) =0.36A, diode current
- Cout(min)=ΔIL/(8*fs*ΔVout) = 10uF, minimum capacitor
- Isw(max) =ΔIL/2+Iout = 1.32A , max switching current

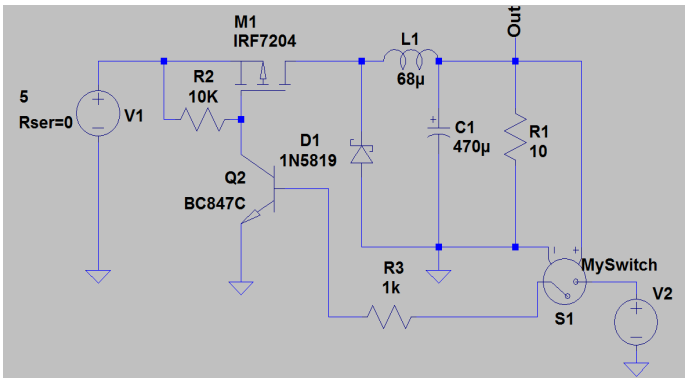

Figure 8. Buck design

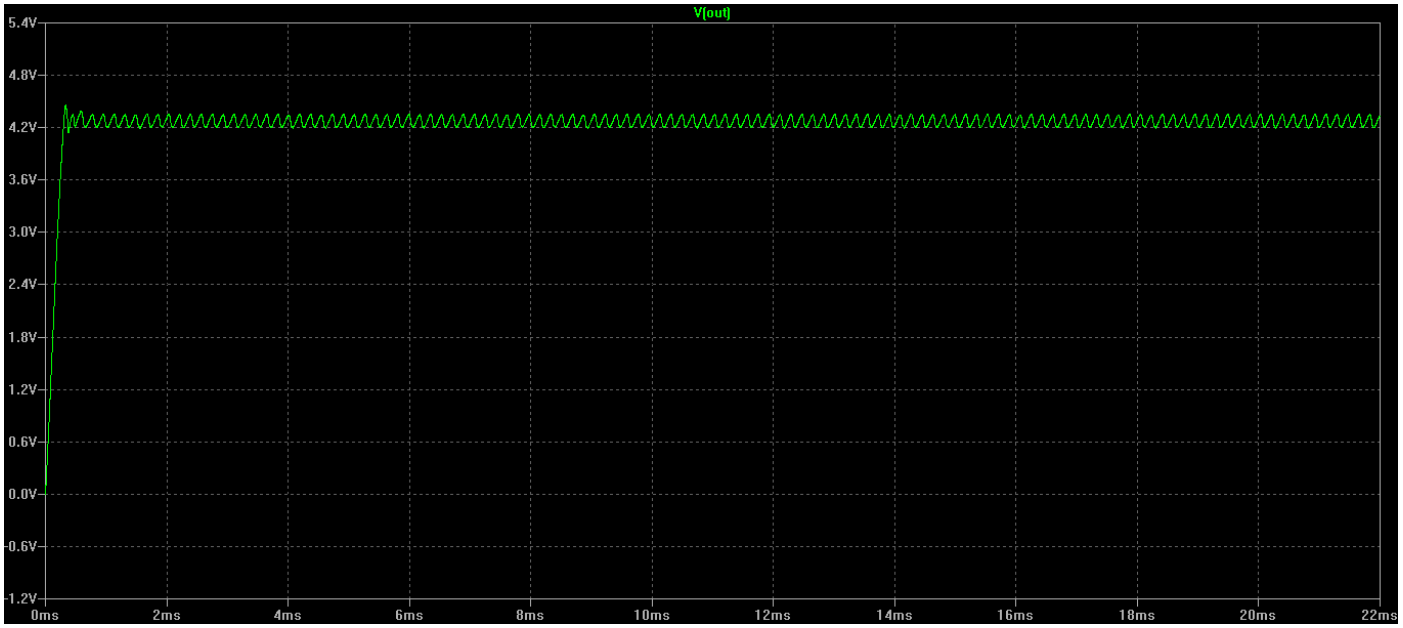

Figure 9. Buck design simulation using LTSpice – output voltage

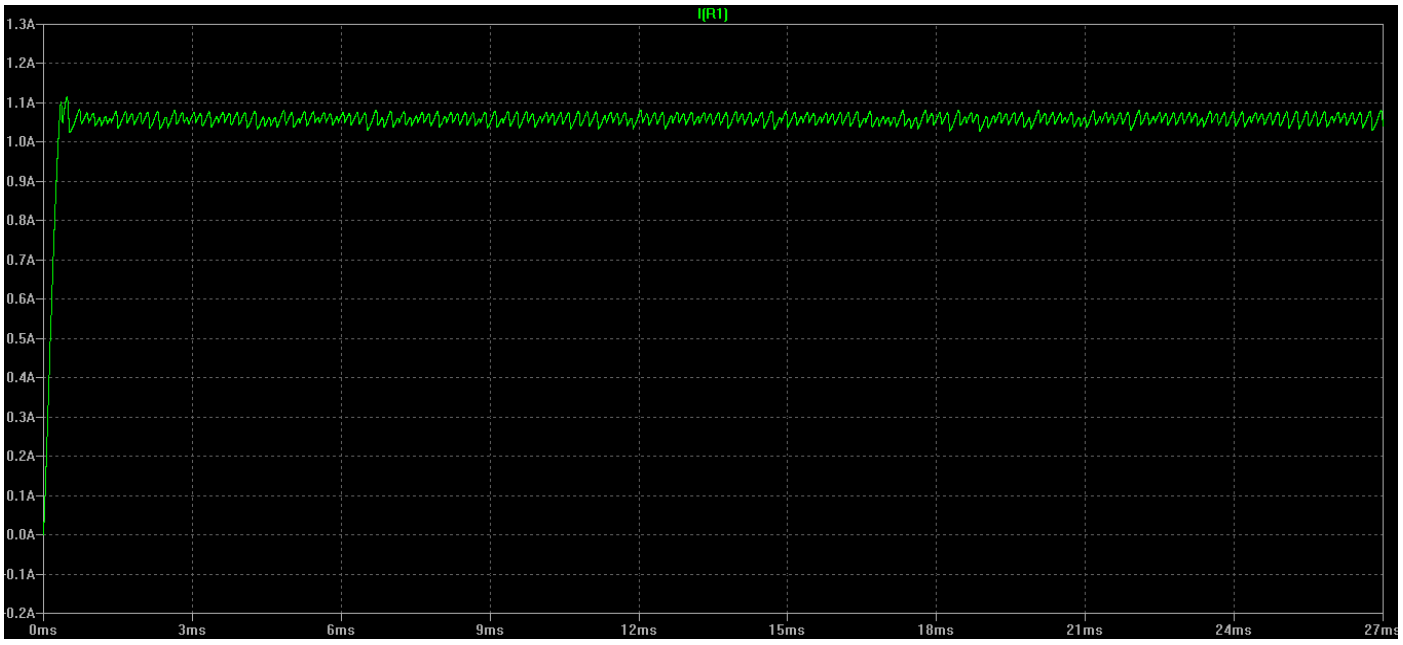

Figure 10. Buck design simulation using LTSpice – output current

Figures 9 and 10 show the simulation results for buck design using LTSpice simulator. The PWM signal for buck can be implemented using the PWM module of the GreenPAK4. The PWM2 and CNT8 modules are used for implementation of the PWM signal.

Figure 11 shows the results of the above design implementation - PWM signal generated by the GreenPAK4 and the output voltage (CH2) of 4.2V (which verifies buck design and simulation results).

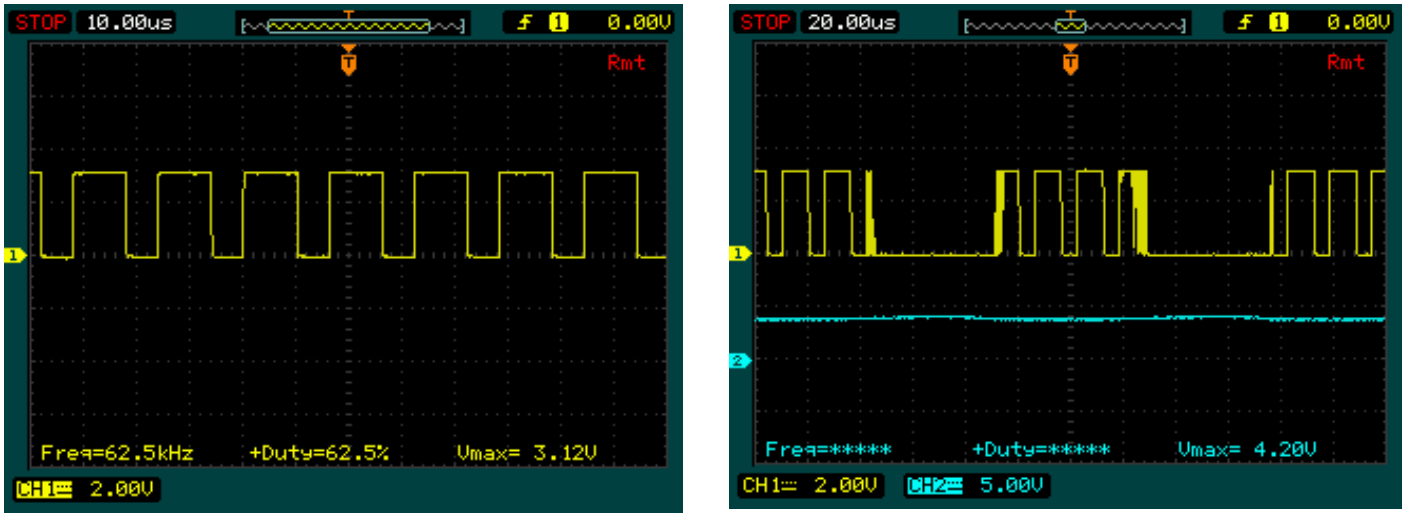

Figure 11. Buck design implementation measurements – PWM and output voltage

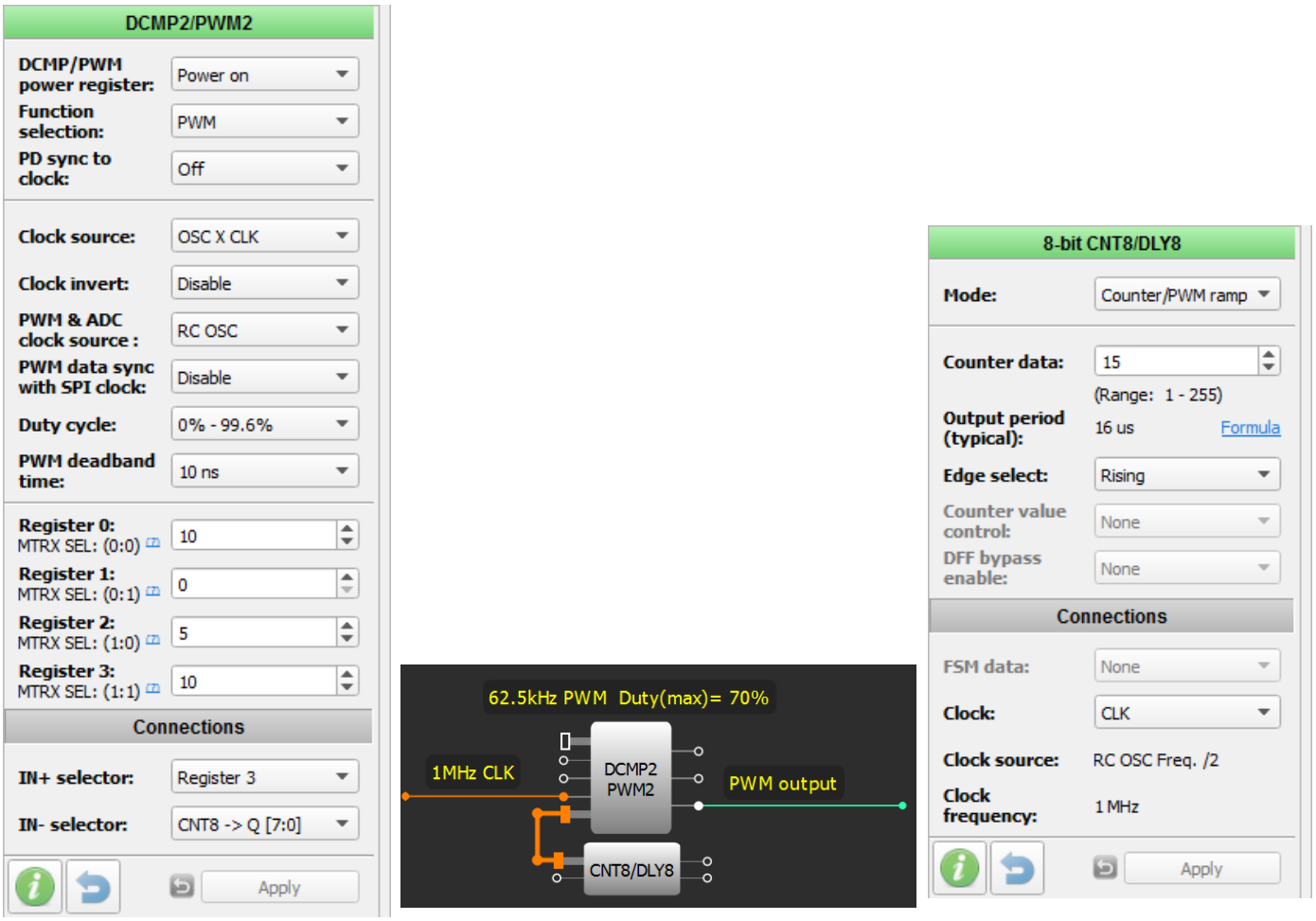

Figure 12. PWM signal generation used for buck – GreenPAK4 implementation

Figure 12 depicts the implementation parameters used for the PWM signal for buck converter. The PWM2 and CNT8 modules are used to generate the PWM signal. The IN+ selector for the PWM2 module is set to Register 3, and the IN- to counter (CNT8). Switching frequency is determined by the following formula:

$$fsw = \frac{fclk}{Counter_{data} + 1}$$

Duty cycle is determined by the value present in Regsiter3. CNT8 is set to count to 15 and Register3 to 10, in order to achieve the switching frequency of 62.5kHz with a 62.5% duty cycle.

Figure 13 depicts the LiPo charger implementation using the GreenPAK4. Following are I/0 pins used for LiPo charger implementation:

- PIN12, input pin for over-temperature protection
- PIN13, input pin for CC/CV switch
- PIN14, output pin for over-voltage and over-temperature indication
- PIN15, input pin za CV mode
- PIN16, input pin for over-volatge protection
- PIN17, output pin for Buck PWM
- PIN19, CC/CV switching indication

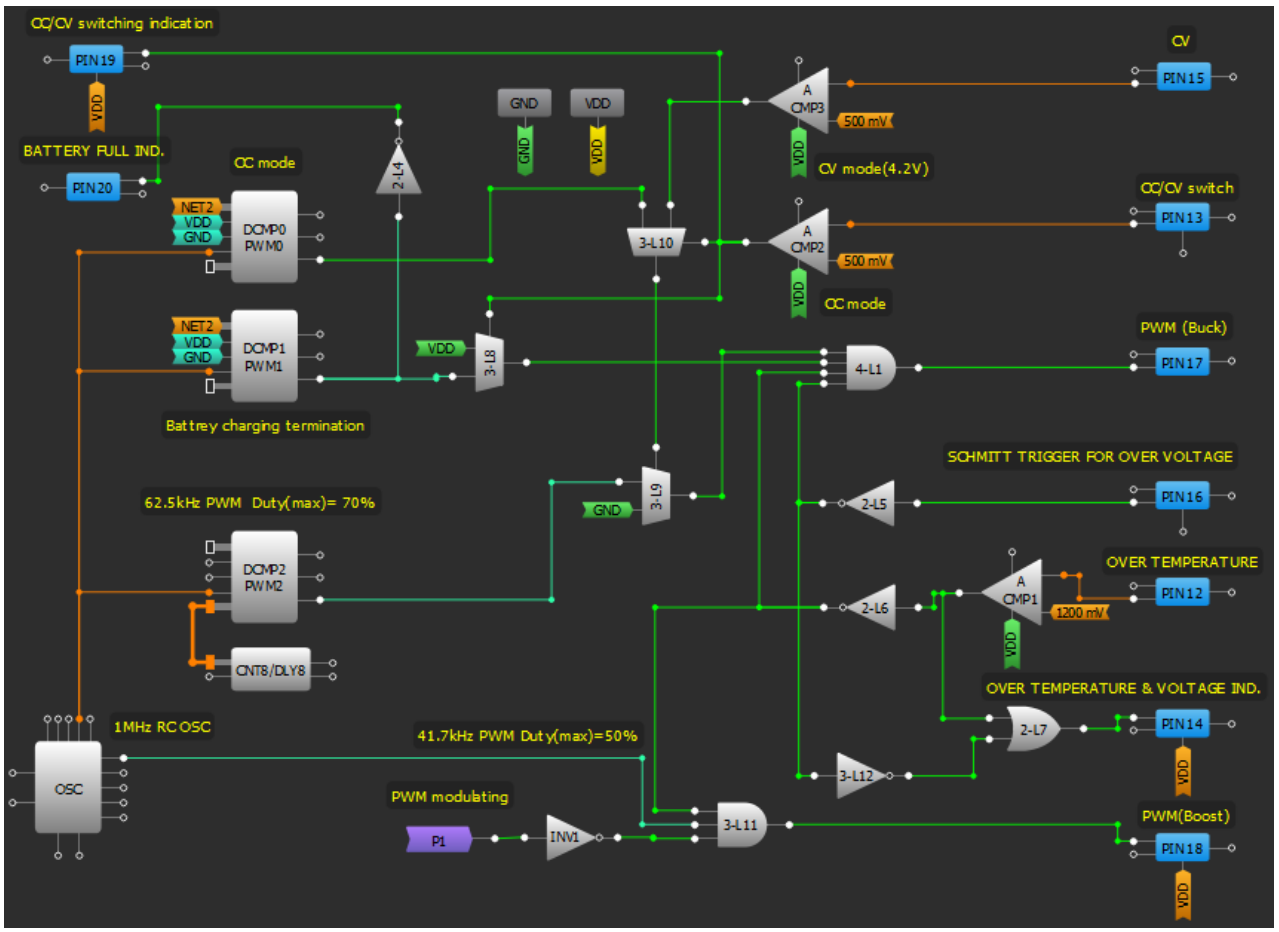

Figure 13. GreenPAK4 implementation (Matrix 1)

- PIN20, battery full indication
- PIN8, ADC input (Current sensing trough the battery)

Following are GreenPAK4 components used for LiPo charger implementation:

- PGA
- ADC
- DCMP0/PWM0, used as digital comparator
- DCMP1/PWM1, used as digital comparator
- DCMP2/PWM2, used as PWM signal generator for buck
- CNT8/DLY8, used as counter
- OSC, used for clock generation and boost PWM signal generation
- ACMP1, analogue comparator H=50mV
- ACMP2, analogue comparator H=50mV
- ACMP3, analogue comparator H=0mV
- 3-L8, multiplexer
- 3-L9, multiplexer
- 3-L10, multiplexer
- 4-L1, AND logic gate
- 2-L7, OR logic gate
- 2-L4, inverter
- 2-L5, inverter
- 2-L6, inverter
- 3-L12, inverter

The design of the LiPo charger is already explained; the following text will put focus on the implementation using the GreenPAK4.

CC/CV switch:

The CC/CV switch is responsible to switch the LiPo charger between two charging modes. If voltage on the battery is below 4.15V, the charger stays in CC mode; if it is equal or slightly above 4.15V, charger is in CV mode.

Figure 14 depicts the CC/CV switch using an analog comparator ACMP2. Input for the ACMP2 is PIN13 which is connected to an external voltage divider shown on Figure 15. Output of the ACMP2 is connected as a selector bit of the 3L10 multiplexer. When ACMP2 is 0, the 3L10 will output left channel (CC mode) and if the voltage on battery is above 4.15V, it will output 1 that will make 3L10 output the right channel (CV mode).

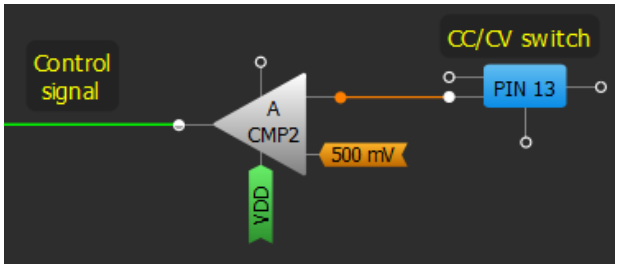

Figure 14. CC/CV switch implementation

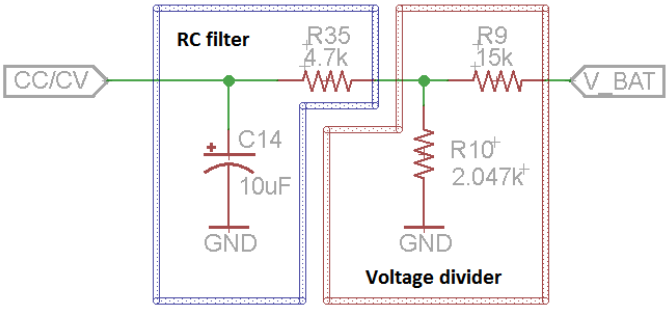

Figure 15 – Voltage divider and RC LPF for the CC/CV switch

IN- on ACPM2 is set to 500 mV, so in order to detect whether the voltage on the battery is above 4.15V, the voltage resistor must be designed to output 500mV when input (Vbat) is 4.15V. Following is the required calculation for the voltage divider:

$$R2 = \frac{Vt}{\frac{Vbat - Vt}{R1}}$$

- Vt = 500mV, output
- Vbat = 4150mV, voltage on battery
- R1 = 15Kohm

A simple RC LP filter is used to cancel any noise on input to the CC/CV switch. Cut off frequency of the designed filter is 3.38Hz. Also, 5mV hysteresis is used on ACMP2 as the voltage on the battery varies during the charging. Figure 16 shows ACMP2 settings.

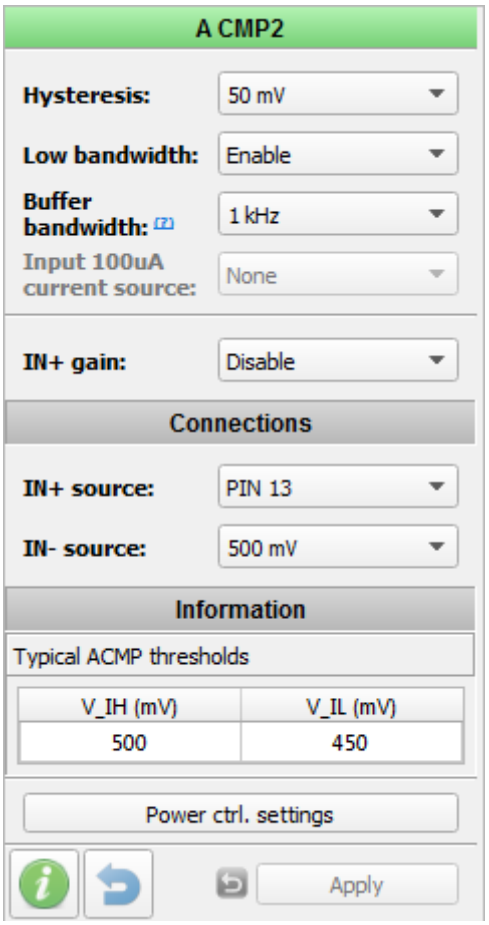

Figure 16. ACMP2 settings

CC mode

The CC (constant current) mode is used when voltage on the battery is below 4.2V. In this mode, circuitry is needed to maintain constant current through the battery.

For current sensing, the circuitry in Figure 5 is used. R_sense is set to 2mOhm. The gain of the current sensing OP-AMP is set to 200. If current through R_sense is 0.5A, voltage on the input of OP-AMP is Vin = I*R_sense=1mV. When amplified by 200, we have 200mV at the input of the ADC module in GreenPAK4. 50% of the maximum charging current is used for charging the battery, and in this case it is 0.5A.

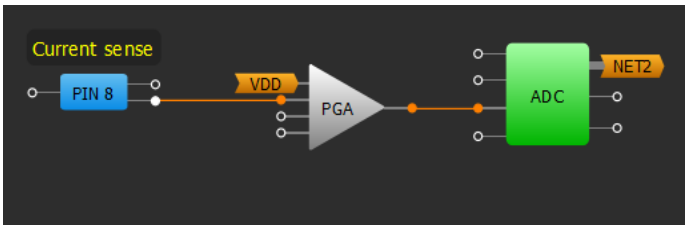

Figure 17. ADC

Output of the current sensing circuit is connected to PIN8, which is connected to the PGA. The PGA is in turn connected to the ADC. Output of the ADC is connected to the digital comparators DCMP0 and DCMP1. Using DCMP0, the LiPo charger maintains constant charging current of 500mA.

Figure 18 depicts the DCMP0 settings. The IN+ selector is ADC output, and the IN- selector is Register 0. In order to have information, if current is above 500mA, the Register 0 is set to 50 using the following calculation:

GreenPAK4 ADC is 8 bit, so resolution is :

$$\frac{Vref}{2^n} = \frac{1.2\ V}{256} = 4.6875 \frac{mV}{sample}$$

When current through R_sense is 0.5A, voltage on the ADC input is 200mV as explained earlier, so

Register 0 = $\frac{200\ mV}{4.6875\ mV} = 42.66 \approx 43$

If the current through R_sense is above 0.5A, the DCMP0 output will disable the PWM buck output in order to prevent rise of current and will maintain it to a constant. The DCMP0 output is connected to a 3L10 multiplexer input. When in CC mode, if output of DCMP0 is 0 (current bellow 0.5A), the output of the 3L9 multiplexer will be the output of the PWM2 module. In case DCM0 output is 1(current above 0.5A), output of 3L9 will be GND.

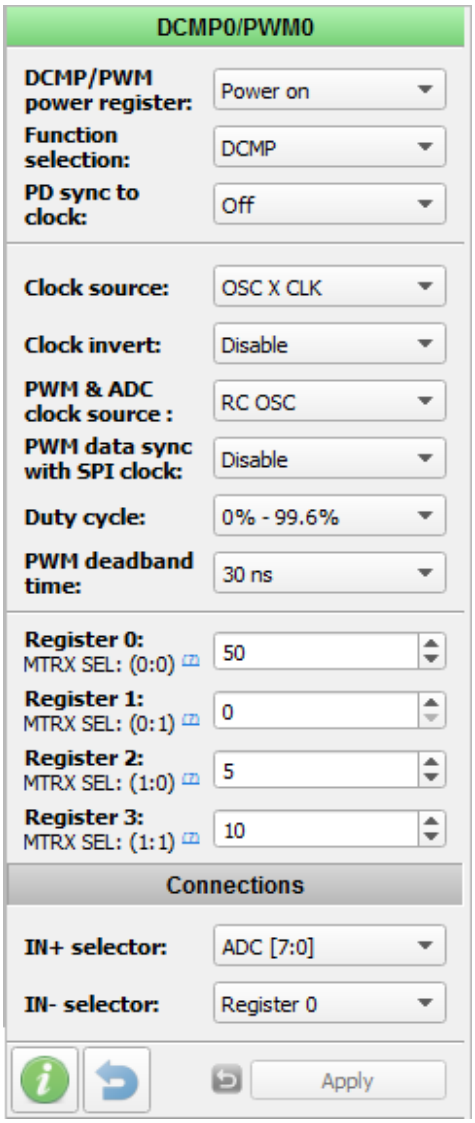

Figure 18. DCMP0 settings

CV mode:

When the CC/CV logic directs to CV mode, output of 3L10 multiplexer will be the output of ACMP3. ACMP3 is supplied with an external voltage divider so that when the voltage on the battery is above 4.2V, it is able to output 1. This will also put an output of 3L9 to GND and turn the buck output off. In the battery voltage is below 4.2V, the ACMP3 will output 0 so that the 3L9 output is the PWM signal, generated by PWM2 module. This method is used to keep the voltage constantly 4.2V on the battery.

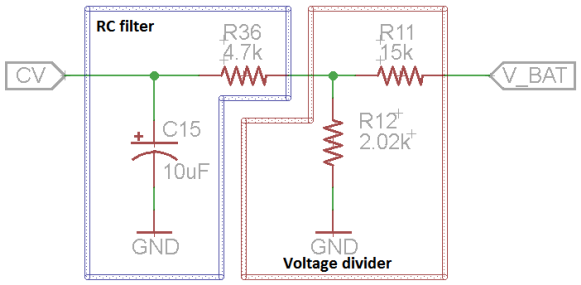

Figure 19. Analogue frontend for ACMP3

Figure 19 depicts the analog frontend for ACMP3 (voltage divider set to output 500mV when voltage on the battery is 4.2V and the RC filter to reduce noise).

Battery charging termination:

The DCMP1 is used to detect the battery charging termination. When the charger is in CV mode and the current is 10% of maximum charging current (0.1A), charging will be terminated. Register 2 is compared with the value generated by the ADC using the digital comparator DCMP1. The value in Register 2 is calculated as follows:

$V_{R\_sense} = 0.1\ A * 0.002\ Ohm = 0.0002\ V = 0.2\ mV$

$V_{out} = G * V_{R\_sense} = 40\ mV$

Figure 20. Over temperature protection

$$\frac{Vref}{2^n} = \frac{1.2\ V}{256} = 4.6875 \frac{mV}{sample}$$

Register 2 =

$$\frac{40\ mV}{4.6875\ mV} = 8.5333 \approx 9$$

Over-temperature protection

Figure 20 depicts the circuitry used for over-temperature protection. A 10KOhm NTC resistor with a constant B=4050K is used for temperature monitoring. If the temperature is above 50C, the ACMP1 will terminate battery charging.

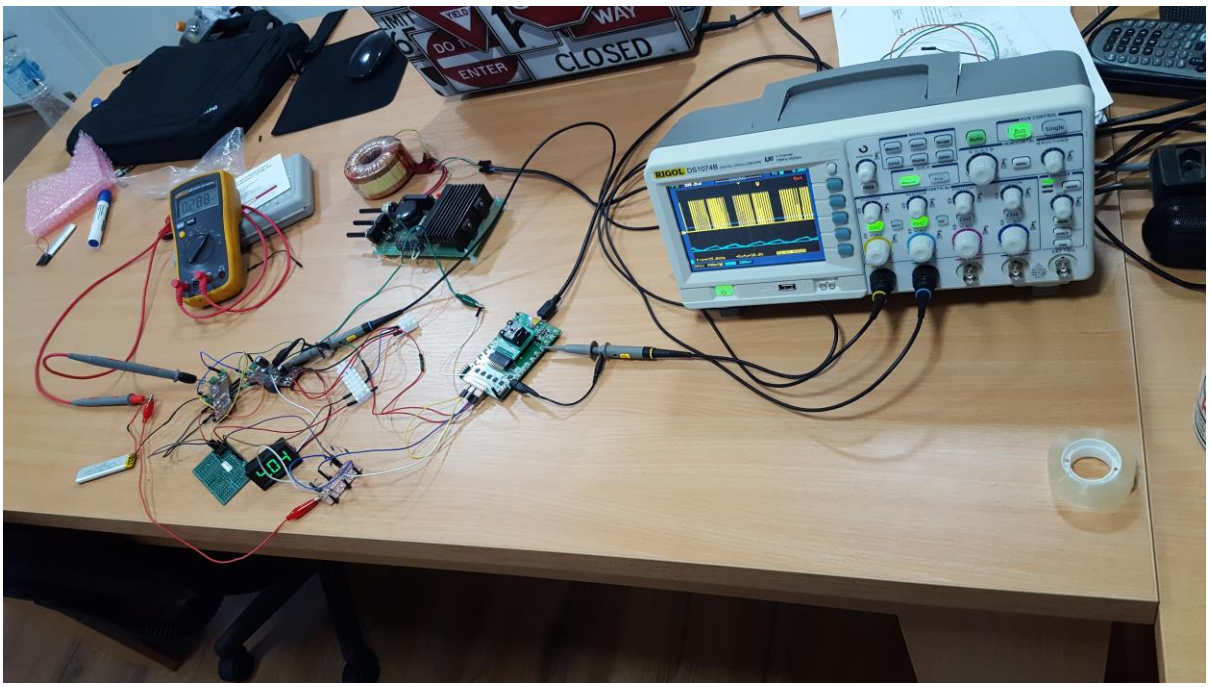

Figure 21. LiPo charger testing

Figure 21 shows the LiPo charger implementation testing. Voltage on the battery is 4.04V; which means it is in CC mode. In this phase of development, 290mA charging current was used in CC mode.

Boost DC-DC converter design and implementation

A boost DC-DC converter is used to step power bank 3.7-4.2V voltage up to 5V required by the smartphone. Boost parameters are as follows:

- n = 0.85, for calculations 0.85 efficiency is used
- ΔV_{out}=50mV, output voltage ripple
- Vin(min) = 3.3V, this is minimal input in boost
- Vin(max = 4.2V, this is maximum input in boost
- fs = 41.7kHz, this is switching frequency
- Vout = 4.9-5.2V
- $D = 1 - \frac{Vin(\min)*n}{Vout} = 50\%$, duty cycle

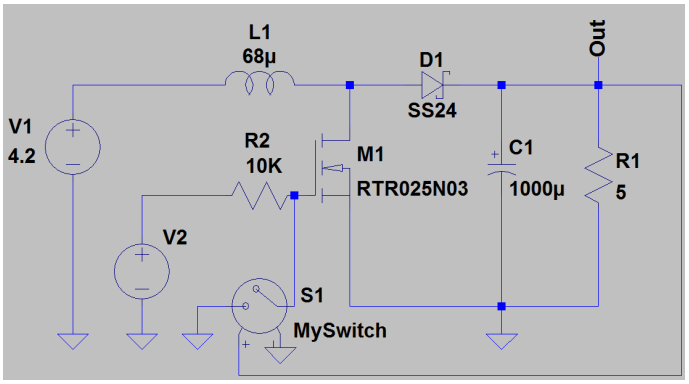

Figure 22. Boost DC-DC converter schematics

- $IL = (0.2 \text{ to } 0.4) * \text{Iout(max)} * \frac{Vout}{Vin}$ = 0.496 A, inductor ripple current
- $L = \frac{Vin*(Vout-Vin)}{IL*fs*Vout}$ = 62.5uH, inductor
- $Isw(max) = \frac{IL}{2} + \frac{Iout(max)}{1-D} = 2.56A$, max output current
- $Cout(min) = \frac{Iout(max)*D}{fs*\Delta Vout} = 311uF$

Figure 22 depicts the analog boost implementation, simulated using LT Spice.

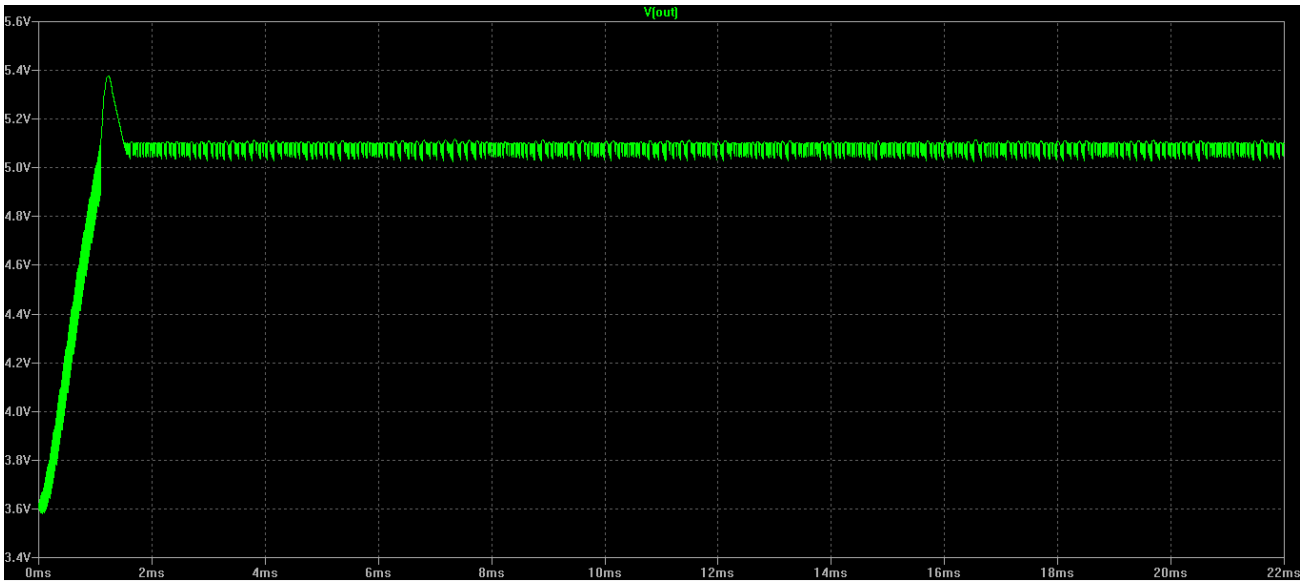

Figure 23. Simulation results for Boost converter implementation

The results of the simulation are shown in Figure 23. Boost is implemented using the OSC as a PWM source (with 41.7kHz frequency).

Figure 24 depicts the boost implementation using the GreenPAK4. PWM is generated using the OSC with the clock predivider set to 2 and the OUT0 second divider set to 24 (in order to achieve the 41.7kHz frequency). Comparator ACMP5 is used to compare feedback with the set voltage threshold. When voltage on the feedback pin is above the set threshold, the PWM source is turned off. This is a simple way of controlling the output voltage on the boost converter.

Figure 25 shows the results of the implemented boost converter. The results are as expected, when compared with simulation results. Figure 26 depicts the boost design test charging a Bluetooth speaker with an internal LiPo battery.

Figure 25. Boost implementation results

Extensions of this design

This example covered all the logic, clock generation and feedback provided by sensors to the power management controller for the LiPo battery.

This design can be expanded in the analog domain by simply using additional voltage protection circuitry. Regarding the implementation on the digital side, the design presented here already implemented all the major requirements.

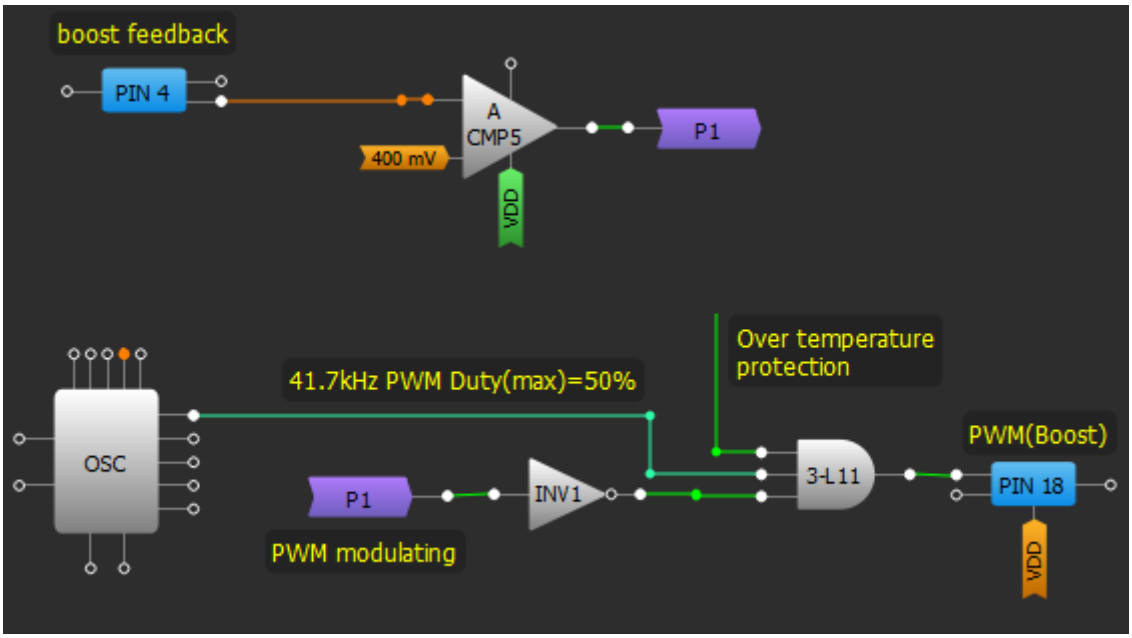

Figure 24. GreenPAK4 Boost implementation

Figure 26. Boost implementation test charging Bluetooth speaker

Conclusion

The proposed design and implementation shows that the power management controller and the LiPo charger (including the buck and boost DC-DC converters) can easily be implemented using a GreenPAK4. Using a GreenPAK4 allows us to get the desired behavior of the system without having to invest in custom silicon development. This shows that similar products can be designed and tailored to a designers needs by using the GreenPAK technology.

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