Hitless Protection Switching (HPS) Without Relays

82P28xx, 82P2521 Application Note AN-522

1 INTRODUCTION

This application note covers Hitless Protection Switching (HPS) applications without relays for IDT's High-Density LIU. The High-Density LIU family includes the following devices:

- IDT82P2828: 28(+1) channel T1/E1/J1 Short Haul LIU
- IDT82P2821: 21(+1) channel T1/E1/J1 Short Haul LIU
- IDT82P2521: 21(+1) channel E1 Short Haul LIU
- IDT82P2816: 16(+1) channel T1/E1/J1 Short Haul LIU
- IDT82P2808: 8(+1) channel T1/E1/J1 Short Haul LIU

In today's telecommunication systems, ensuring no traffic loss is becoming increasingly important. More and more, people are relying on Internet to conduct financial transactions, make telephone calls and perform video conferencing. Loss of data could have a devastating effect including the loss or delay of a critical financial transaction, hearing annoying flickering noises on the telephone lines, or viewing distorted video clips.

To address these problems, redundancy protection must be built into the systems carrying this traffic. Although there are many types of redundancy protection schemes, This application note only deals with 1+1 and 1:1 hardware protection schemes based on IDT's High-Density LIU family.

Special care has been taken in the design for the High-Density LIU family to support these protection schemes and provision for power failure on the primary or backup card, and - while carrying live traffic - support fast switching between primary and backup card and hot insertion of a backup card.

In summary, IDT's High-Density LIUs provide the following advanced features:

- optimized high impedance options
  - High Impedance during Power Off (Power Failure)
  - Asynchronous hardware control (OE, RIM) for fast global high impedance of receiver and transmitter (hot switching between working and backup board)
  - Per-channel register control for high impedance, independent for receiver and transmitter
  - Provides transmit driver over-current detection and protection with optional automatic high impedance of transmit interface
- fully integrated receive termination to support
  - 1+1: Primary and Redundant card use shared I/O card and common termination
  - 1:1: Primary and Redundant card independent termination, Y-Cable

2 HPS APPLICATION SCHEMES

The High-Density LIU provides both Differential and Single Ended interfaces for receive and transmit. HPS support is provided for both termination options. The design of HPS scheme is flexible and varied. Following is an outline of the supported protection schemes.

T1/E1/J1 1+1 and 1:1 relay-less Hitless Protection Switch (HPS) is a means to provide 100% linear redundancy for T1/E1/J1 applications.

In the 1+1 redundancy scheme, there are two identical cards: a primary and secondary or protection card. The primary card is active and the secondary card is always in hot standby. They share the same line interface which is usually located on a shared I/O card.

The 1:1 redundancy scheme is very similar to the 1+1 scheme. There is also a primary and a protection card, however each card contains its own transformer and protection circuitry. This scheme is typically used when the redundancy is based on a system level or for pizza-box designs that do not provide space for a shared I/O panel. For an optimized 1:1 scheme, a fully internal receive termination option of the LIU (no external resistors) is required.

If the primary card fails, the traffic is switched to the secondary card. In the older generation of T1/E1/J1 line cards, the primary and secondary cards share the same line by use of multiple mechanical relays. When the primary card fails, the switching from the primary to the secondary card relies on mechanical relays. Mechanical relays are not only costly but have a lot of drawbacks as well. First, the relays require drivers to switch them. This implies bigger bill of materials and results in higher system cost as well as potentially more reliability issues from the relays and drivers. Secondly, the relays are big and take up a lot of room on the PCB. Depending on the types of relay, each could take up to an area of 10 mm^2. As traffic volume grows, more channels or line cards are required to handle heavier traffic load. The mechanical relays result in bigger and more costly boxes. Finally, mechanical relays have higher switching latency. Depending on the relays, it could take up to tens of milliseconds to switch the relays. During this time, there are enough bit errors to jeopardize mission-critical traffic.

In the relay-less hitless protection switching T1/E1/J1 line cards, switching traffic from the primary to backup card is accomplished by the monolithic LIU. Relays are eliminated from the system resulting in a fewer components, higher reliability, better performance and cost effective system. The IDT82P2828/2821/2521/2816/2808 T1/E1/J1 Short Haul LIU is the latest T1/E1/J1 silicon from IDT to enable low latency relay-less redundancy applications.

2.1 IDT HIGH-DENSITY LIU HPS SUPPORT FEATURES OVERVIEW

The IDT High-Density LIU products have various features for optimized hitless protection switching support which include fast high impedance output line drivers, arbitrary waveform generator at the transmit output, and internal /external line impedance matching capabilities.

The transmit high impedance driver enables 1+1 and 1:1 redundancy applications without extra mechanical relays and still achieves excellent analog performance. In the transmit path, the impedance for all channels is controlled by the OE pin.

Likewise, all the receiver inputs are set in high-impedance by controlling the RIM pin. This enables a parallel connection with the backup receiver input without affecting the receive traffic.

There may be a variance between the time the TTIP/TRING and RTIP/RRING are set into high impedance and TTIP/TRING and RTIP/RRING are enabled.

For TTIP/TRING the delay from falling edge of OE until TTIP/TRING pins enter high impedance is about 40 ns, while the delay from rising edge of OE until TTIP/TRING are enabled is about 200 ns. Special care should be taken to minimize the overlap between the primary and secondary cards during protection switching.

For the RTIP/RRING the delay from the falling edge of RIM until RTIP/RRING enter high impedance is less than 40 ns, while the delay from the rising edge of RIM control level until RTIP/RRING enter internal impedance (low impedance) is about 0.4-6 us. During switchover, the amplitude of receive signal may increase (both receivers are in high impedance state), however this should not have any affect on the receive performance of the High-Density LIU.

2.2 1+1 HPS SCHEME

Section 2.2.1 and 2.2.2 illustrates the implementation of the IDT High-Density LIU Differential and Single Ended interface for a 1+1 relayless hitless protection switching scheme. It shows a typical multi-service chassis populated with T1/E1/J1 line cards. There are 2 x N line cards, control card, backplane and I/O card as detailed as follows:

- 1st to Nth active cards. These are T1/E1/J1 primary cards populated with one or multiple IDT High-Density LIUs
- 1st to Nth protection cards. These are T1/E1/J1 secondary cards populated with one or multiple IDT High-Density LIUs and are in hot standby. Each line card has a backup line card and connects to the same traces to the backplane
- interface cards. These cards consist of transformer and metallic line protection devices, plugged into the backplane and are shared among the primary and secondary cards.

2.2.1 1+1 HPS SCHEME, DIFFERENTIAL INTERFACE (SHARED COMMON TRANSFORMER)

Figure-1 shows 1+1 HPS scheme for Differential interface (shared common transformer. The impedance matching setting is as follows:

- LIU receive configuration: Fully Internal Impedance Matching, no external termination resistor
- LIU transmit configuration: Internal Impedance Matching

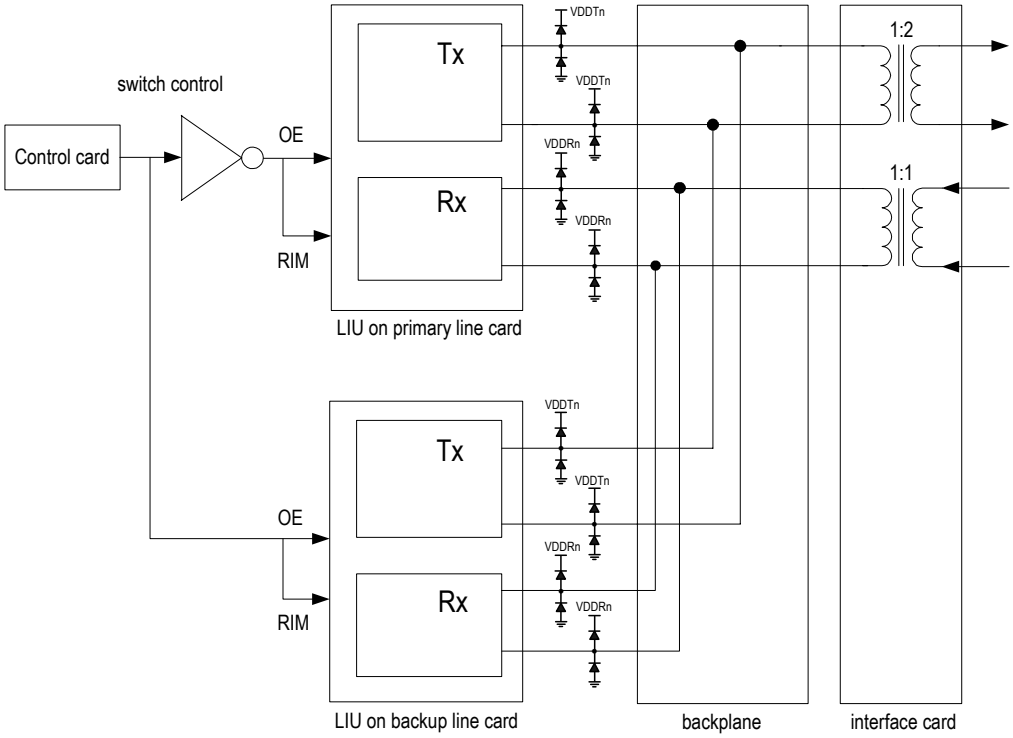

Figure-1 1+1 HPS Scheme, Differential Interface (Shared Common Transformer)

2.2.2 1+1 HPS SCHEME, SINGLE ENDED INTERFACE

Figure-2 shows 1+1 HPS scheme for Single Ended interface. The impedance matching setting is as follows:

- LIU receive configuration: 75 Ω External Impedance Matching
- LIU transmit configuration: 75 Ω Internal Impedance Matching

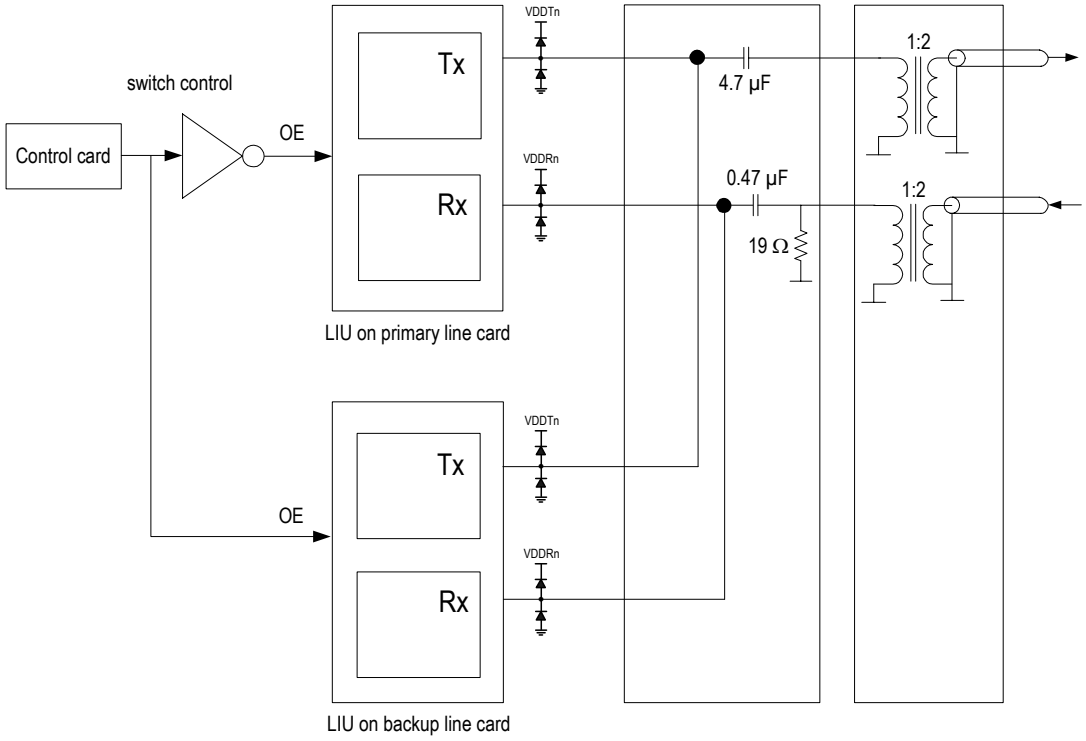

Figure-2 1+1 HPS Scheme, Single Ended Interface

2.3 1:1 HPS SCHEME

Figure-3 illustrates the implementation of the IDT High-Density LIU Differential interface for a 1:1 relay-less hitless protection switching. It shows a typical multi-system implementation or pizza-box design, populated with T1/E1/J1 line cards. There are usually two line cards as detailed in the following:

- one active cards - This is a T1/E1/J1 primary card populated with one or multiple IDT High-Density LIUs, transformers and metallic protection devices
- one protection card - This is a T1/E1/J1 secondary card populated with one or multiple IDT High-Density LIUs, transformers and metallic protection devices. This card is in hot standby.

The impedance matching setting for 1:1 HPS scheme Differential Interface is as follows:

- LIU receive configuration: full internal impedance matching, no external termination resistor
- LIU transmit configuration: internal impedance matching

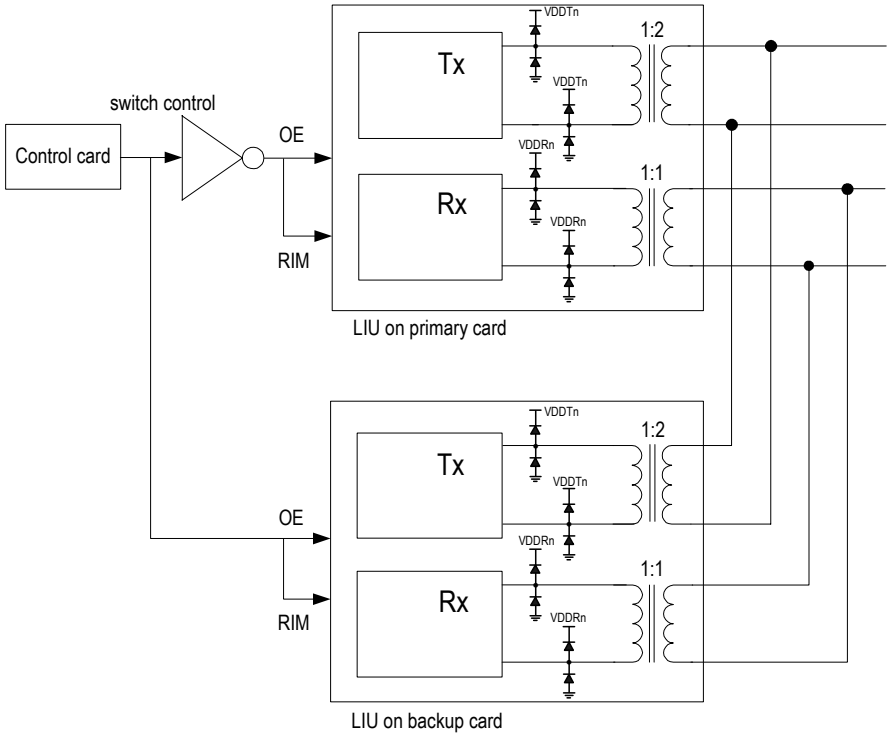

Figure-3 1:1 HPS Scheme, Differential Interface

3 TEST REPORT

3.1 BACKUP CARD POWER FAILURE TEST

During this test, all VDDs of the LIU on the backup board are shorted to GND. The Tx/Rx of the primary board and backup board are configured as follows:

- Primary board Tx: normal communication
- Primary board Rx: normal communication
- Backup board Tx: high impedance during power off (VDD shorted to GND)
- Backup board Rx: high impedance during power off (VDD shorted to GND)

Backup card power failure test is considered the worst case setup for the waveform measurements. The following waveform measurements also apply to section 3.3 Hot Swap Test - Long Term Bit Error Test and 3.4 Hot Switch Test - Long Term Bit Error Test.

3.1.1 WAVEFORM MEASUREMENT OF 1+1 / 1:1 HPS SCHEME FOR E1 120 OHM DIFFERENTIAL INTERFACE

Figure-4 is the setup of waveform measurement of 1+1 HPS scheme for E1 120 Ω Differential interface. The setup also applies to 1:1 scheme.

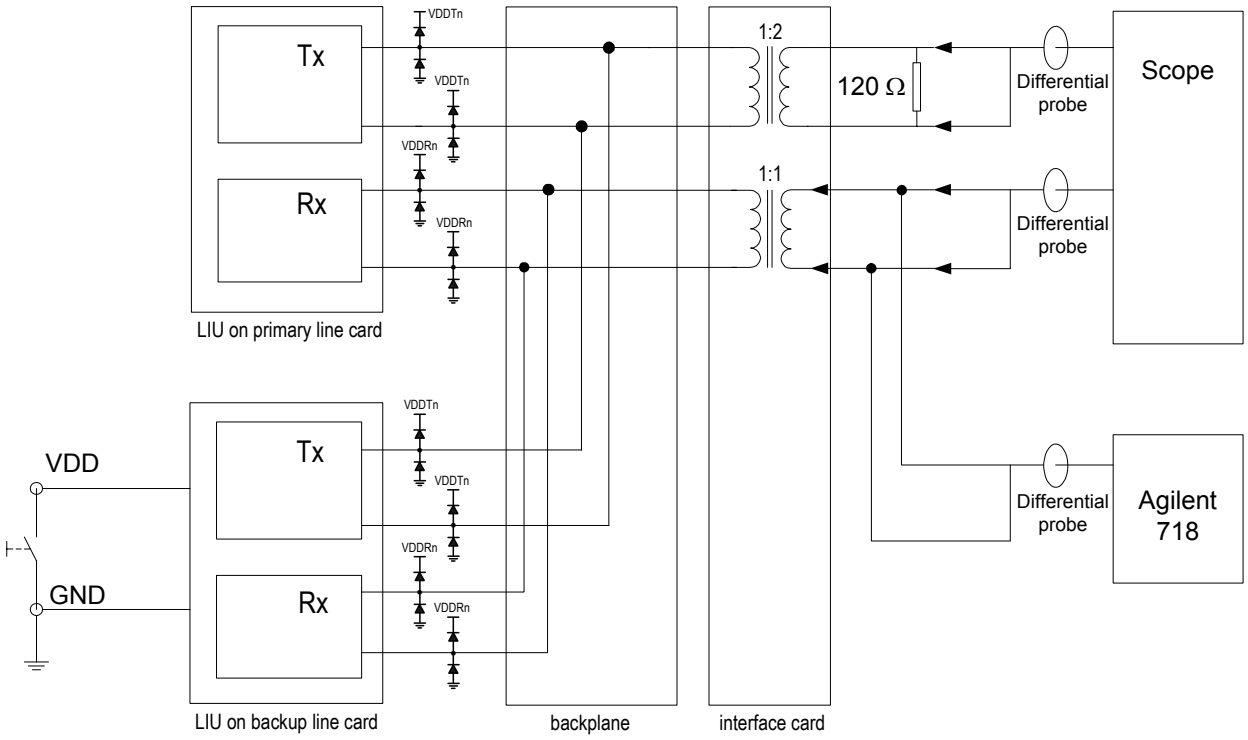

Figure-4 E1 120 Ω Waveform Measurement Setup

Figure-5 shows the E1 120 Ω template test on the 120 Ω resistor at the line transmit side (TTIP/TRING).

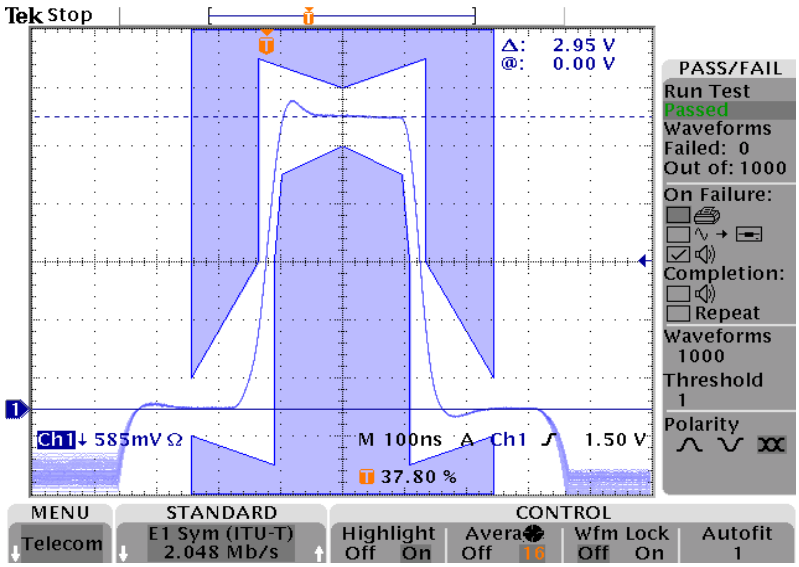

Figure-5 E1 120 Ω Template Measured on Tx Line

3.1.2 WAVEFORM MEASUREMENT OF 1+1 / 1:1 SCHEME FOR DS1 100 OHM DIFFERENTIAL INTERFACE

Figure-6 is the setup of waveform measurement of 1+1 DS1 100 Ω Differential interface. The setup also applies to 1:1 application scheme.

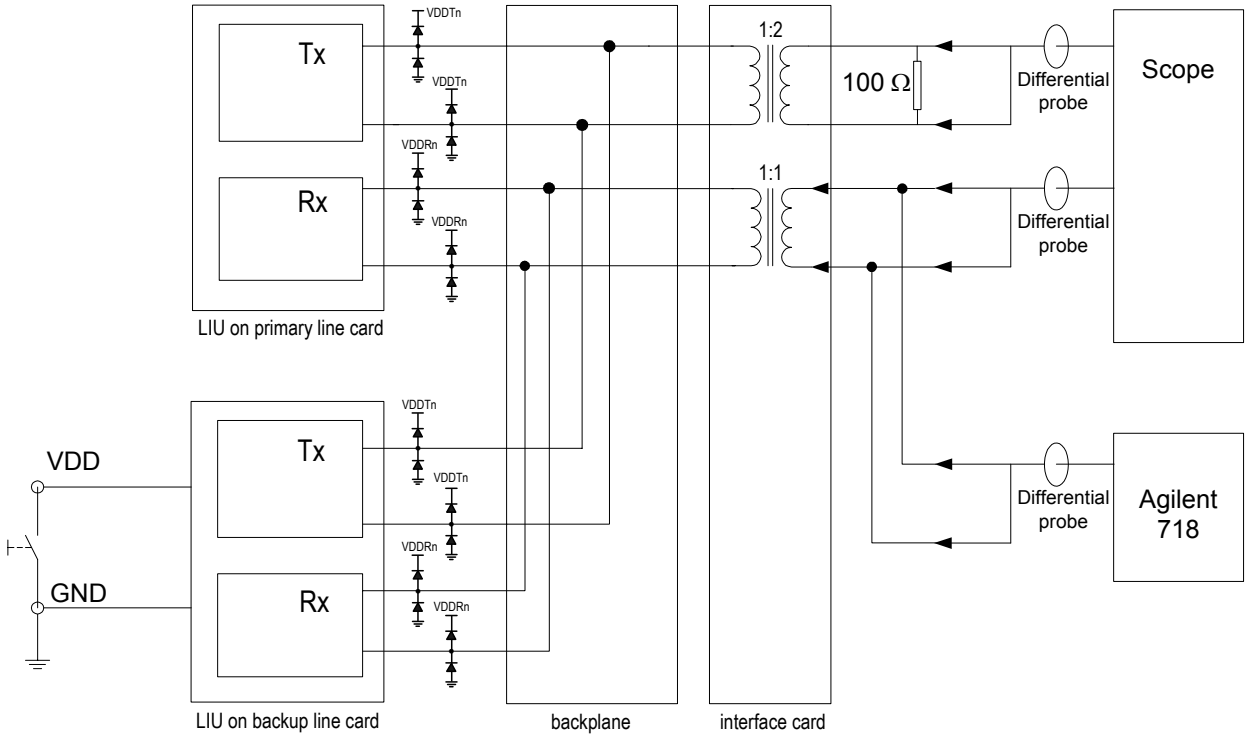

Figure-6 DS1 100 Ω Waveform Measurement Setup

Figure-7 shows the DS1 100 Ω template test on the 100 Ω resistor at the line transmit side (TTIP/TRING)

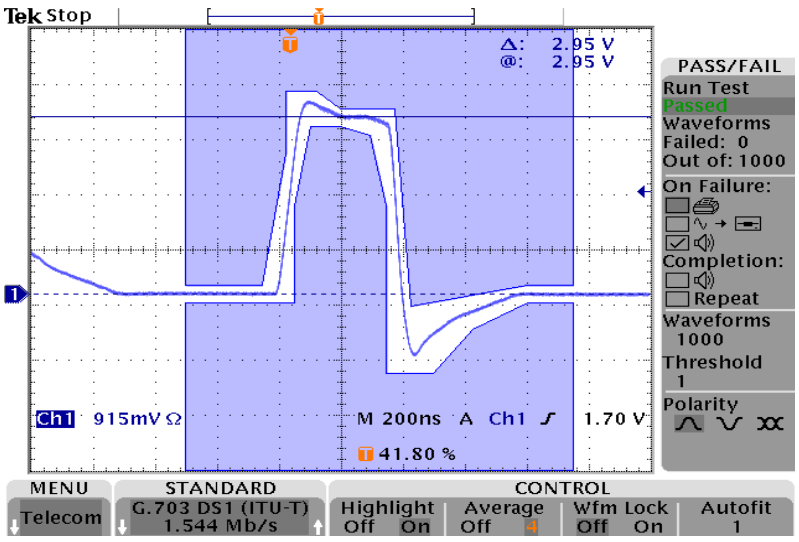

Figure-7 DS1 Template Measured on Tx Line (0~133 ft)

3.1.3 WAVEFORM MEASUREMENT OF 1+1 SCHEME FOR E1 75 OHM SINGLE ENDED INTERFACE

Figure-8 is the setup of waveform measurement of 1+1 scheme for E1 75 Ω Single Ended interface.

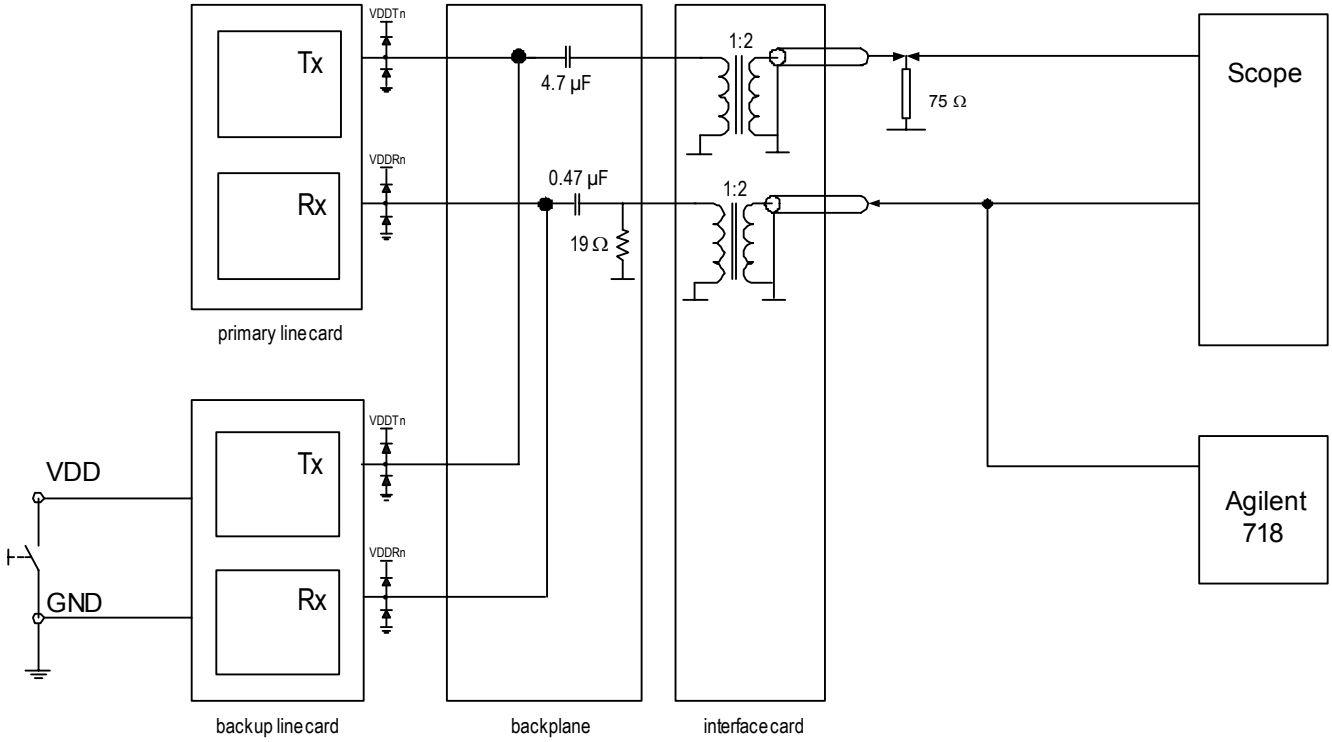

Figure-8 Waveform Measurement Setup

The High-Density LIU provides an User-programmable Arbitrary waveform generator (AWG). The AWG enables the user to customize the transmit template and adjust it to specific application requirements if necessary. Refer to the High-Density LIU datasheet for more information on AWG programming.

For Single Ended termination, in order to improve the waveform, it is recommended to change sample 4 from '0F' to '08', and sample 13 from '00' to '06' as outlined below.

Table-1 Use-programmable Arbitrary Waveform (Scale = 0x33)

SAMP[4:0]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
WDAT[6:0]	00	00	00	08	3C	3C	3C	3C	3C	3C	3C	3C	06	00	00	00	00	00	00	00

Figure-9 shows the E1 75 Ω template test on the 75 Ω resistor at the line transmit side with the adjusted AWG values.

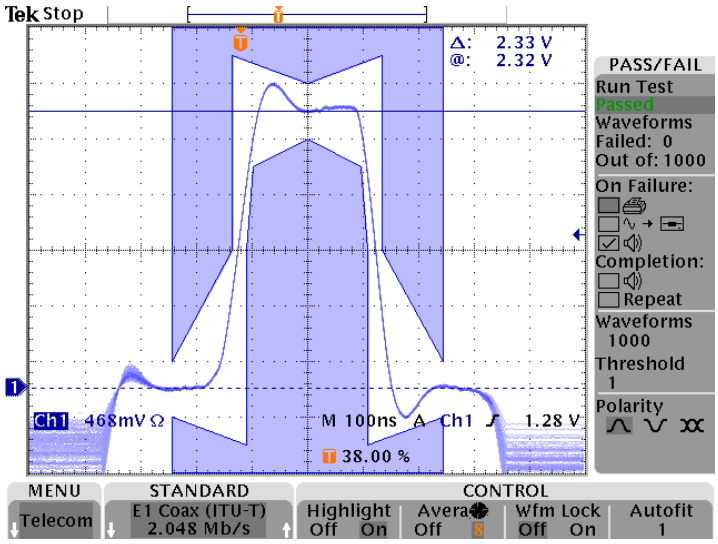

Figure-9 Templates Measured on Tx Line (Scale=0x33)

3.2 LONG TERM BIT ERROR TEST

Test Setup

- -PRBS
- -Primary card transmits live traffic
- -Backup card power tied to ground
- -Test configuration:

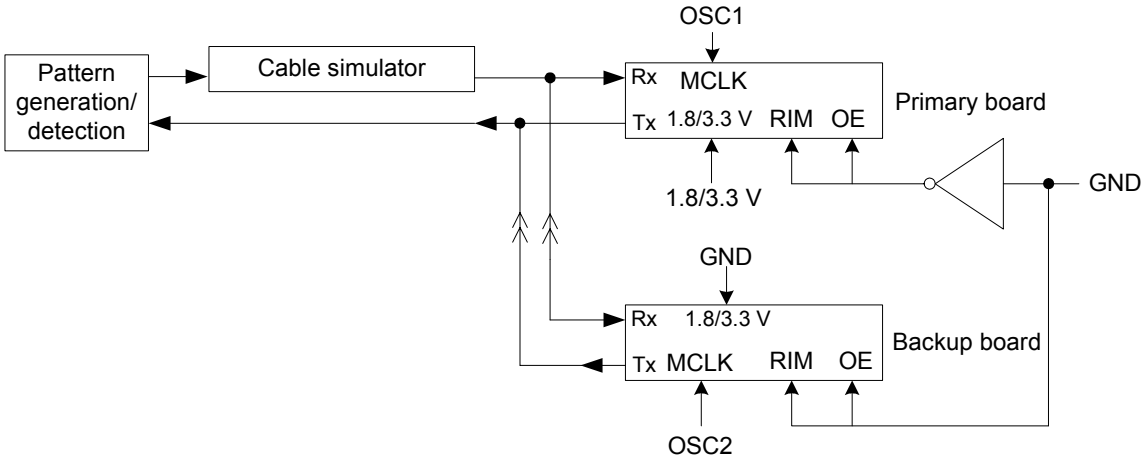

Figure-10 Test Setup

Test Result of Long Term Bit Error Test

- Differential mode (Cable simulator=12 dB): No bit error found for 8 hours
- Single Ended mode (Cable simulator=12 dB): No bit error found for 8 hours

3.3 HOT SWAP TEST - LONG TERM BIT ERROR TEST

Test Setup

- -PRBS
- -Primary card transmits live traffic
- -Backup card power on/off (repeat cycle=1min)
- -Test configuration:

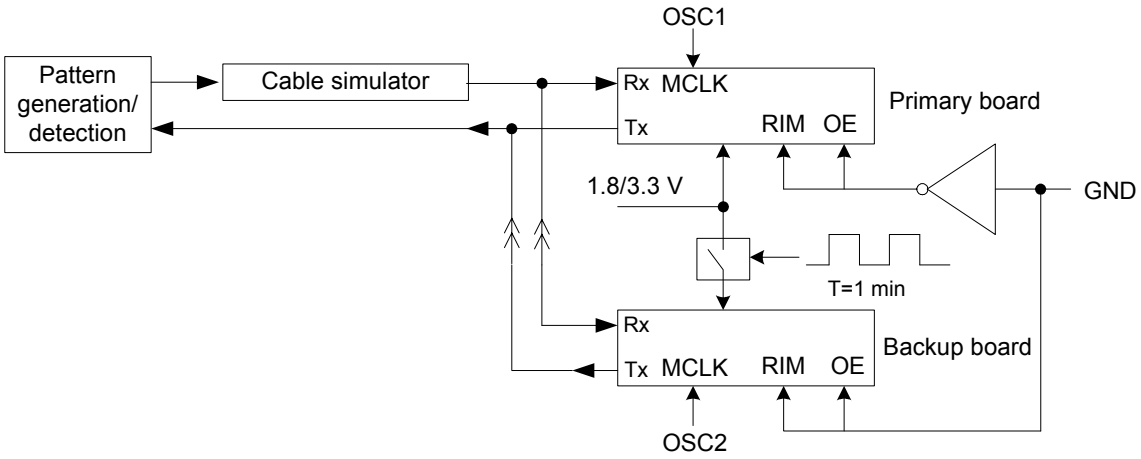

Figure-11 Test Setup

Test Result of Long Term Bit Error Test

- Differential mode (Cable simulator=12 dB): No bit error found for 8 hours
- Single Ended mode (Cable simulator=12 dB): No bit error found for 8 hours

3.4 HOT SWITCH TEST - LONG TERM BIT ERROR TEST

Test Setup

- Differential interface
  - Rx on primary board is configured into full internal impedance matching. Tx on primary board is configured into internal impedance matching
  - Both Rx and Tx on backup board are configured as high-impedance by pin OE and pin RIM. TTIP/TRING is set into High-Impedance state. RTIP/RRING is set into external impedance matching (High-Impedance)
- Single Ended interface
  - Both Rx on primary and backup board are set into external impedance matching (high impedance)
    Tx on primary board is set into internal impedance matching
    Tx on backup board is set into High Impedance
- PRBS/QRSS for E1/T1
- Primary card transmits live traffic
- Switch data between primary and backup card with 1Hz cycle
- Test configuration:

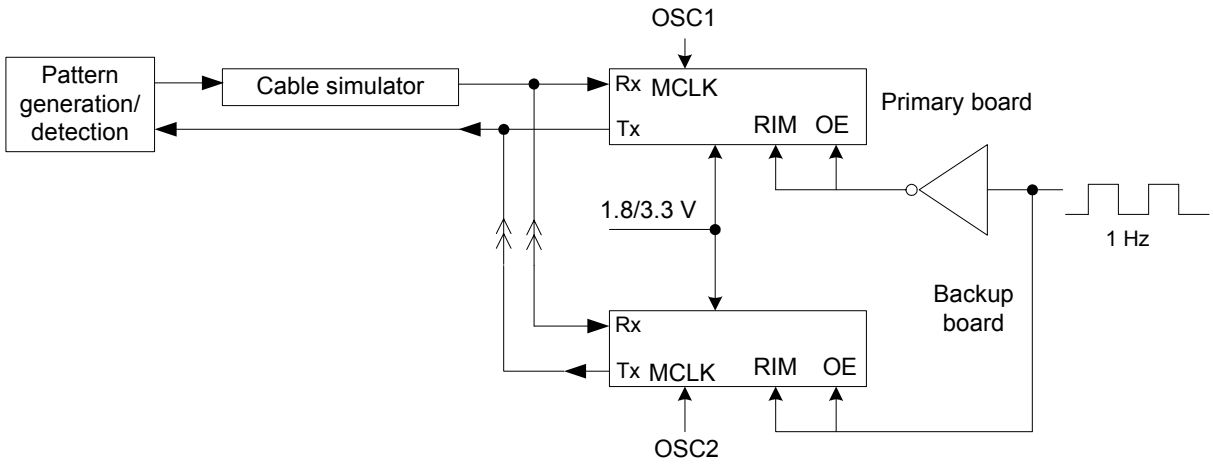

Figure-12 Test Setup

Test Result of Long Term Bit Error Test

Table-2 Test Result

	LOSS of Frame	Bit Error		Note
		Maximum number of errors per switching event	Probability of an error during a switching event	
Differential	0	3	60%	Cable loss=13.4 dB, 4 hour with 2880 times switch
Single Ended	0	3	60%	Cable loss=9.3 dB, 4 hour with 2880 times switch

4 RETURN LOSS TEST RESULT (75/100/120 OHM)

Return Loss Test Setup

The return loss test environment is setup as shown in Figure-13. The calibration must be done before return loss test.

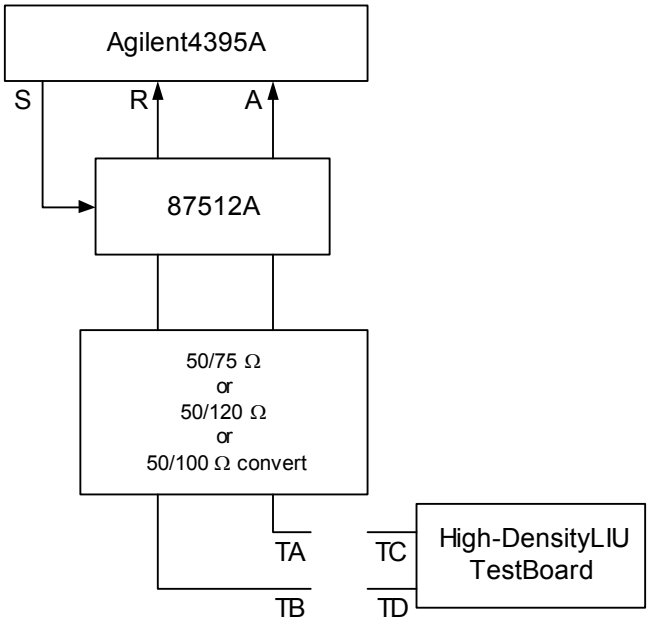

Figure-13 Test Setup

Return Loss Requirement

Table-3 Return Loss Requirement

T1/E1	Frequency Band (KHz)	Transmit Return Loss (dB)	Receive Return Loss (dB)	
			G.703	Italy PTT
E1	20-51		NA	20
	51-102	>8	12	20
	102-2048	>14	18	20
	2048-3072	>10	14	14
T1/J1	39-77	>8	12	20
	77-1544	>14	18	20
	1544-2316	>10	14	14

4.1 RECEIVER RETURN LOSS TEST

Configuration of Receive Line Interface

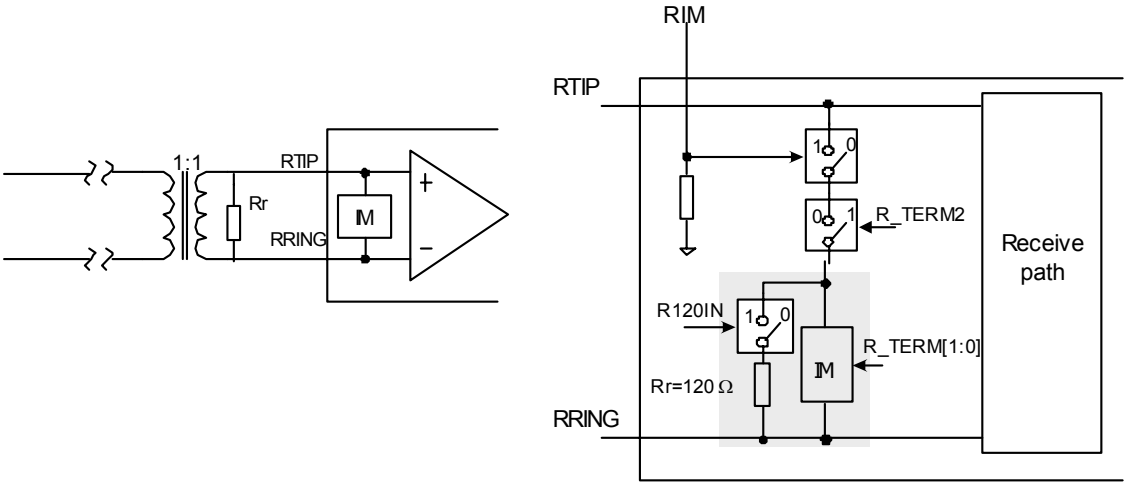

Figure-14 Return Loss Test Setup of the Rx Port

4.2 TRANSMIT RETURN LOSS TEST

Configuration of Transmit Line Interface

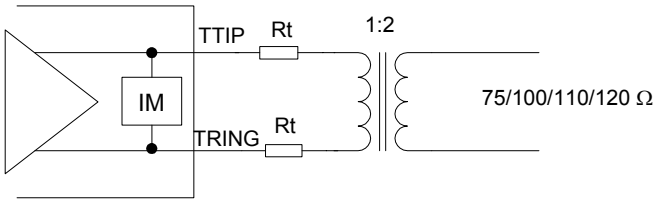

Figure-15 Return Loss Test Setup of the Tx Port

Test Graphics

Figure-16 T1 Receive Return Loss (Partially Internal Impedance Matching)

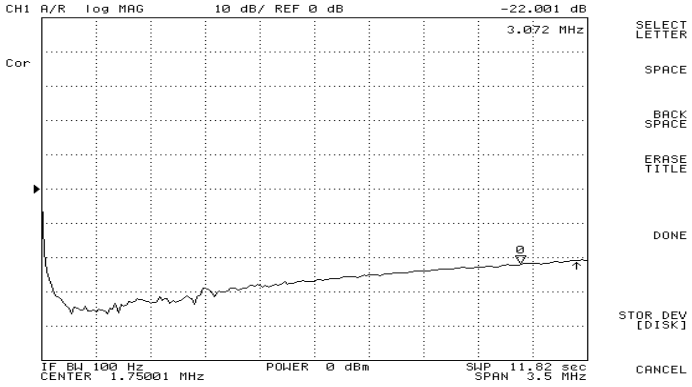

Figure-17 E1 120 Ω Receive Return Loss (Partially Internal Impedance Matching)

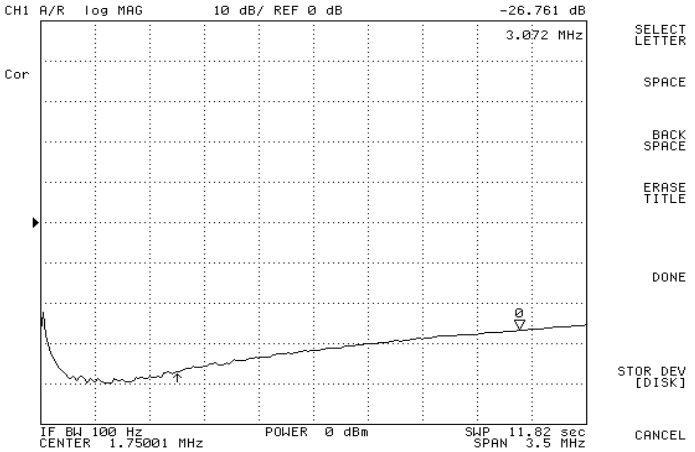

Figure-18 E1 75 Ω Receive Return Loss (Partially Internal Impedance Matching)

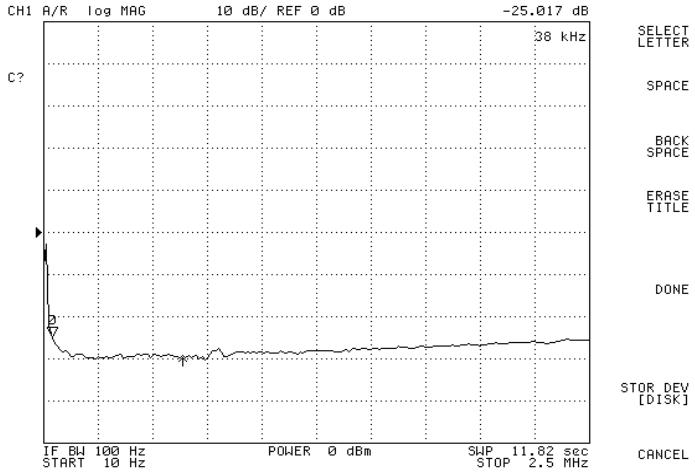

Figure-19 T1 Receive Return Loss (Fully Internal Impedance Matching)

Figure-20 E1 120 Ω Receive Return Loss (Fully Internal Impedance Matching)

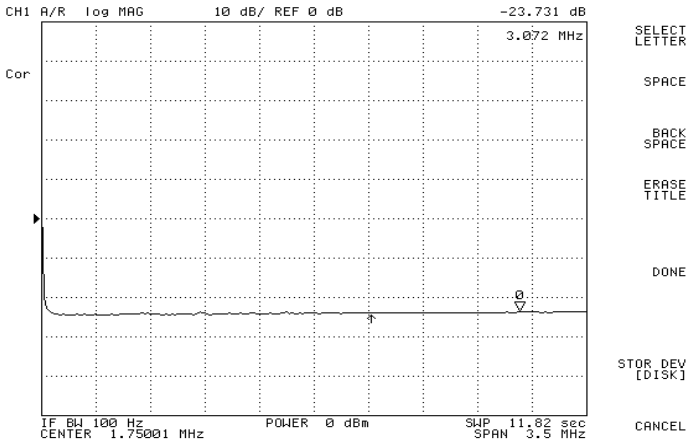

Figure-21 E1 75 Ω Receive Return Loss (Fully Internal Impedance Matching)

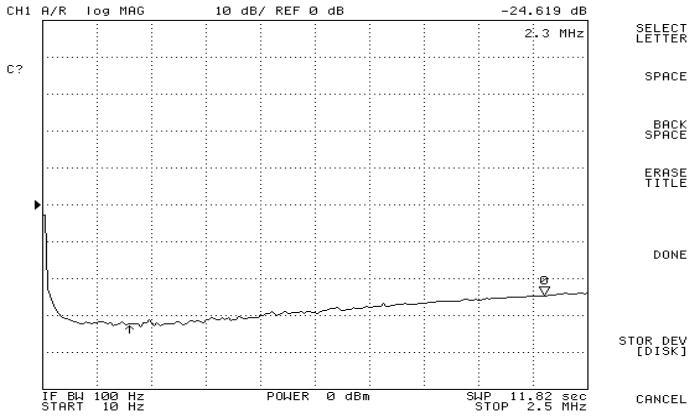

Figure-22 T1 Receive Return Loss (External Impedance Matching)

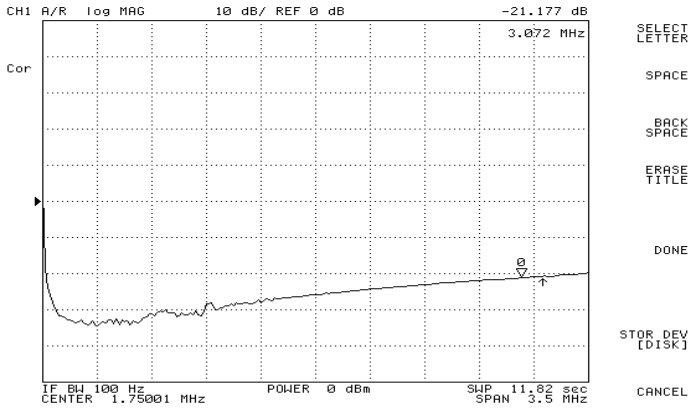

Figure-23 E1 120 Ω Receive Return Loss (External Impedance Matching)

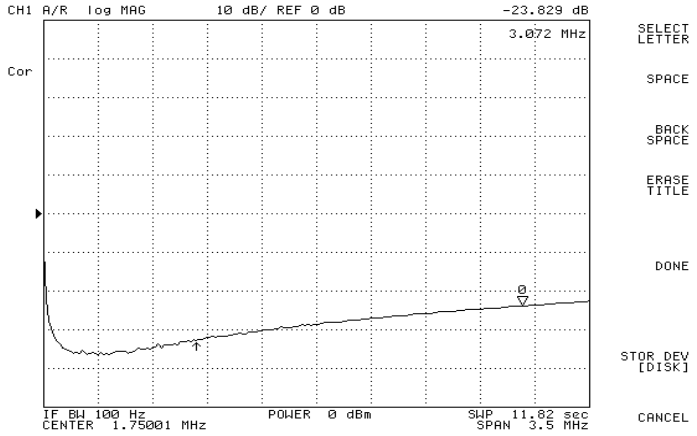

Figure-24 E1 75 Ω Receive Return Loss (External Impedance Matching)

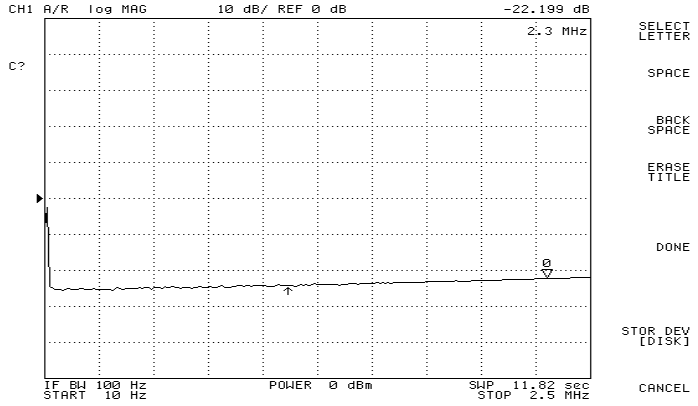

Figure-25 T1 Transmit Return Loss

Figure-26 E1 120 Ω Transmit Return Loss

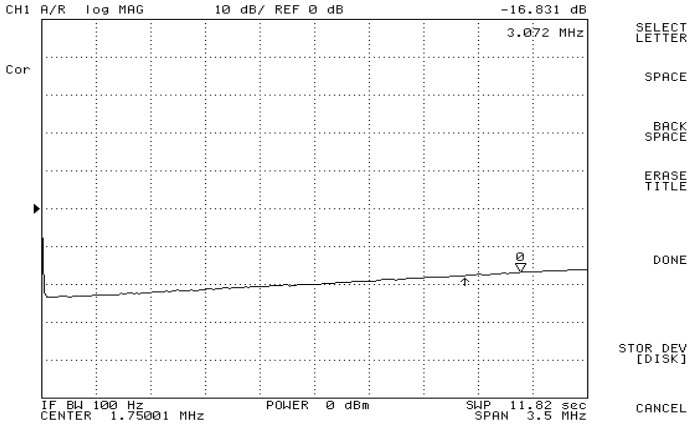

Figure-27 E1 75 Ω Transmit Return Loss

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