Introduction

Cascading PLLs is more common practice than most people think. The majority of clock generators use a crystal in the range 20MHz to 40MHz and then use a PLL to synthesize the desired output clock. The application that receives the clock will synthesize it further up to make Gb/s line rates or GHz processor speeds, for example. Sometimes there is a zero-delay buffer involved as well, causing a cascade of three PLLs.

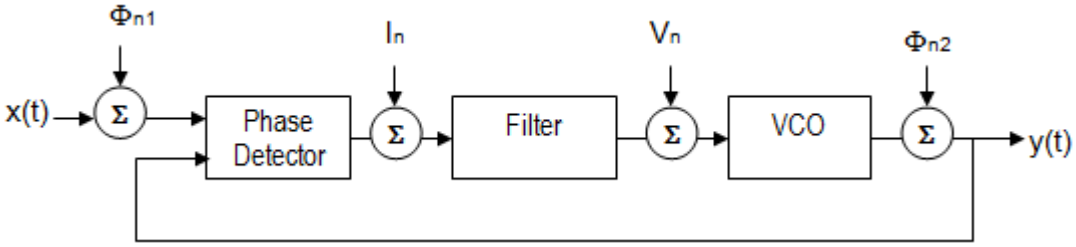
Some literature discourages cascading of PLLs, mostly because jitter peaking adds up when cascading PLLs. This application note shows examples of how jitter peaking accumulates when cascading PLLs and how the accumulation can be limited. It may be easier to adjust PLL properties to allow for cascading than to try and avoid using PLLs altogether.

PLL Theory

A PLL is a feedback system that adjusts the output such that it is phase aligned with the input. Moreover, in the lock condition, the phase difference between the input and output is constant with time. A simple block diagram of the system is shown in Figure 1. Notice the terms: Φ_{n1} – noise from outside the PLL, I_n – noise from the phase detector and filter, V_n – noise on the VCO control voltage, and Φ_{n2} – noise from the VCO. In an ideal PLL, these terms would not exist and the output, y(t), would be jitter free. However, these noise sources do exist and they manifest themselves as jitter on the output. The first critical observation: PLLs generate jitter. The jitter characteristic is a complex function of all the noise sources.

For phase noise entering at x(t) at the input, the PLL behaves as a low-pass filter. The PLL will track and pass low frequency phase noise and will attenuate high frequency phase noise. It will do that with a 2nd or higher order response. A 2nd order response can have a Q factor that creates some amplification near the loop bandwidth before the curve rolls off to the attenuation side.

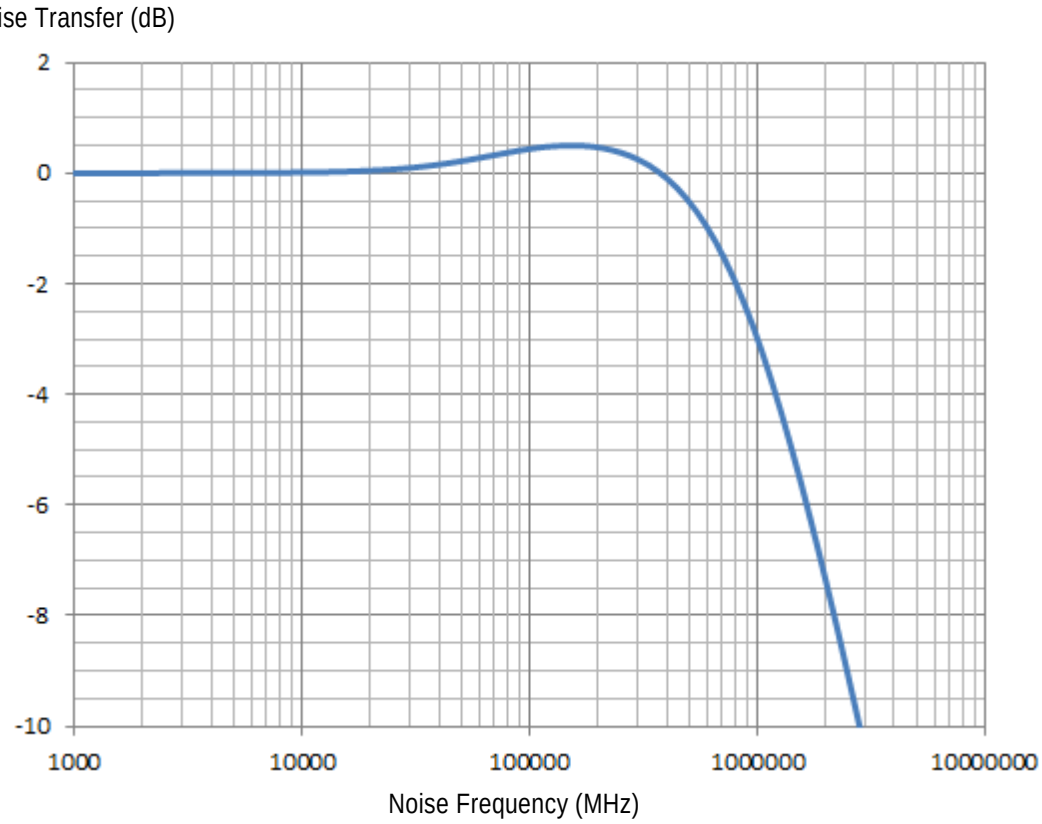
Figure 1. PLL Block Diagram



Jitter Peaking Accumulation

Figure 2 is an example of a PLL noise transfer curve that has a small amount of amplification near the loop bandwidth. This amplification is called jitter peaking. In this example, the jitter peaking is 0.5dB and the loop bandwidth is 1MHz.

Figure 2. Phase Noise Transfer Function with 0.5dB Jitter Peaking



Cascading two PLLs of identical bandwidth with 0.5dB jitter peaking results in a combined jitter peaking of 1dB. Cascading three PLLs of identical bandwidth with 0.5dB jitter peaking results in a combined jitter peaking of 1.5dB. The jitter peaking increases with each added PLL and may increase beyond what the system can tolerate.

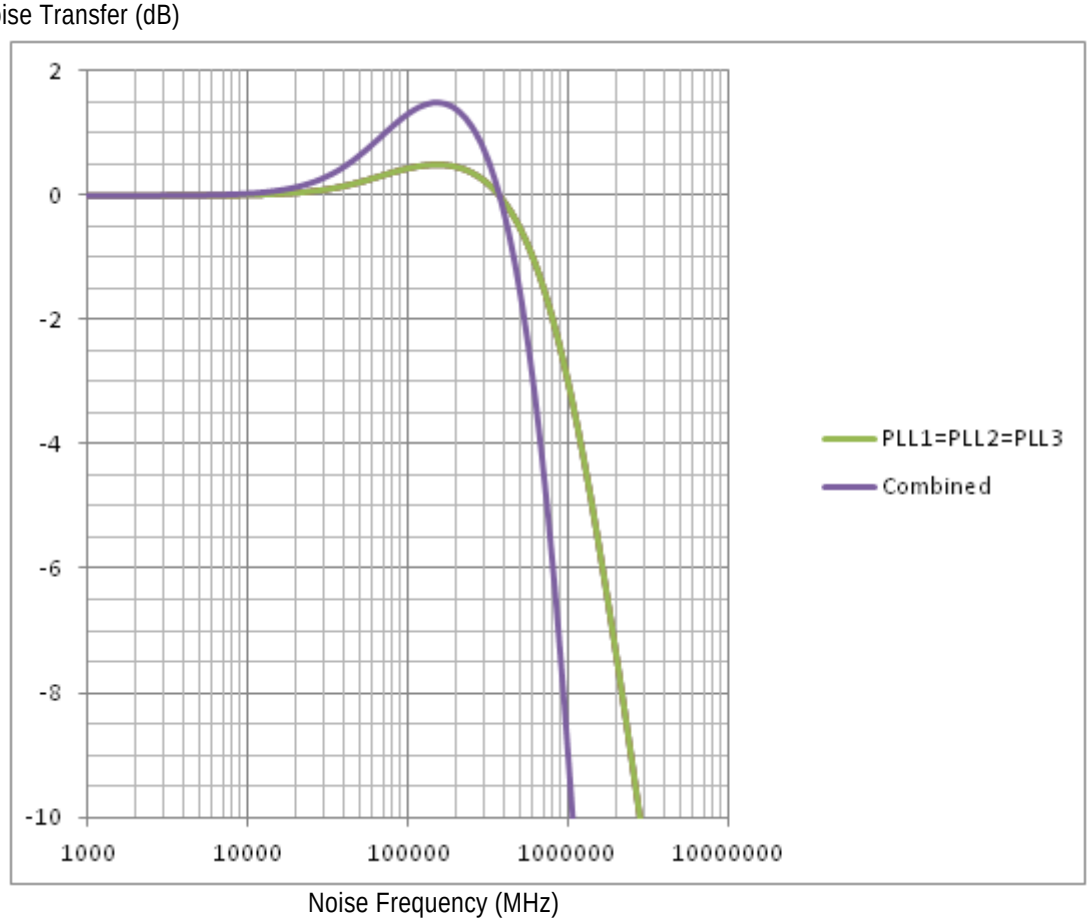
There are two ways to prevent combined jitter peaking from increasing:

1. Design the individual PLLs with very low jitter peaking so the combined jitter peaking when cascading multiple PLLs is still within the system requirement.
2. Use PLLs with different loop bandwidths so the peaking is not accumulating at the same noise frequency. The peaking is distributed over a wider frequency range instead of accumulating in a narrow frequency range.

In practice, a combination of both methods is commonly used to limit jitter peaking in a clock distribution system. A good example of such a clock distribution system is PCI Express®. The clock generator can be a CK420, followed by a DB1900 zero-delay buffer to fan-out the clocks. Both are designed to be used in this fashion, with the CK420 bandwidth set to much less than 1MHz and the DB1900Z bandwidth selectable as either 1MHz or 3MHz. The combination of zero-delay ICs meets the PCI Express system requirements. The PCI Express system requirements are 3dB maximum peaking for generations 1 and 2 and 2dB maximum peaking for generations 3 and 4.

Figure 3 is an example with 3 cascaded PLLs, each with 0.5dB jitter peaking.

Figure 3. Cascading 3 PLLs, each with 0.5dB Jitter Peaking

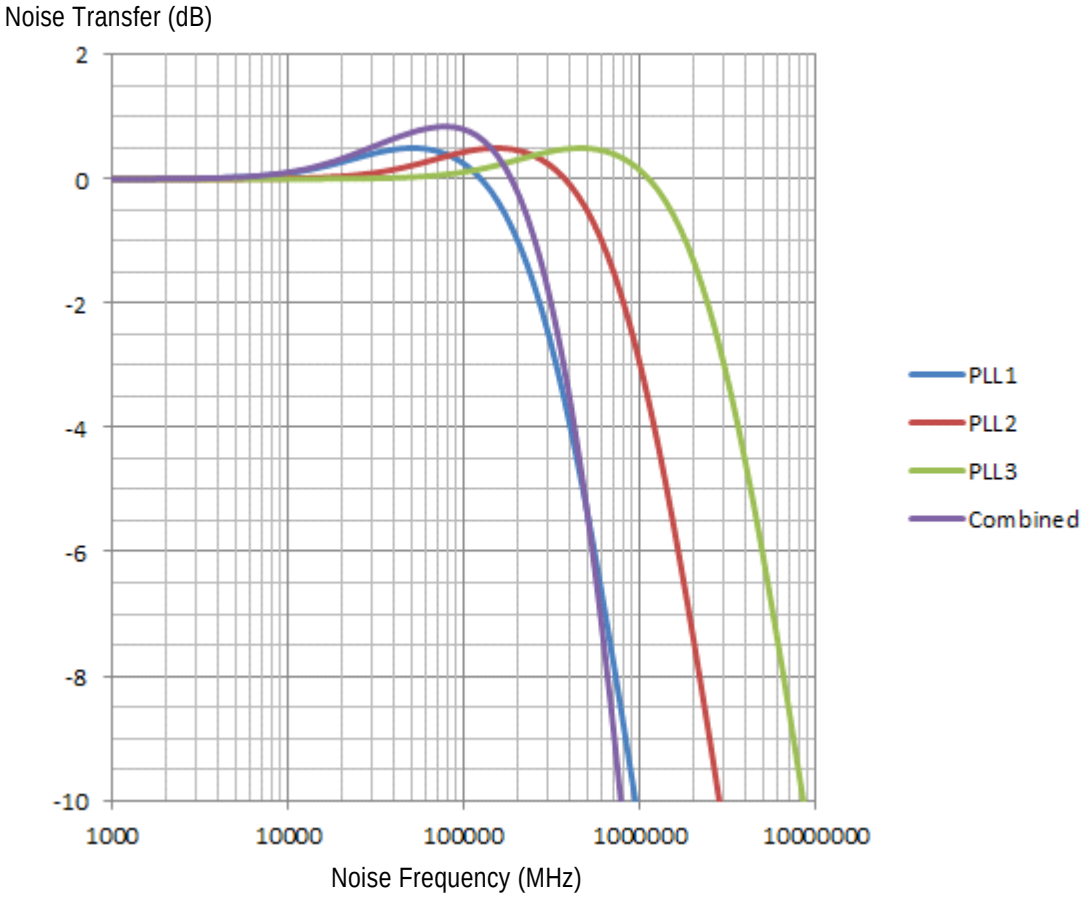


The combined transfer function of these three identical PLLs has 1.5dB peaking and still meets all PCI Express requirements.

Worst case is when the three PLLs have exactly the same loop bandwidth where the combined jitter peaking is the sum of the jitter peaking of each individual PLL. To ensure the acceptable combined jitter peaking is not violated, design the individual PLLs with jitter peaking below half the acceptable value, in the case of cascading two PLLs, and below one third the acceptable value in the case of cascading three PLLs.

Figure 4 is an example with 3 cascaded PLLs, each with 0.5dB jitter peaking. To limit the peaking of the combined noise transfer, the loop bandwidths are set a factor 3 apart.

Figure 4. Cascading 3 PLLs, a Factor 3 Apart, each with 0.5dB Jitter Peaking



The combined transfer function of these three PLLs shows 0.85dB jitter peaking. With three identical loop bandwidths, the jitter peaking grows from 0.5dB to 1.5dB, a 1dB increase. When spreading the loop bandwidths a factor 3 apart, jitter peaking grows from 0.5dB to 0.85dB, a growth of only 0.35dB.

Spreading the loop bandwidths of cascaded PLLs farther apart can further lower the accumulated jitter peaking. If the PLL bandwidths can be separated by a factor of 10, the combined jitter peaking of three PLLs with individual jitter peaking of 0.5dB, can be lowered to 0.53dB, an increase of only 0.03dB.

A useful rule of thumb is this: the closer a single PLL's jitter peaking is to the system limit in a cascade chain, the further apart the loop bandwidths of the cascaded PLLs need to be. With a 1dB system jitter peaking limit, we have shown that a factor of three bandwidth separation is sufficient for a cascade of three PLLs. The jitter peaking due to this PLL configuration is only 0.85dB, well under the 1dB limit.

Table 1. Jitter Peaking versus Loop Bandwidth Ratio Examples

Jitter Peaking (dB)			Loop Bandwidth			Combined Jitter Peaking (dB)
PLL1	PLL2	PLL3	PLL1	PLL2	PLL3	
1.0	1.0	1.0	REF / 1	REF	REF × 1	3.00
			REF / 2	REF	REF × 2	2.07
			REF / 3	REF	REF × 3	1.49
			REF / 5	REF	REF × 5	1.17
			REF / 10	REF	REF × 10	1.04
0.5	0.5	0.5	REF / 1	REF	REF × 1	1.50
			REF / 2	REF	REF × 2	1.15
			REF / 3	REF	REF × 3	0.85
			REF / 5	REF	REF × 5	0.63
			REF / 10	REF	REF × 10	0.53
0.2	0.2	0.2	REF / 1	REF	REF × 1	0.60
			REF / 2	REF	REF × 2	0.51
			REF / 3	REF	REF × 3	0.39
			REF / 5	REF	REF × 5	0.29
			REF / 10	REF	REF × 10	0.22
0.5	0.5	0.5	REF / 10	REF	REF × 2	0.54
0.5	0.5	0.5	REF / 2	REF	REF × 10	0.92
0.5	0.5	N/A	REF	REF × 1	N/A	1.00
			REF	REF × 2	N/A	0.90
			REF	REF × 3	N/A	0.78
			REF	REF × 5	N/A	0.62
			REF	REF × 10	N/A	0.53

The absolute value of the loop bandwidth is irrelevant, so the table above is set up with loop bandwidth ratios. It calls PLL2 the reference and shows the ratio of PLL1 and PLL3 versus the PLL2 loop bandwidth. The last rows are for two PLLs, and PLL1 is used as the reference. The two rows with unequal loop bandwidth ratios for PLL1–2 and PLL2–3 shows how the PLL1–2 ratio is more important than the PLL2–3 ratio. This can also be observed in Figure 4 where the combined jitter transfer plot follows most closely the PLL1 jitter transfer plot. The PLL2 loop bandwidth is the closest to PLL1 and has the largest influence on the combined plot. PLL3 has the largest ratio versus PLL1 and affects the combined plot the least.

Conclusion

These examples show how to control jitter peaking when cascading PLLs. In practice, a combination of minimizing jitter peaking, and separating loop bandwidths is used. Table 1 shows the results of cascading PLLs with various jitter peaking and bandwidth values.

IDT provides clock generators and zero-delay buffers for PCI Express clock trees. The devices are designed such that cascading the clock generator's PLL, the zero-delay buffer's PLL and the PCIe chipset PLL works without excessive jitter peaking and stays well within the PCI Express requirements. Other markets may have different jitter peaking requirements than PCI Express, but the principles shown in this application note are still applicable.

Revision History

Table 2. Revision History

Revision Date	Description of Change
July 21, 2017	Numerous text updates and changes on pages 2, 4 and 6.
June 30, 2017	Initial release.

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