

Introduction

The SPICE model for the ISL705XRH and ISL706xRH rad hard supervisory circuits were developed to help system designers evaluate the operation of this IC prior or in conjunction with proto-typing a system design. This model accurately simulates typical performance characteristics at room temperature (+25 °C) such as steady state switching, input voltage and output current transients. Behaviors not supported are temperature analysis, process variation, and AC analysis. Functionality has been tested on ORCAD 10.0 and CADENCE ORCAD 16.3. Other SPICE simulators may be used however the model may require translation.

Reference Documents

- ISL705ARH, ISL705BRH, ISL705CRH, ISL706ARH, ISL706BRH, ISL706CRH Datasheet, [FN7662](#)
- ISL705RH Voltage Supervisory Circuit Evaluation Board User's Guide, [AN1650](#)
- ISL706RH Voltage Supervisory Circuit Evaluation Board User's Guide, [AN1671](#)

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Project Files

The zip file: **ISL705xRH_ISL706xRH SPICE FILES.zip** contains the project file ISL705ARH.opj to be used in ORCAD simulator. The project file contains two schematics which correlate with the ISL705XRH and ISL706XRH evaluation boards (see Figures 8 and 9). For details on the application schematic refer to the evaluation board user's guide [AN1650](#) and [AN1671](#). Each schematic has been set up with a time domain simulation profile for quick evaluation of the model. The schematic pages may be accessed through the main directory window in ORCAD (see Figure 1).

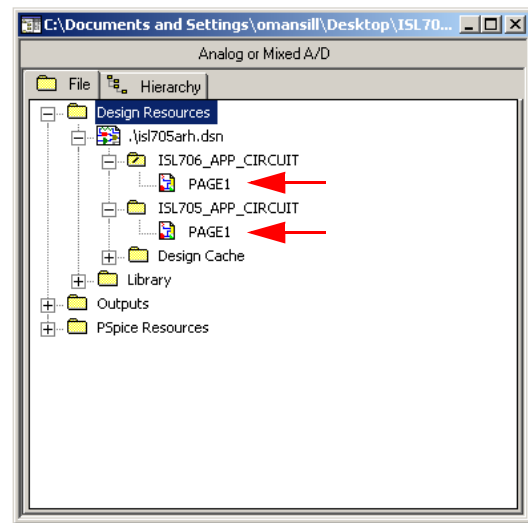


FIGURE 1. APPLICATION SCHEMATIC LOCATION

Figures 2 through 7 show simulation results of the RESET and PFI transient response. These can be compared to Figure 8 through 13 of the datasheet for model accuracy.

Model Parameter List

The model has been developed with a single netlist with multiple variables that are automatically modified to meet IC parameters when the part is placed in an ORCAD schematic from the model library. If the user would like to import the netlist to another SPICE simulator the variables must be entered manually. The parameter list spreadsheet maps the variable state to the corresponding version of the IC, so the user can easily modify the netlist and import the model to other SPICE simulators.

Simulation Performance Curves

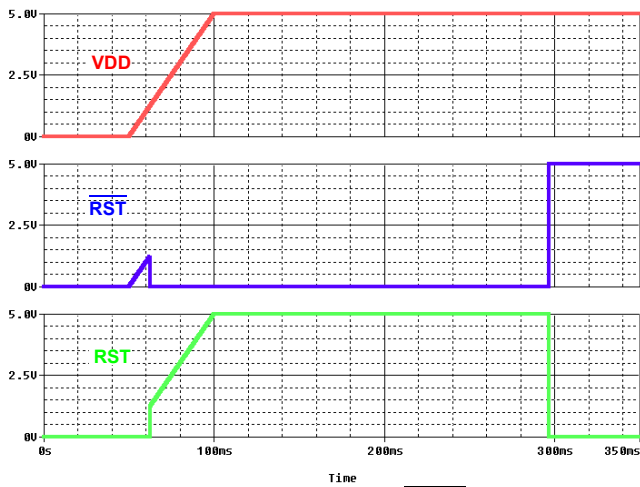


FIGURE 2. ISL705xRH RESET AND $\overline{\text{RESET}}$ ASSERTION

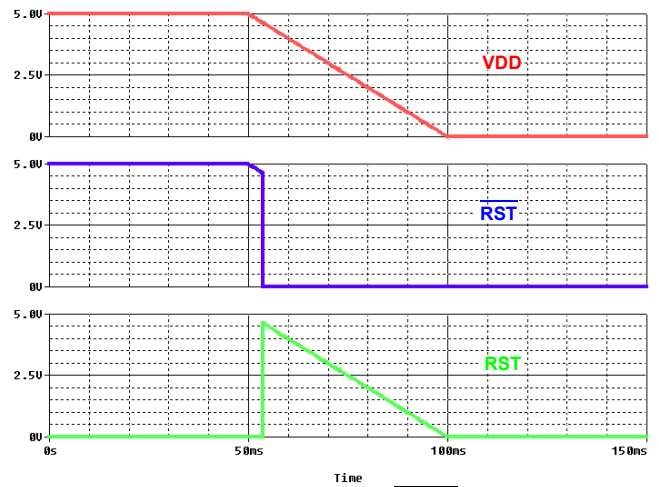


FIGURE 3. ISL705xRH RESET and $\overline{\text{RESET}}$ DEASSERTION

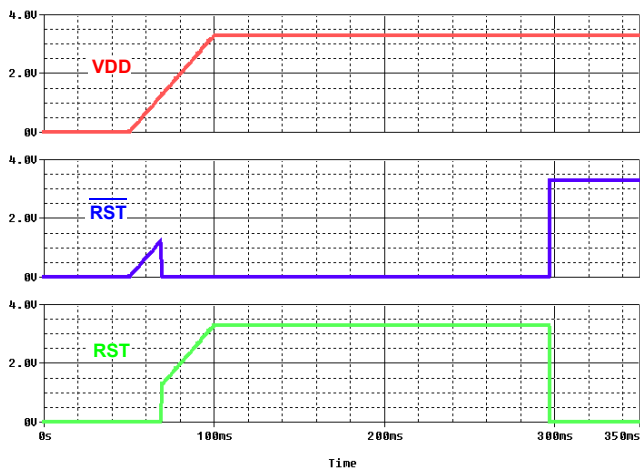


FIGURE 4. ISL706xRH RESET AND $\overline{\text{RESET}}$ ASSERTION

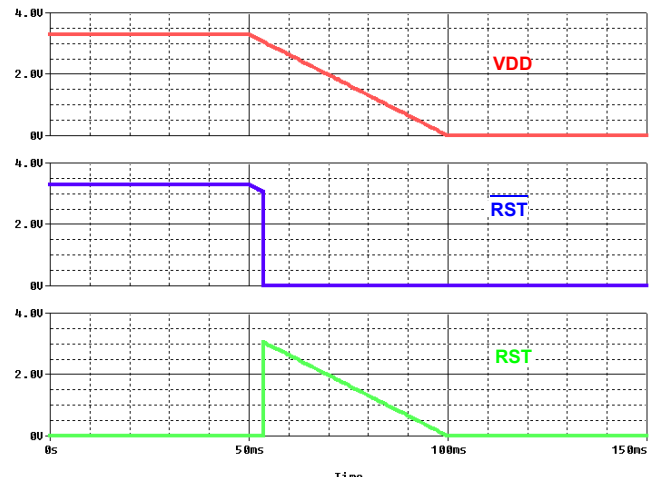


FIGURE 5. ISL706xRH RESET and $\overline{\text{RESET}}$ DEASSERTION

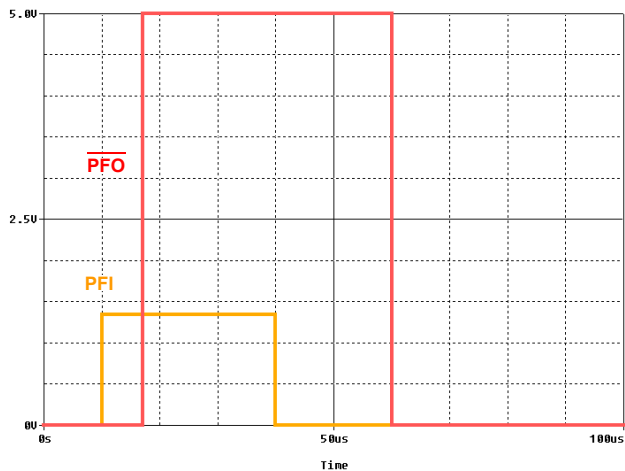


FIGURE 6. ISL705xRH PFI TO $\overline{\text{PF0}}$ RESPONSE

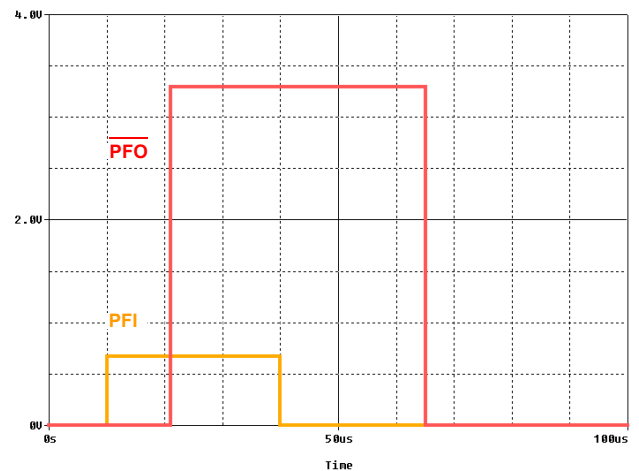
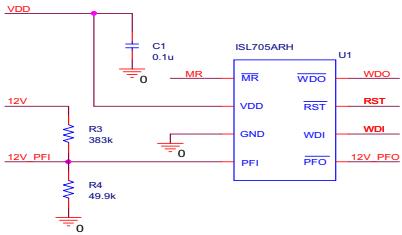
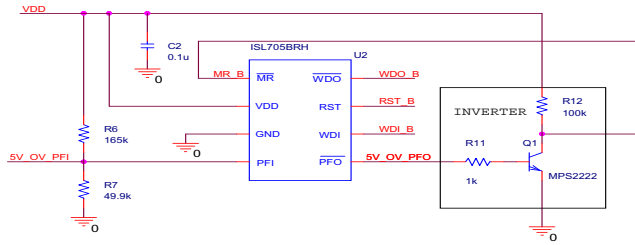


FIGURE 7. ISL706xRH PFI TO $\overline{\text{PF0}}$ RESPONSE

SECTION 1 (ISL705ARH)



SECTION 2 (ISL705BRH)



SECTION 3 (ISL705CRH)

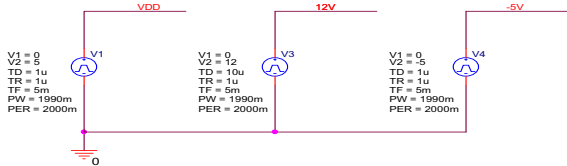
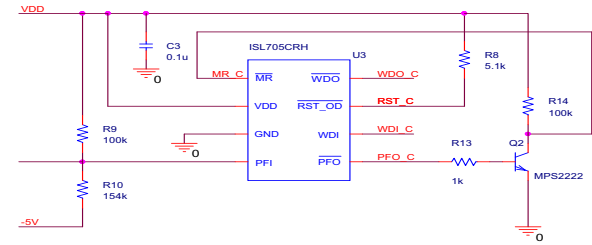
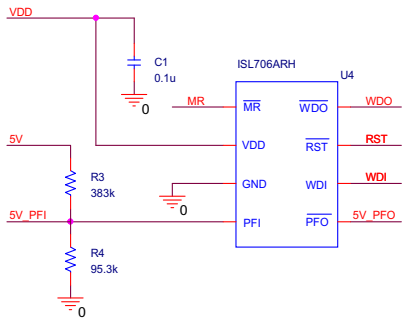
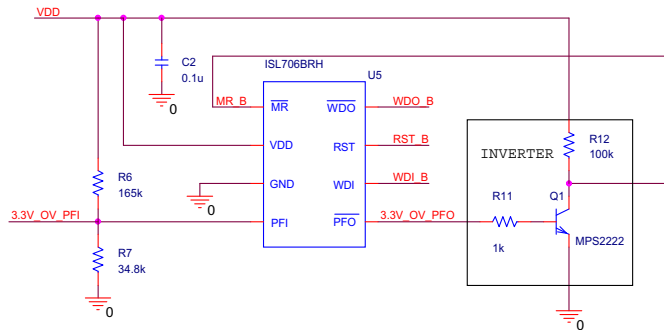


FIGURE 8. ISL705xRH SIMULATION APPLICATION SCHEMATIC

SECTION 1 (ISL706ARH)



SECTION 2 (ISL706BRH)



SECTION 3 (ISL706CRH)

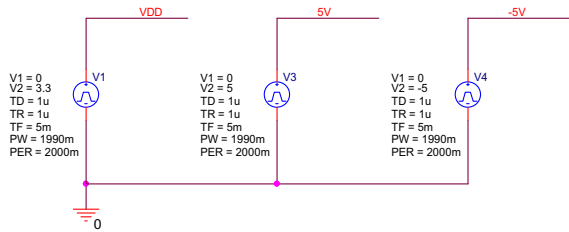
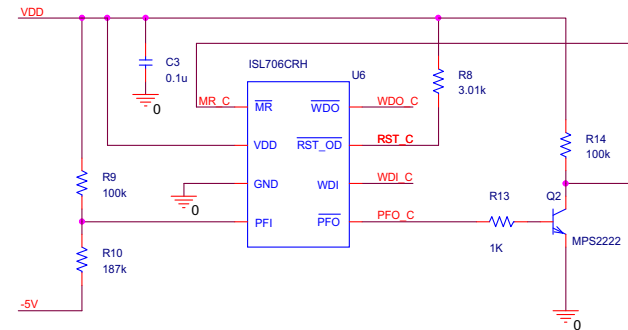


FIGURE 9. ISL706xRH SIMULATION APPLICATION SCHEMATIC

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