Recommended Test Procedures for Analog Switches

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The following text describes the basic test procedures that can be used for most Intersil CMOS switches. Various test conditions are used with the various switches. Table 1 has been included to help define the specific test setups to be used with each variety of switch. One additional note, all schematics assume an open switch for high logic inputs (i.e., NC).

DC Switch Parameters

$+V_S$, $-V_S$: ANALOG SIGNAL RANGE

The analog signal range is the maximum input signal level which can be switched to the output with minimal distortion. For supply voltages lower than nominal, the analog signal range should be restricted to the voltage span between the supplies. Note that other parameters, such as “ON” resistance and leakage currents, are guaranteed over a smaller input range and tend to degrade toward the analog limits ($+V_S$ and $-V_S$). Intersil switches can tolerate the positive analog signal limit ($+V_S$) applied to one side of a switch cell while the negative analog signal limit ($-V_S$) is applied to the other side (the switch must be open to avoid excessive currents).

The analog signal range is measured (Figure 1) by increasing an input waveform until the output shows evidence of distortion or the maximum analog level is reached (as stated in the maximum ratings section of the data sheet).

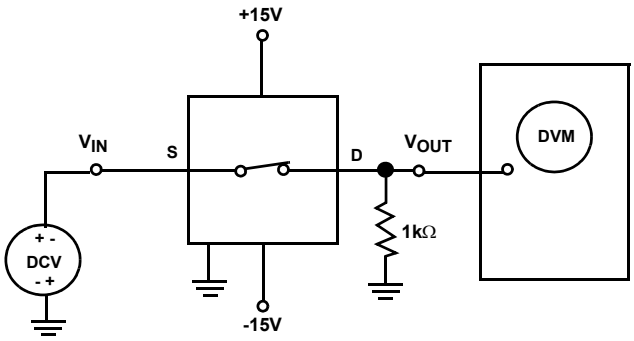
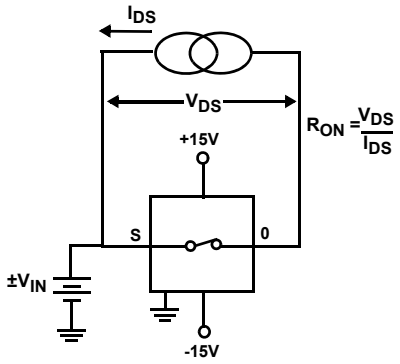


FIGURE 1. SUGGESTED CIRCUIT TO DETERMINE ANALOG SIGNAL RANGE

R_{ON}: ON RESISTANCE

“ON” resistance is the effective series on-switch resistance measured from input to output under spedified conditions. Note that R_{ON} typically changes with temperature (highest at high temperature), and to a lesser degree with signal voltage and current.

R_{ON} is calculated from the voltage drop across a switch with a known current flow as in Figure 2.



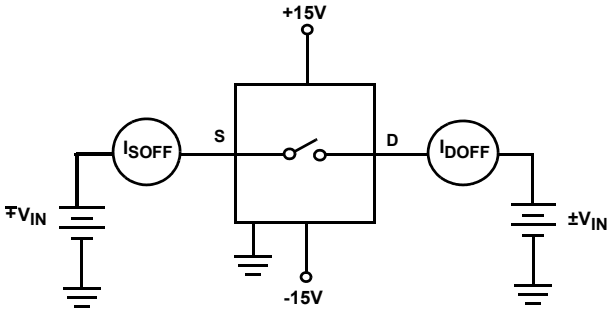
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 2. “ON” RESISTANCE TEST CIRCUIT

$I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$: LEAKAGE CURRENTS

Intersil prefers to guarantee only worst case high temperature leakage currents because the room temperature picoampere levels are virtually impossible to measure repeatedly on currently available automated test equipment. Even under laboratory conditions, fixture and test equipment leakage currents may frequently exceed the device leakage currents. Since the leakage currents tend to double for every 10°C increase in temperature, it is reasonable to assume that the +25°C value is about 1/1000 the +125°C value; however, in some cases there may be ohmic leakage paths, such as across the package, which would tend to make the +25°C reading slightly higher than expected.

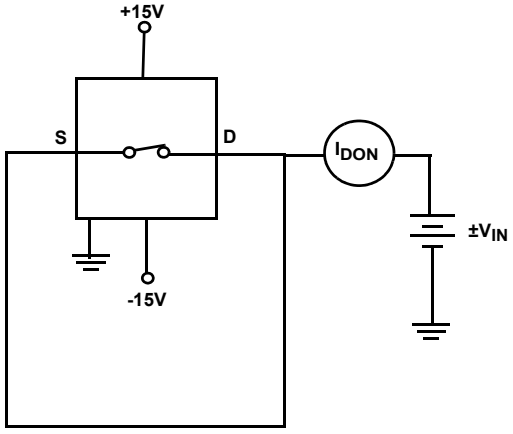
$I_{S(OFF)}$, measured directly with the circuit in Figure 3, consists largely of the diode leakage current from the source-body junction. $I_{D(OFF)}$, also measured directly with the circuit in Figure 3, is largely due to the diode leakage current in the drain-body junction.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 3. OFF LEAKAGE CURRENT TEST CIRCUIT

"ON" leakage current ($I_{D(ON)}$) is the current flowing through both the source-body and drain-body junctions of a closed switch. $I_{D(ON)}$ tends to have the most noticeable effect since it creates an offset voltage across the switch equal to $I_{D(ON)}$ *R_{ON}. $I_{D(ON)}$ is measured directly with the circuit in Figure 4.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

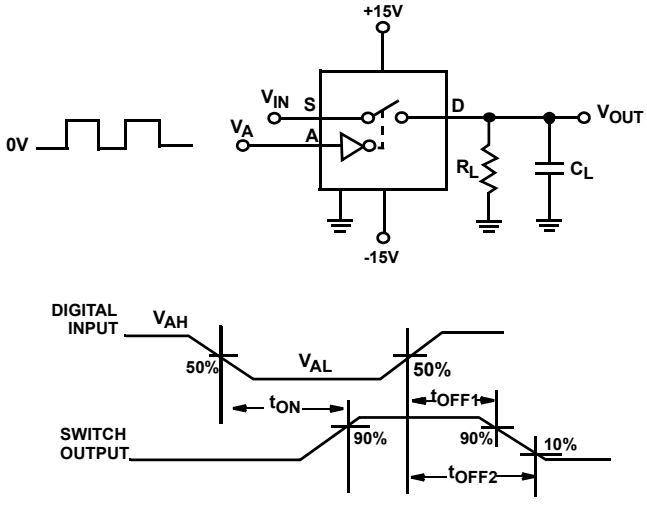
FIGURE 4. "ON" LEAKAGE CURRENT TEST CIRCUIT

Dynamic Switch Parameters

t_{ON}, t_{OFF}: ACCESS TIME

Switch "Turn On" time t_{ON} is the time required to activate an "OFF" switch to an "ON" state. t_{ON} is measured from the 50% point of the logic transition to the 90% point of the output transition (Figure 5).

Switch "Turn Off" time t_{OFF} is the time required to deactivate an "ON" switch to an "OFF" state. t_{OFF} is measured from the 50% point of the logic transition to either the 90% point or 10% point (Figure 5).



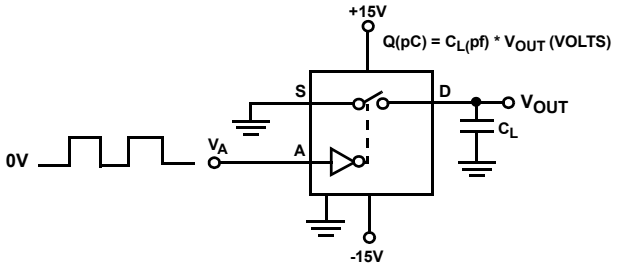
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 5. "TURN ON" AND "TURN OFF" DELAY TEST CIRCUIT AND WAVEFORMS

CHARGE INJECTION

Cycling a switch "ON" or "OFF" results in a small amount of charge being injected into the analog signal path. This charge injection is generated through the capactive coupling between the digital control lines and the analog outputs. The ensuing voltage spikes create an acquisition interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled onto the analog lines is especially critical when switching voltage to a capacitor since the injection charge will change the capacitor voltage at the instant of switching.

Charge injection, measured in pico-coulombs, is measued with the aid of the circuit in Figure 6.

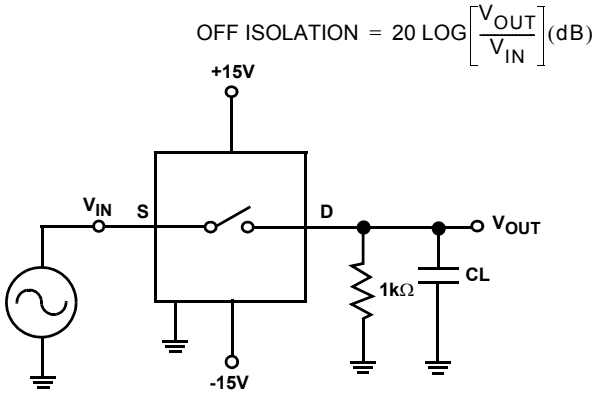


SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 6. CHARGE INJECTION TEST CIRCUIT

OFF ISOLATION

Off isolation is the degree of attenuation seen at the output of an "Open" switch when a high frequency signal is applied to the input. This feed through occurs through the source-body and drain-body capacitances and has a greater effect at higher frequencies. Off isolation is usually specified in decibels where Off Isolation = 20Log (V_{OUT}/V_{IN}), see Figure 7. The islolation generally decreases by 10dB/decade with increasing frequency.



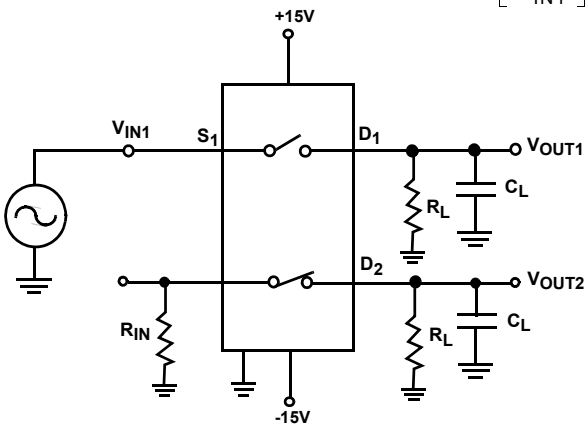
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 7. OFF ISOLATION TEST CIRCUIT

CROSSTALK

Crosstalk is the amount of signal cross coupling from an “OFF” analog input to the output of another “ON” channel output. Crosstalk is usually measured in decibles where: Crosstalk = $20\text{Log}(V_{OUT2}/V_{OUT1})$, see Figure 8.

$$\text{CROSSTALK} = 20\ \text{LOG}\left[\frac{V_{OUT2}}{V_{IN1}}\right](\text{dB})$$

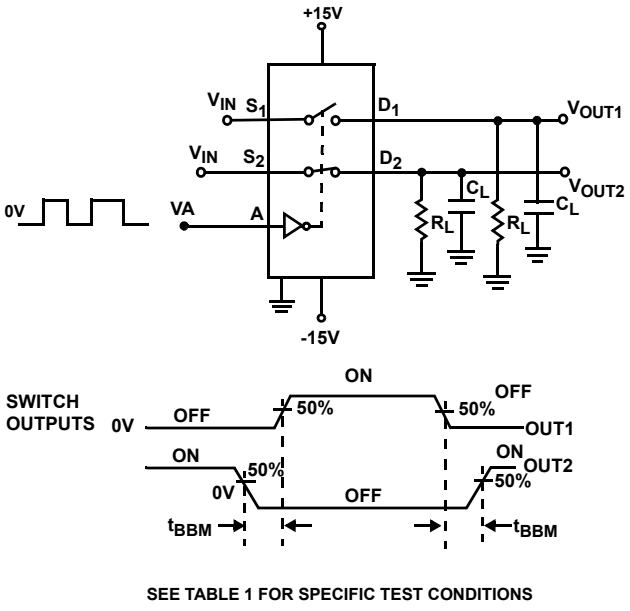


SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 8. GENERAL CROSSTALK TEST CIRCUIT

$T_{(BBM)}$: BREAK-BEFORE-MAKE-DELAY

The break-before-make-delay $T_{(BBM)}$ is the elapsed time between the “Turn Off” of one switch and the corresponding “Turn On” of another for a common change in logic states (Figure 9). The delay measurement is taken at the 50% levels of the output transitions. The $T_{(BBM)}$ delay prevents the switches from being simultaneously closed during switching transitions.



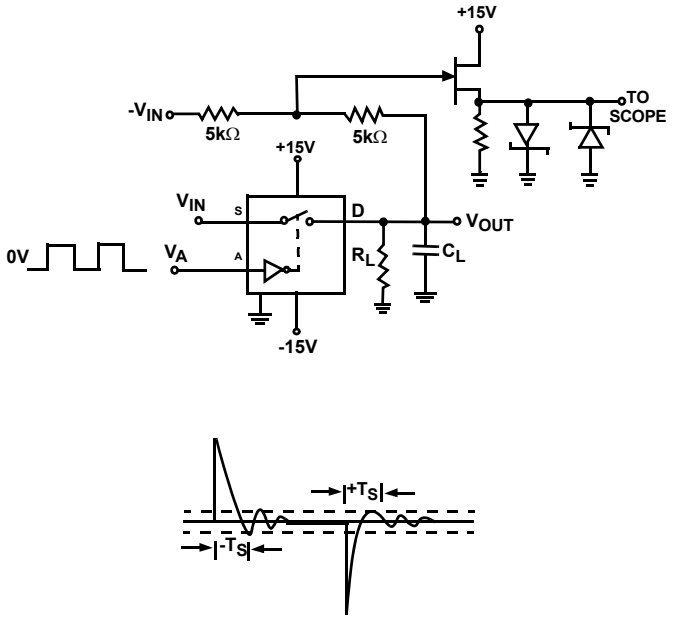
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 9. BREAK-BEFORE-MAKE-DELAY TEST CIRCUIT AND WAVEFORMS

SETTING TIME

Setting time is the time required for the switch output to settle within a given percentage of the final value following a change in the digital input level. Usually the worst-case settling time occurs when the switch is required to slew across its full dynamic range (generally a 0V to +10V transition). This is known as full-scale settling time.

The settling time circuit, Figure 10, employs two resistors to generate an error voltage equal to the output error. A FET is used to buffer the summing junction from the oscilloscope probe capacitance.



SETTLING TIME (T_S) IS MEASURED USING A HIGH SPEED RECOVERY OSCILLOSCOPE TO DISPLAY THE ERROR VOLTAGE V_E.

SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 10. SETTLING TIME TEST CIRCUIT AND WAVEFORM

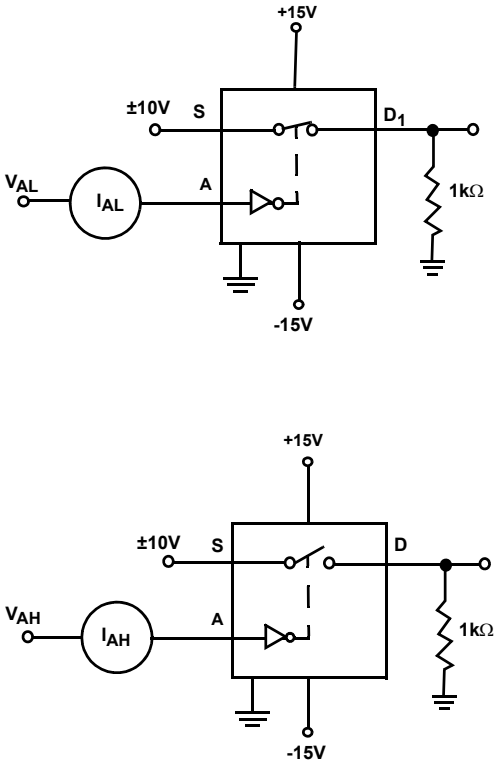
Switch Logic Parameters

V_{AL}, V_{AH}: INPUT THRESHOLDS

The input thresholds are the digital input upper and lower limits at which proper switching action is guaranteed to take place. The input low threshold V_{AL} is the maximum allowable voltage that can be applied to the digital input and still be recognized as a logic low (“0”) input. The input high threshold V_{AH} is the minimum allowable voltage that can be applied to the digital input and still be recognized as a logic high (“1”) input. All other parameters will be valid if the logic inputs are either below V_{AL} or above V_{AH}.

I_{AL}, I_{AH}: INPUT LEAKAGE CURRENT

Input leakage current is the bias current flowing either into or out of the digital input terminal. Input leakage current high (I_{AH}) is the current flowing while the digital input is in the high state ($\geq V_{AH}$), while input leakage current low (I_{AL}) is the current flowing when the digital input is in the low state ($\leq V_{AL}$). Input leakage currents are measured directly using the circuits in Figure 11.



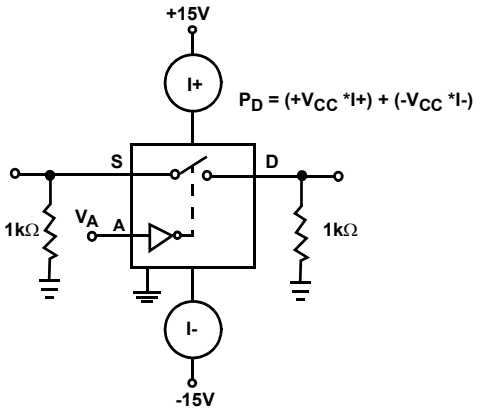
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 11. INPUT LEAKAGE CURRENT TEST CIRCUITS

Static and Package Related Switch Parameters

I+, I-, P_D: POWER DISSIPATION

Quiescent power dissipation $P_D = (+V_{CC}*I+) + (-V_{CC}*I-)$ (Figure 12). P_D may be specified with the switch in either a cycling or a steady state condition. Note that, as with all CMOS devices, power dissipation increases with switching frequency.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 12. SUPPLY CURRENT TEST CIRCUIT

$C_{S(OFF)}$, $C_{D(OFF)}$, $C_{D(ON)}$, $C_{DS(OFF)}$,C_A: SWITCH CAPACITANCE

The various switch capacitances are stated as typical values. These values are given by design and are not subject to production testing (Figure 13).

Capacitance Source-Off $C_{S(OFF)}$ is the capacitance with respect to ground seen at the analog input with the switch open. This capacitance is the sum of the source capacitance of the N-channel and P-channel switching devices.

$$C_{S(OFF)} = C_{SGP1} + C_{SBP1} + C_{SGN} + C_{SBN}$$

Capacitance Drain-Off $C_{D(OFF)}$ is the capacitance with respect to ground seen at the output terminal with the switch open. This capacitance is the sum of the drain capacitance of the N-channel and P-channel switching devices.

$$C_{D(OFF)} = C_{DGP1} + C_{DBP1} + C_{DGN} + C_{DBN}$$

Capacitance Drain-On $C_{D(ON)}$ is the capacitance with respect to ground at the drain with the switch closed. Generally $C_{D(ON)}$ is the total of the source-off and drain-off capacitances.

$$C_{D(ON)} = C_{D(OFF)} + C_{S(OFF)}$$

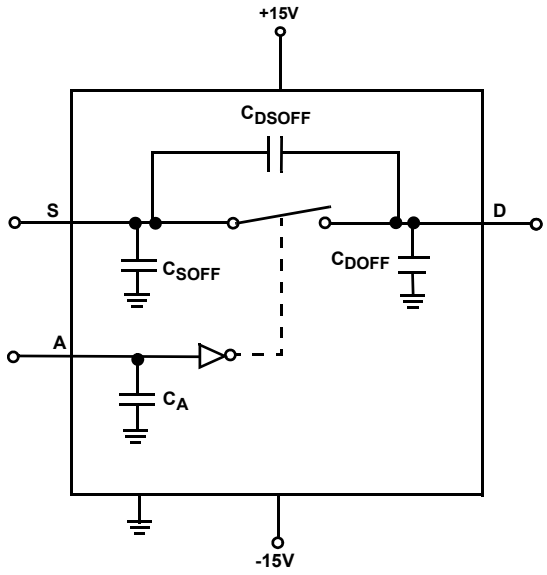
Input to output capacitance $C_{DS(OFF)}$ is the capacitance between the analog input and output with the switch open.

Digital input capacitance C_A is the capacitance with respect to ground at the digital input. C_A chiefly affects propagation delays when the switch is driven by CMOS logic.

Switch Test Fixture Design Rules

The high performance characteristics of Intersil switches require high quality test fixtures for accurate characterization. The following design rules should eliminate most sources of error and provide highly accurate results.

- Decoupling capacitors should be placed as close to the supply pins as possible.
- A ground plane should be used to minimize distributed capacitance.
- All grounds should terminate at a single point ground.
- All sensitive analog lines should be routed between ground traces and kept away from digital lines.
- Analog and digital lines should cross at right angles.
- All unused logic pins should be connected to either V_{AL} or V_{AH}.
- All unused analog pins should be connected to ground through a 1kΩ resistor.
- Teflon sockets should be used to minimize socket capacitance.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 13. EQUIVALENT SWITCH CIRCUIT INCLUDING CAPACITANCES

TABLE 1. TEST CONDITIONS FOR "HI" TYPE SWITCHES

	LOGIC LEVELS	LOGIC REFERENCE	R_{ON}	I_S, I_D	t_{ON}, t_{OFF}	CHARGE INJECTION	CROSSTALK	OFF ISOLATION	SETTLING TIME	BREAK-BEFORE-MAKE	I_{AL}, I_{AH}	POWER DISSIPATION
HI-200	V_{AL} = 0.8V V_{AH} = 2.4V	V_{REF} OPEN	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V R_L = 1kΩ C_L = 35pF V_A = 0V, 4V			V_{IN} = $3V_{RMS}$ f = 100kHz R_L = 1kΩ C_L = 10pF V_A = 5V, 0V		V_{AL} = 0V V_{AH} = 4V	V_{AL} min = 0V V_{AH} max = 5V	V_A = 0V or V_A = 3V
HI-201	V_{AL} = 0.8V V_{AH} = 2.4V	V_{REF} OPEN	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V V_A = 0V, 4V R_L = 1kΩ C_L = 35pF			V_{IN} = $3V_{RMS}$ f = 100kHz R_L = 1kΩ C_L = 10pF V_A = 5V, 0V		V_{AL} = 0V V_{AH} = 4V	V_{AL} min = 0V V_{AH} max = 5V	V_A = 0V or V_A = 3V
HI-201HS	V_{AL} = 0.8V V_{AH} = 3.0V		V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V R_L = 1kΩ C_L = 35pF V_A = 3V, 0V	C = 1000pF	V_{IN} = $3V_{RMS}$ f = 100kHz R_L = 1kΩ V_A = 3V, 0V R_{IN} = 1kΩ	V_{IN} = $3V_{RMS}$ f = 100kHz R_L = 1kΩ C_L = 10pF V_A = 3V, 0V	V_{IN} = +10V R_L = 1kΩ C_L = 35pF V_A = 3V, 0V		V_{AL} min = 0V V_{AH} max = 5V	V_A = 0V or V_A = 3V
HI-303	V_{AL} = 0.8V V_{AH} = 4.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300Ω C_L = 33pF V_A = 4V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = $1V_{RMS}$ f = 500kHz R_L = 1kΩ C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300Ω C_L = 33pF V_{IN} = +3V	V_{AL} min = 0V V_{AH} max = 5V	V_A = 0.8V or V_A = 4.0V
HI-307	V_{AL} = 3.5V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300Ω C_L = 33pF V_A = 5V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = $1V_{RMS}$ f = 500kHz R_L = 1kΩ C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300Ω C_L = 33pF V_{IN} = +3V	V_{AL} min = 0V V_{AH} max = 15V	V_A = 0V or V_A = 15V
HI-390	V_{AL} = 0.8V V_{AH} = 4.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300Ω C_L = 33pF V_A = 5V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = $1V_{RMS}$ f = 500kHz R_L = 1kΩ C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300Ω C_L = 33pF V_{IN} = +3V	V_{AL} min = 0V V_{AH} max = 5V	V_A = 0.8V or V_A = 4.0V
HI-5042 Thru HI-5051	V_{AL} = 0.8V V_{AH} = 3.0V	V_L = 5V V_R = 0V	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +10V	V_{IN} = +10V R_L = 1kΩ	C = 10000pF	V_{IN} = $2V_{P-P}$ f = 100kHz R_L = 100Ω C_L = 15pF R_{IN} = 0Ω	V_{IN} = $2V_{P-P}$ f = 100kHz R_L = 100Ω C_L = 15pF			V_{AL} min = 0V V_{AH} max = 5V	V_A = 0V or V_A = 3.0V

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