Digital IF Subsampling Using the HI5702, HSP45116 and HSP43220

Introduction

This note is about the conversion of previously analog receiver designs into a digital form. It includes a technique for IF subsampling that can simplify the digital circuits compared to a one to one correspondence with analog methods. An example of a Digital Receiver design based on off-the shelf Intersil Components, is included.

Discussion

It is often desired to downconvert a bandpass signal to its baseband representation. Bandpass signals can be expressed as a sum of two quadrature components which are 90 degrees out of phase. In general:

$x(t) = x1(t) \cos\omega_c t + x2(t) \sin\omega_c t$

where x1(t) is the in phase component, x2(t) is the quadrature component of the signal x(t) and ω_c is the center frequency of the band pass signal (carrier frequency).

In the down conversion process the receiver needs to effectively shift the carrier frequency ω_c to baseband (DC). To achieve this one must multiply the incoming bandpass signal x(t) with the complex phasor $[\cos\omega_c t - j\sin\omega_c t]$ and then low pass filter the result. This operation will accomplish the desired frequency shift.

$x(t) [\cos\omega_c t - j\sin\omega_c t] = 1/2[x1(t) + x1(t) \cos2\omega_c t - jx1(t) \sin2\omega_c t + x2(t) \sin2\omega_c t - jx2(t) + jx2(t)\cos2\omega_c t]$.

After low pass filtering, the second harmonic components are filtered out and the result is the desired baseband signal representation of x(t):

LPF (output) $= 1/2[x1(t) - jx2(t)]$.

Figure 1 illustrates the Functional Block Diagrams that represent this mathematical process.
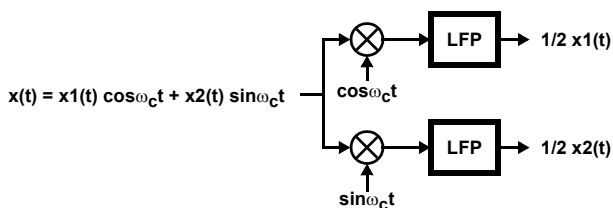
FIGURE 1. BASEBAND DOWNCONVERSION BLOCK DIAGRAM

An all digital implementation of this function implies that the A/D converter needs to digitize the incoming waveform x(t). The carrier frequency ω_c is typically much higher than the frequency of the actual baseband signal. The Nyquist criterion specifies the minimum sampling rate of the A/D required for signal reconstruction. This minimum sampling rate is defined as twice the frequency of the baseband signal. Based on this definition alone it appears that the carrier frequency ω_c does not influence the sampling rate of the A/D converter. For example, if a baseband signal of 9600 bits/sec is transmitted

using a ω_c of 45MHz at the A/D input, then the sampling rate to reconstruct the 9600 bits/sec signal needs to be a minimum of 9600 x 2 = 19.2kHz. The 19.2kHz rate is the signal reconstruction requirement for the sampling rate independent of the value of ω_c. Based on this discussion, a low speed A/D can potentially be used to sample the signal at very high IF frequencies and still recover the baseband information. This concept is referred to as undersampling or subsampling. Subsampling makes an all digital implementation of down conversion at high IF frequencies (i.e., 40MHz-200MHz) feasible. This is because A/Ds would no longer present a limiting factor. A/Ds at low sampling rates are relatively inexpensive and available. From a pure Nyquist rate, theoretical standpoint, this appears as a viable approach; in practice though there are a number of additional factors that need to be evaluated for such a design. The A/D requirements are still a key factor and they impact the design outcome and overall feasibility to a great extent. The designer must carefully analyze the following requirements before deciding on an A/D for a particular undersampling application.

A/D Dynamic Range Requirement: This is derived by examining the operational environment and the desired system signal to noise ratio. The noise environment, signal interference conditions, multipath, and adjacent channel rejection requirements are some of the primary variables that influence the dynamic range specifications of the A/D in a classical receiver architecture. In addition, the existence of a system AGC and the parameters of the filters that proceed the A/D need to be taken into account for these calculations.

A/D Sampling Rate Requirement: This is derived primarily from the baseband signal bandwidth. The minimum rate is defined by the Nyquist criterion. The overall system frequency plan and the baseband digital rates required by the system can also influence the decision on the rate selection. Implementation issues such as availability of only certain clock rates can also play a role in selecting the sampling rate. A minimum rate may be set by the A/D track and hold droop specification.

A/D Track and Hold Aperture Jitter Requirement: This requirement is a function of the IF frequency. The track and hold circuit must have enough bandwidth to adequately cover the IF frequency that is being sampled. In addition, the effects on the system performance due to the sampling aperture error have to be evaluated. The aperture jitter of the track and hold directly influences this aperture error result. The degradation due to aperture jitter is a function of the sampled IF frequency. The higher the IF frequency, the tighter the track and hold aperture jitter requirements become in order to maintain a desired aperture error system specification.

An example of a digital receiver application will be used to further elaborate on undersampling and to demonstrate the points made thus far.

This design is based on the Intersil HI5702 A/D for the IF sampling, the Intersil HSP45116 numerically controlled oscillator/modulator (NCOM) to perform the multiplication of the A/D samples with the complex phasor [cosω_c t - jsinω_c t], followed by the Intersil decimating digital filters HSP43220 that generate the low rate filtered baseband data. The down conversion and filtering operations are followed with a digital FSK/FM demodulator that processes the baseband in phase (I) and quadrature (Q) data as it is being output from the digital low pass filters (HSP43220). The digital demodulator can be a simple discriminator implementation based on delay and multiply calculations on the I and Q channels. Figure 2 illustrates this general purpose digital IF design. The Block Diagram includes an optional AGC circuit. The utility of this AGC circuit is explained later in this paper.

The target receiver design is a standard FSK/FM receiver with a 45MHz IF and 25kHz of channel bandwidth. It is also assumed that the FSK data has a deviation of ($\pm$6.4kHz).   This example can be modified for ETACS, AMPS, Nordic Telephone, MMP and other applications. Existing systems that use traditional analog techniques place the A/D after the analog discriminator which performs the FSK/FM demodulation. These systems experience problems with matching the pre detection filtering to

the discriminator. Assuming the S curve characteristics of the analog discriminator, it is apparent that frequency matching of the analog filters becomes essential to maintain acceptable performance. The digital implementation doesn't suffer from possible filter mismatching and digital filters are not subject to phase non linearities. In addition, the digital approach can improve the performance of the adjacent signal rejection over the rejection that is provided by the analog IF filter, in front of the A/D converter.

The Diagram on Figure 2 shows this basic approach which uses subsampling to convert the 45MHz IF to a 1MHz IF. This assumes that the track and hold is integrated with the A/D as is the case with the HI5702. The Frequency Spectrum Diagrams in Figure 2 show the basic signal processing flow in subsampling. The input signal is first filtered using an analog IF bandpass filter and then amplified by an ACG amplifier to a level sufficient to drive the A/D converter. It is then sampled by the high speed track and hold, and quantized by a 4MHz rate clock at the A/D converter. The sampling process creates a spectrum that repeats the original spectrum every multiple of the sampling frequency as shown in Figure 3. The negative part of the spectrum is shown folded back on and interleaved with the positive part.
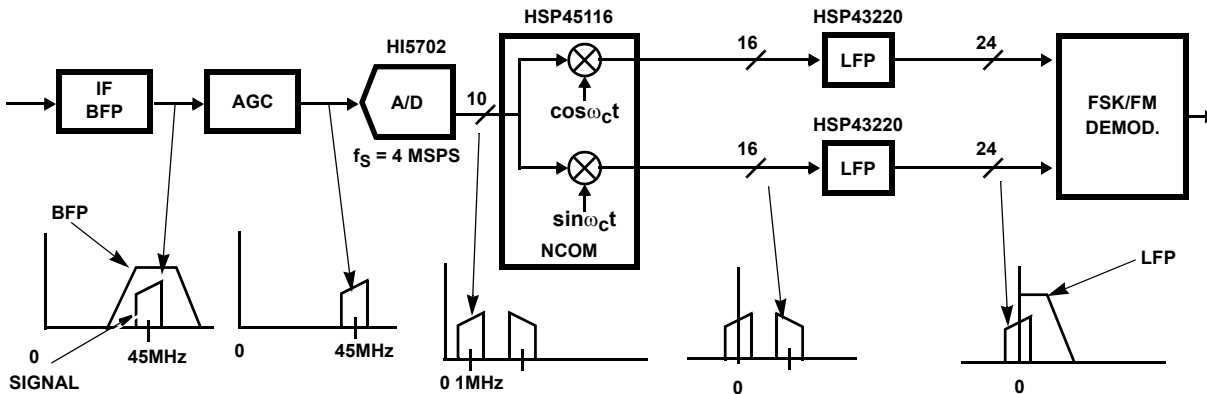

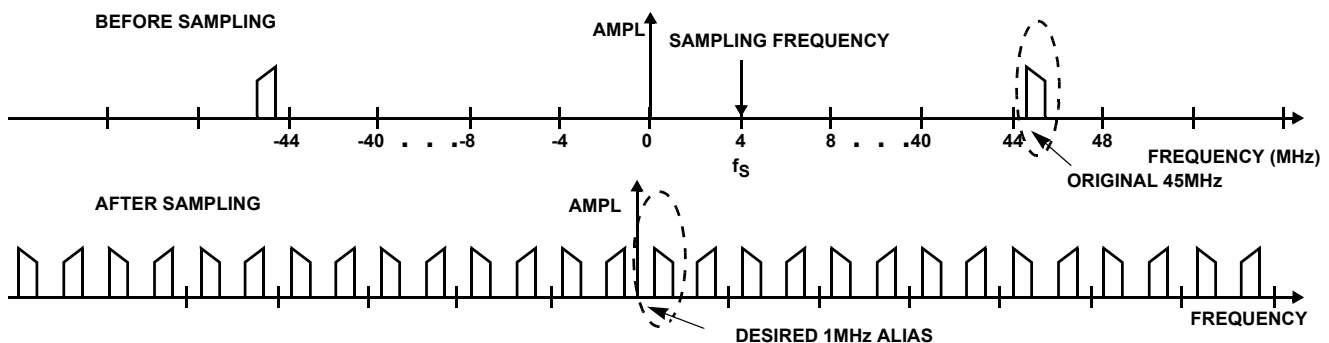**FIGURE 2. DIGITAL IF BASEBAND DOWNCONVERSION BLOCK DIAGRAM**

FIGURE 3. UNDERSAMPLING FREQUENCY PLAN

Two of the repeats (aliases) can be found at frequencies between the sampling frequency and DC. The subsampling approach can

be thought of as generating a signal replica at a much lower IF frequency close to DC. In this example the aliased signal is

centered at 1MHz. This signal is later going to be processed by the NCOM, as shown in Figure 2, to shift it and center it at DC where it can be digitally filtered. The sampling rate, as well as the bit resolution of the A/D are chosen based on the following considerations:

1. The highest usable sampling rate is set by the A/D converter and the subsequent digital processing circuits. For low power operation and ease of processing, the lower the rate, the better. Fundamentally, the lowest rate is twice the signal bandwidth according to the Nyquist criterion. For this example, that works out to 50kHz, given that the signal occupies a 25kHz channel. Practically, however, the filtering in the RF and IF circuits is usually not sufficient to ensure good performance this close in. The sampling frequency has to be high enough so that any noise and interference passing through the RF and IF filtering does not fold back within the sampling bandwidth. These filters only partially reject interference for a bandwidth that is wider than the channel bandwidth. Additionally, the minimum sampling rate is set by the lowest rate that the A/D converter can use without suffering too much track and hold droop. For the Intersil HI5702, the lowest rate is 0.5MHz. For these reasons, the sampling rate was chosen to be 4MHz. This sampling rate aliases the 45MHz IF to create the 1MHz IF. This rate is also easily handled by the Intersil Digital Signal Processing devices (HSP45116, HSP43220) which follow with complex down conversion, decimating and filtering. Higher sampling rates can also be employed if more oversampling of the baseband signal is desired.

2. The digital filters that follow in the processing chain can provide additional adjacent channel rejection to improve selectivity beyond what the analog IF filter is offering. This additional selectivity can be 30-40dB more than provided by the IF filter prior to the A/D. In this example the combination of the analog IF filter and the digital filter selectivities can provide overall adjacent channel rejections of 60dB to 70dB.

One consideration to be addressed is the placement of gain and the use of AGC. In most analog designs, the majority of the gain is in the final IF after the filtering that establishes the selectivity. Since we are using digital processing to do some of this filtering, large interfering signals might exist at the input to the A/D converter. We cannot allow clipping in the IF prior to the A/D converter because of these adjacent channel signals. For this reason, the A/D will have to be operated with adequate headroom in order to ensure that the adjacent channel signals are not above full scale. Another reason to use headroom is Raleigh fading due to multipath. This phenomenon causes rapid variations in the signal level for a number of applications such as a mobile cellular terminal. The receiver of this fading signal needs to handle variations that can potentially range from +10dB to -40dB.

Excluding the requirements for multipath and interference, for +10dB of pre detection SNR alone, the required number of A/D bits is 2 (assuming ~ 6dB/bit). The system, though, needs to achieve 40dB more adjacent channel rejection which implies that the SNR at the A/D will be at -30dB or so given the +10dB of pre detection SNR that is needed. This, along with 6dB of headroom, sets the required A/D quantization to a minimum of 6 bits or about 36dB of ENOB (equivalent number of

bits). To ensure good ENOB performance, an 8-bit A/D should be sufficient. Note that the driving specification for the A/D is the spurious free dynamic range that the system requires.

3. In choosing the subsampling rate one should also be concerned with the phase noise due to the clock edge jitter of the sampling clock. This combined with the inherent aperture jitter in the A/D can limit of how low the sampling rate can be set.

An approximation to the aperture error of the A/D converter can be derived from the formula:

$$ta = \frac{1}{2^n \Pi fmax}$$

where:

n = number of bits
ta = aperture error
$fmax$ = IF frequency

For the given IF frequency and sampling rate the aperture error of the A/D converter needs to be less than 27ps for a 1 LSB degradation at 8 bits. The hold time is 250ns for the 4MHz sampling rate. All of these requirements are met or exceeded with the HI5702 A/D converter.

4. The quantization noise is another noise source that needs attention. For this example, given the choice of the sampling frequency, the quantization noise will be spread over the 4MHz bandwidth and will therefore be attenuated when the signal is filtered to 25kHz bandwidth during the pre detection filtering. This reduction in bandwidth gives 22dB of SNR improvement. With a required SNR of 35dB in 3kHz of bandwidth after the final filtering at the FM demodulator, the quantization noise is not of concern.

The digital filtering process needs to also be evaluated since this process is essential to achieve the additional filter selectivity for the overall system. By using the HSP43220 the additional filter selectivity desired for this application can be achieved. The HSP43220 is a decimating digital filter. Decimation is the filtering operation employed in digital filtering that accomplishes the rate reduction from filter input to filter output. A summary of the HSP43220 features include:

• DC to 33MHz clock rate
• 16-bit 2's complement input
• 20-bit coefficients
• 24-bit extended precision output
• Programmable Decimation up to a maximum of 16,384

Decimation factors, sampling rates and number of filter taps need to be traded in configuring the filter response. For the application of this example the HSP43220 can be programmed to provide the desired filter response. An example of two possible filter specifications are attached. The filter coefficients for these two cases were generated using DECIMATE™ which is a software filter design tool developed for the HSP43220. The user defines the desired filter response and the program determines if the HSP43220 can implement the given response and then it derives the necessary coefficients, and hardware configuration.

The filter parameters as well as the frequency response for these two filter examples are as follows:

Filter 1.

Passband = 7500

Transition Band = 3000

Passband Attenuation = 0.5dB

Stopband Attenuation = 60dB

Input Sample Rate = 4e+06

FIR Input Rate = 125000

Output Rate = 62500s

INTERSIL DECI MATE

HDF FREQUENCY RESPONSE

FIR FREQUENCY RESPONSE

SYSTEM FREQUENCY RESPONSE

RENESAS
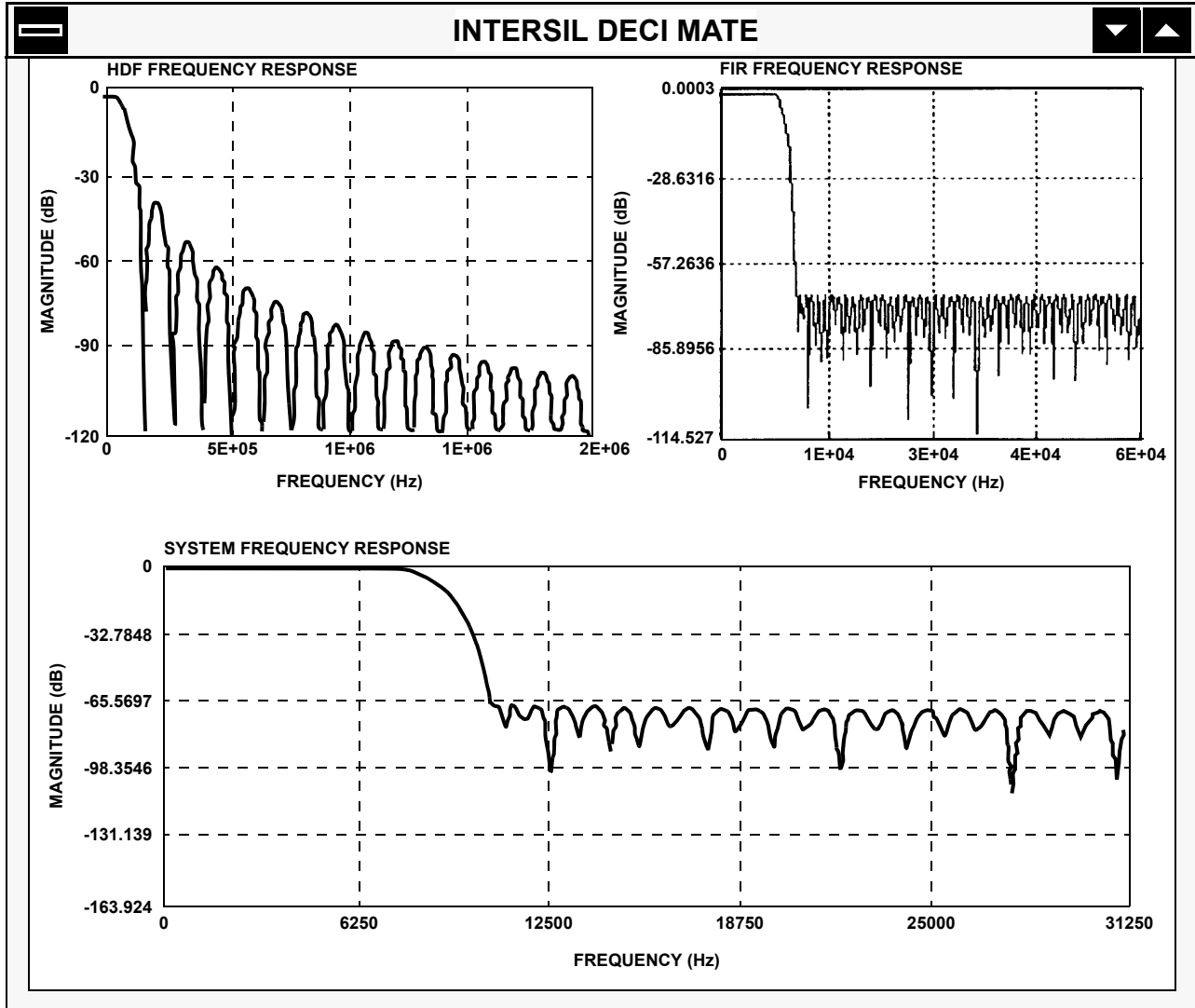
Filter 2.

Passband = 10000
Transition Band = 3000
Passband Attenuation = 0.5dB
Stopband Attenuation = 60dB
Input Sample Rate = 4e+06
FIR Input Rate = 125000
Output Rate = 62500

INTERSIL DECI MATE

HDF FREQUENCY RESPONSE

FIR FREQUENCY RESPONSE

SYSTEM FREQUENCY RESPONSE
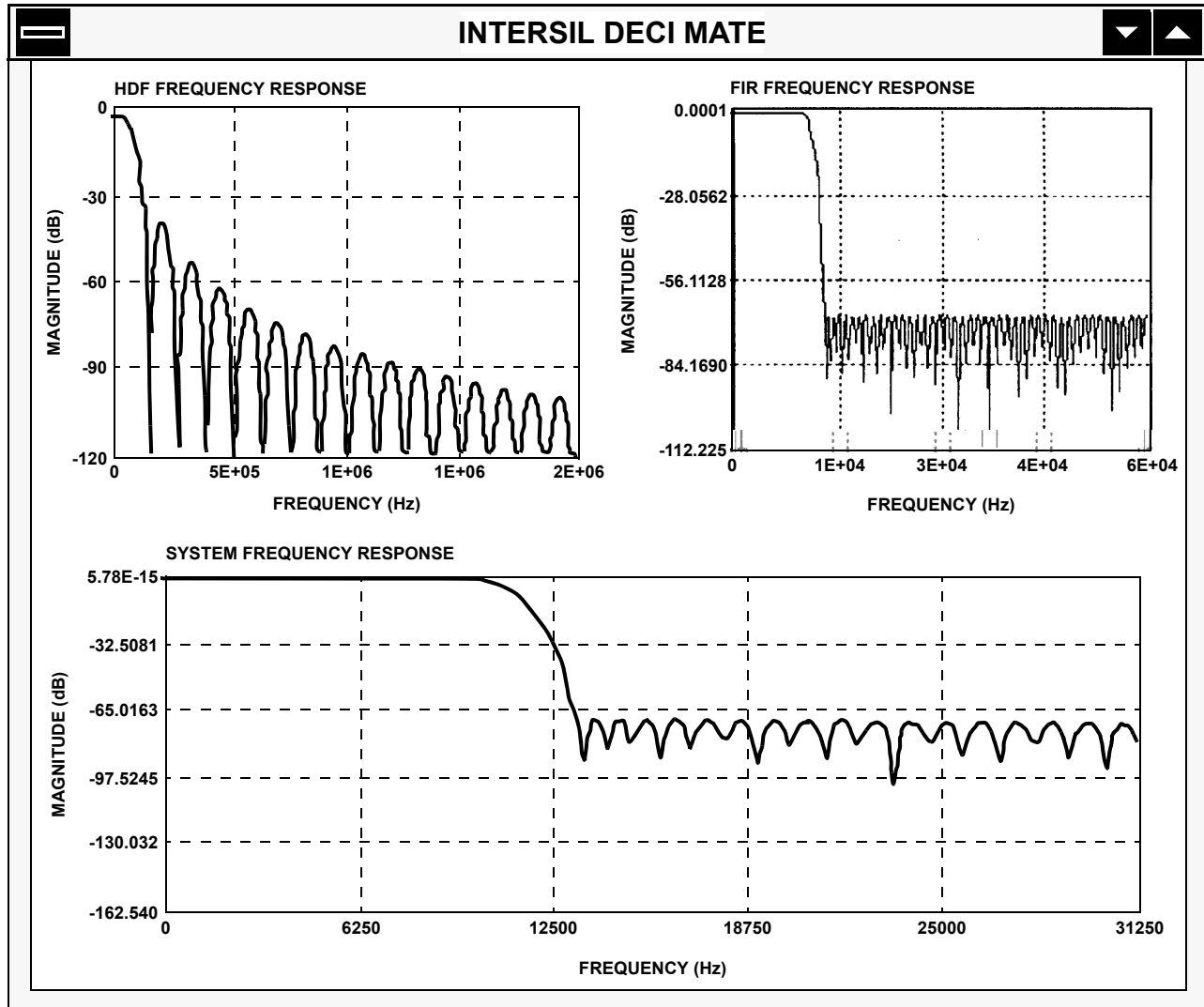
The HSP43220 architecture is composed of the cascade of two filtering stages. The High Order Decimation Filter (HDF), followed by a Finite Impulse Response (FIR) filter. The individual responses of both filters are shown on the two top frequency spectrum responses. The HDF has a sinx/x type of a response and it does the initial filtering followed by the FIR that provides the desired stopband and transition band output characteristics. The cascaded final system response which is the actual output of the HSP43220 is shown on the bottom frequency response plot.

Besides the HSP43220, Intersil has a number of other high speed digital filters that can be appropriate for undersampling applications. The reference part numbers for some of these filter products include the HSP43168, the HSP43124, the HSP43216 and the HSP50016. Information and more details of these digital filters as well as for other Digital Signal Processing (DSP) products can be found in the Intersil DSP Data Book.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

    "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

    "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

    Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1)   "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2)   "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

Renesas Electronics Corporation

http://www.renesas.com