CCE4510 Power-Up Sequencing

This Application Note describes example circuitry to provide a correct power-up sequence for the CCE4510.

Contents

1. General Description

For proper operation of the CCE4510, VDD (pins VDDA or VDDD) must be powered up before VCC (pins VCC or LP1/2).

Not respecting the power-up sequence may result in damage to the IC.

VDD is defined as powered when a voltage level of 3 V is reached, VCC is defined as powered when a voltage level of 8 V is reached. Nevertheless, depending on the power dissipation of the output stage, a damage to the IC is also possible at lower voltage levels of VCC.

VDD is needed to define the state of the output drivers. If VDD is not present and VCC is powered, this could lead to an internal short at the output stage and damage the output drivers.

There are two different scenarios which can be identified as potential causes:

a. LP1/2 is powered by the connected IO-Link Device.
   This is usually prohibited by the IO-Link specification, which states that the IO-Link Device shall always be powered by the master (see IO-Link Interface and System Specification Version 1.1.3, Chapter 5.4).
b. Using the “No Gate Driver / Internal Sense” application (see CCE4510 Datasheet).
   In this case, LP1/2 and VCC are directly connected to the power supply with no external N-channel MOSFET disconnecting LP1/2 from the power supply while turned off.

To prevent any damage to the IC, an additional external circuitry can be implemented to provide a correct power-up sequencing. An example for a discrete solution is provided in this document.

2. Discrete Solution

The discrete example solution uses a P-channel MOSFET to switch on VCC after VDD is powered. To switch the P-channel MOSFET, an N-channel MOSFET is used.

Figure 1 shows the schematic of the discrete example solution.

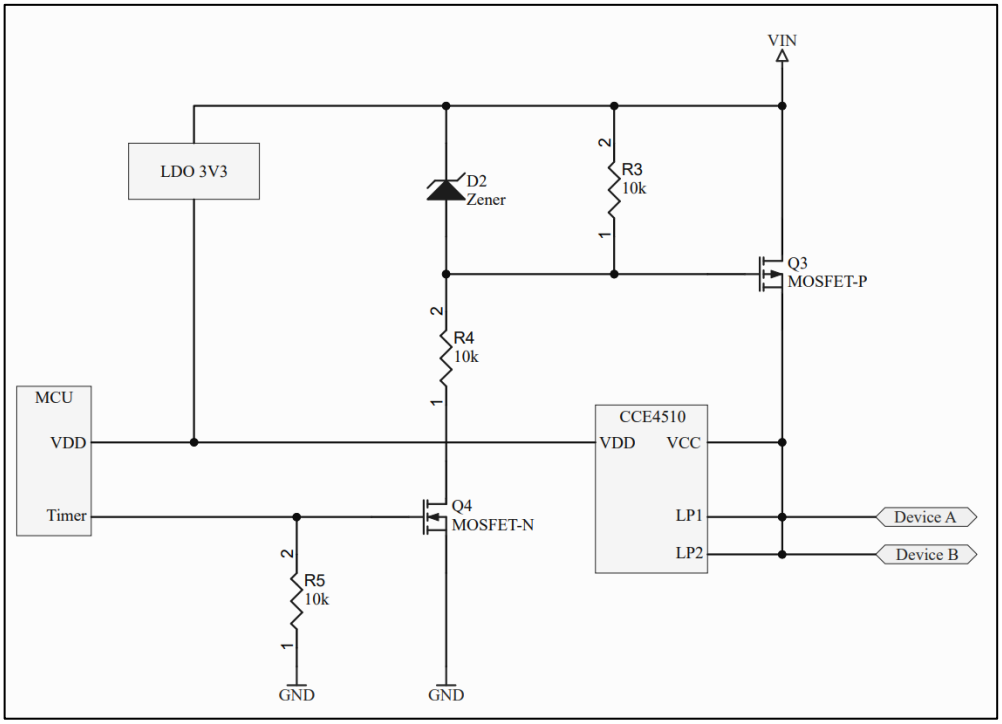

Figure 1. Discrete Example Solution

2.1 General Operating Principle

A P-channel MOSFET (Q2) is used to switch the VCC power supply of the CCE4510. To switch the P-channel MOSFET, an N-channel MOSFET (Q1) is used. The gate-source voltage (V_{GS}) of Q2 is set by the voltage divider R1/R2 so that the required input voltage range is covered. To limit V_{GS} to the maximum allowed V_{GS} of Q2, a Zener-Diode (D1) is used. Q1 is controlled by the MCU, and the gate of Q1 is connected to a pull-down resistor (R3) to make sure it is not floating if the MCU has not actively switched on Q1.

2.2 System and Component Requirements

To provide a fully functional example and to choose components, system and component requirements have been defined.

System Requirements

Requirement	Value
Input Voltage (VCC)	8 V to 32 V
Input Voltage / LDO Voltage (VDD)	3.3 V (typ.)
Output Current	min. 700 mA continuous, 2 A peak (1 ms)

Component Requirements

Component	Requirements
Q1	V_{GS} < 3 V (MCU needs to be able to pull the gate high) V_{DS} > 32 V (when switched off, 32 V can be present)
Q2	V_{GS} < max. Zener break-down Voltage of D1 I_d > 700 mA continuous, 2 A peak (1 ms) V_{DS} > 32 V (when switched off, 32 V can be present)
D1	V_Z needs to be chosen according to Q2s V_{GS}
R1 / R2	Voltage divider needs to fit Q2s V_{GS}
R3	No special requirements

2.3 Example BOM

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	Q1	MOSFET N-CH 60V 200MA SOT23	Toshiba	T2N7002AK
1	Q2	MOSFET P-CH 40V 4.6A SOT23-3	Vishay	SQ2319ADS
1	D1	DIODE ZENER 18V 200MW SOD323	Diodes Inc.	BZT52-C18S
3	R1, R2, R3	RES 10K OHM 5% 1/16W 0402	Yageo	RC0402JR-0710KL

3. Extended Approach

Additionally to the described discrete solution, an extended approach can be used to eliminate the use of the MCU timer pin. For this, an external voltage supervisor from Renesas can be used. A suitable component would be the ISL88001H29Z-T.

The ISL88001 monitors the VDD and turns on the NMOS only when the VDD has passed a certain threshold and the delay time (POR timeout delay) has passed. This secures a safe power-up sequencing, independent from the MCU.

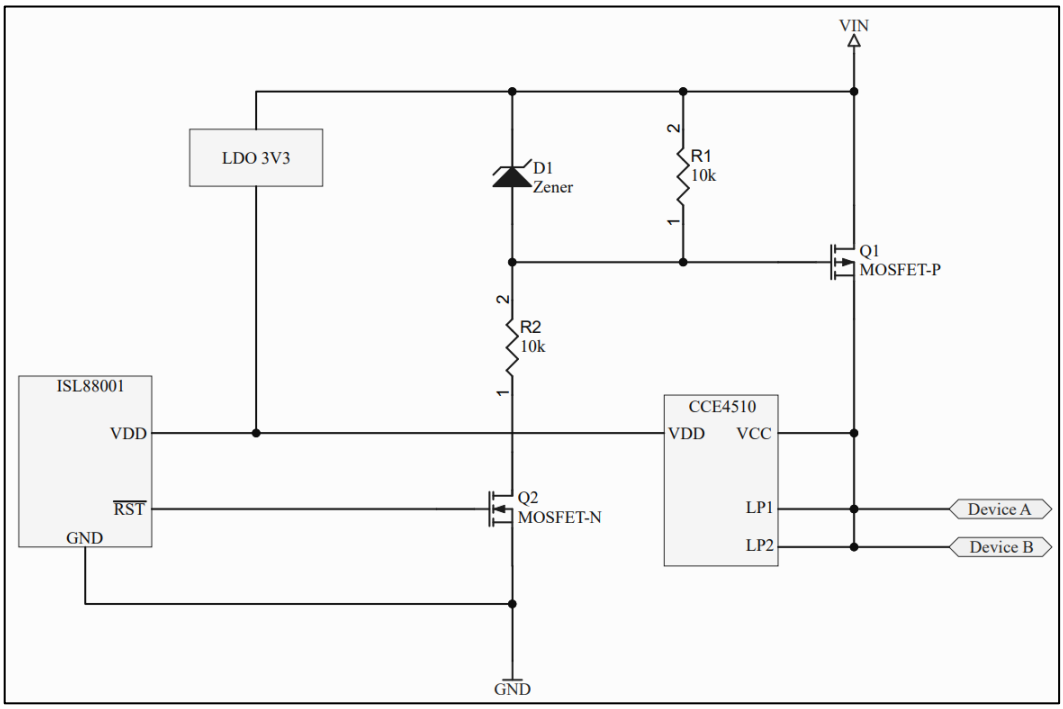

Figure 2. Discrete extended Example Solution

4. Glossary

Term	Description
IC	Integrated circuit
IO	Input output
MCU	Microcontroller unit
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-type metal-oxide semiconductor
POR	Power-on reset

5. Revision History

Revision	Date	Description
1.00	August 1, 2023	Initial release.

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