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Introduction

ClockMatrix provides many tools to manage timing references. It has several different modes to align the output clocks, to control the skew, to measure clocks, select clock sources, and have independent timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks.

A typical large telecom system consists of Line Cards (LCs), Routing/Switching Processors (RSPs), Timing Cards (TC), Fan Trays, back/mid-planes, and/or switching matrixes. Some of these functions can be combined in the same cards (e.g., RSP can have TC functionality as well). If such a system needs to participate in network timing distribution then it is expected that they support SyncE and IEEE1588 standards. It is also expected that these systems contribute very little constant Time Error (cTE) noise to the network clock.

This document addresses the usage of ClockMatrix's Time-to-Digital Converters (TDCs) for precise clock phase measurement using ClockMatrix. It shows the necessary registers to access the TDCs and also the equivalent GUI windows to access using Timing Commander.

Time-to-Digital Converter (TDC)

A TDC circuit is used to recognize events and provide a digital representation of the time they occurred. TDCs are used in applications where measurement events happen either infrequently (e.g., the time of arrival for each incoming pulse) or where measurement events happen in relationship to another event (e.g., the relative offset between an input clock and feedback clock in a DPLL).

ClockMatrix provides access to its DPLL's Phase-Frequency Detector (PFD), or input TDC, for continuous phase measurements between two reference clocks (CLKn). It also provides a dedicated TDC measurement unit, or output TDC, for either single or continuous phase measurements.

Input TDC

Any of the DPLL channels' PFD can be used to measure the phase offset between two input clocks of the same frequency. The PFD has a default resolution of 50ps and a range of ±0.86s. Any frequency from 0.5Hz to 200MHz is supported.

Figure 1. Input TDC Conceptual Diagram

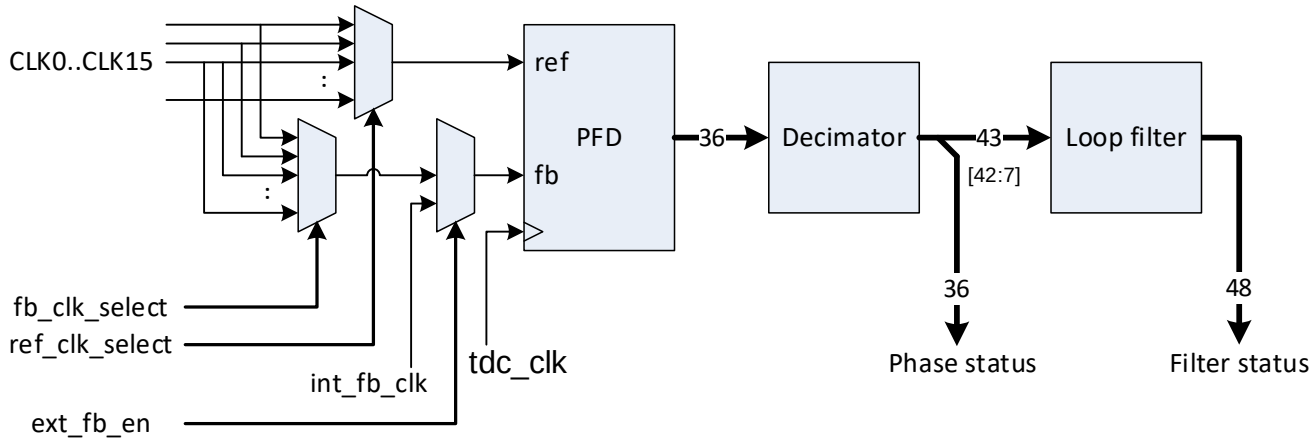
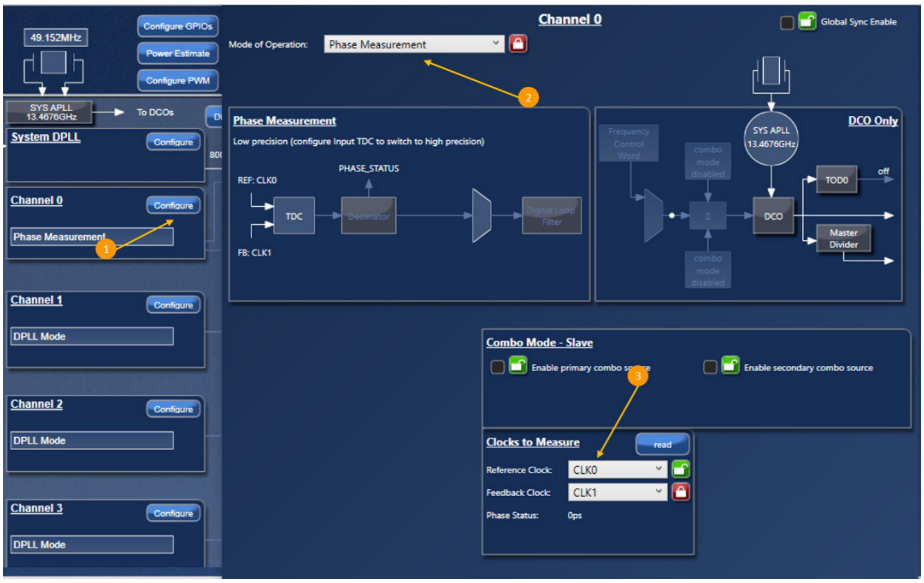


Figure 1 shows the concept of the setup. The reference and feedback clock are selected from inputs CLK0 to CLK15 by programming the DPLL_PHASE_MEASUREMENT_CFG register (for information about which CLKn inputs are available, see the respective datasheet). The registers are shown in Table 1, while the equivalent GUI windows are displayed in Figure 2.

Table 1. Clock Input Selection for Input TDCs Register

Bit Field Name	Field Type	Default Value	Description
PFD_FB_CLK_SEL[3:0]	R/W	0	Select the feedback clock going into the phase detector. The feedback clock selected must have the same frequency as the reference clock selected. 0x00 = CLK0, 0x01 = CLK1, 0x02 = CLK2, 0x03 = CLK3, 0x04 = CLK4, 0x05 = CLK5, 0x06 = CLK6, 0x07 = CLK7, 0x08 = CLK8, 0x09 = CLK9, 0x0A = CLK10, 0x0B = CLK11, 0x0C = CLK12, 0x0D = CLK13, 0x0E = CLK14, 0x0F = CLK15
PFD_REF_CLK_SEL[3:0]	R/W	0	Select the reference clock going into the phase detector. The reference clock selected must have the same frequency as the feedback clock selected. 0x00 = CLK0, 0x01 = CLK1, 0x02 = CLK2, 0x03 = CLK3, 0x04 = CLK4, 0x05 = CLK5, 0x06 = CLK6, 0x07 = CLK7, 0x08 = CLK8, 0x09 = CLK9, 0x0A = CLK10, 0x0B = CLK11, 0x0C = CLK12, 0x0D = CLK13, 0x0E = CLK14, 0x0F = CLK15

Figure 2. Input TDC Input Selection using Timing Commander



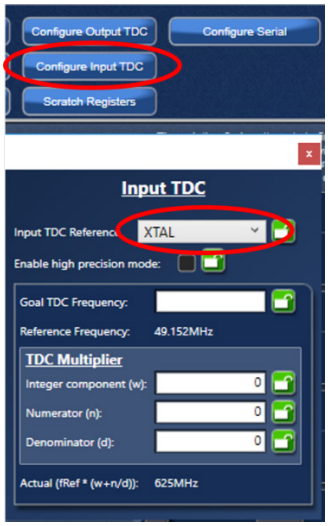
The PFD measures the phase offset between the two clocks for every clock cycle, with a nominal resolution of 50ps (determined from tdc_clk). The phase resolution is 1/32 of the period of the tdc_clk.

By default, the tdc_clk is 625MHz and therefore the phase resolution is 1.6ns/32 = 50ps. The accuracy of the measurement is determined by the selected source. The tdc_clk source can come from the XTAL I/O (default) or XO_DPLL as shown in Table 2. It can be accessed by the GUI as shown in Figure 3.

Table 2. Sample Clock Selection for Input TDCs Register

INPUT_TDC_APLL_REF_SEL	R/W	0	Control mux to forward either a XTAL or XO_DPLL reference towards Input TDC. By default, a XTAL reference is forwarded towards it. 0 = Xtal, 1 = Xo_dpll

Figure 3. Input TDC Reference Selection



Using an nCXO (i.e., via XO_DPLL or overdriving OSCI) will provide for more accuracy in the measurement compared to an uncompensated XO or XTAL. A compensated nCXO assisted to be nominal 0PPM will be even more accurate.

The signed 36-bit phase output (see Table 3) from the phase detector can then be (optionally) low-pass filtered by a decimator, which will also add 7 bits of additional granularity (for more information, see “Finer Measurement Resolution”). As displayed in Figure 1, the signed 36-bit phase values from the phase detector/decimator can be read through the phase_status register, which refreshes every 100 microseconds. When used for phase measurement mode, the range is from (-2^34) to (2^34 -1) ITDC_UI. If PHASE_STATUS is saturated, it is recommended to swap the two clocks being measured.

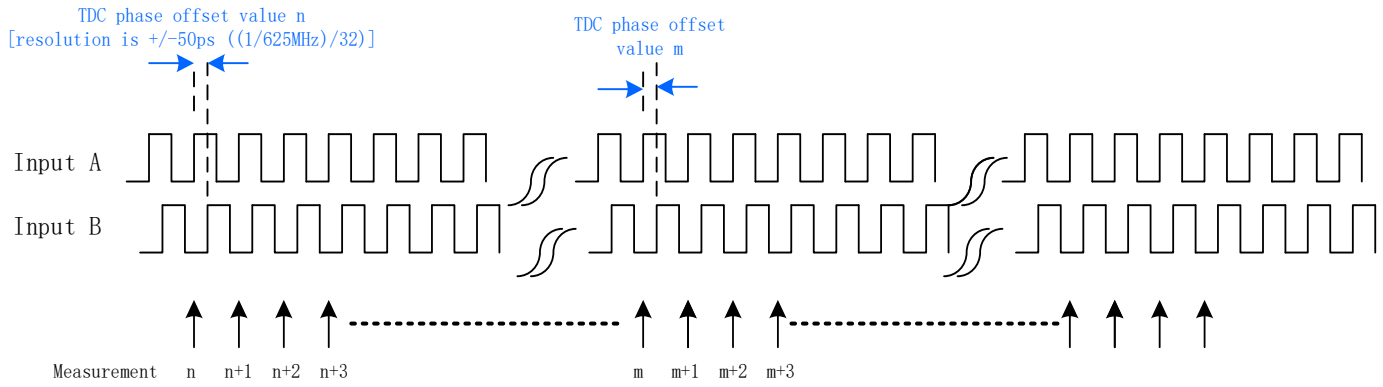
Note: For input clocks < 10kHz, the phase values will update on every input clock cycle (+0~100 microseconds). In the GUI, the phase status can be read from Step 3 in Figure 2.

Table 3. Phase Offset between Two Clocks Register

Bit Field Name	Field Type	Default Value	Description
DPLL_PHASE_STATUS[35:0]	R/O	0	Signed 36-bit phase offset in units of 50 picoseconds.

The phase offset value is a signed value. A +’ve sign means that the feedback clock leads the reference clock; a –‘ve sign means that the feedback clock lags the reference clock.

Figure 4. Input TDC Sampling



As shown in Figure 4, the phase offset of “every” input clock cycle is measured, regardless of its frequency. However, the phase offset register containing this measurement is only refreshed every 100 microseconds. If faster phase offset measurement readings are required, this is supported via direct hardware Control/Status Register access. For more information, contact Renesas technical support.

You must select phase measurement mode as the DPLL’s mode of operation (see Table 4). When using the DPLL channel’s PFD for measurement, the channel becomes unavailable for normal PLL operation but it can be used as a synthesizer. Using the GUI, the PLL mode selection is shown in Step 2 of Figure 2. Also shown in Figure 2, the Channel can also be used in Write Frequency Mode (FCW) when in Phase Measurement Mode. However, FCW can only be used in low precision mode (Phase Status), and not high precision mode (Phase Status and Filter Status). In high precision mode, the channel can only be used as a synthesizer. High precision mode is explained in Finer Measurement Resolution.

Table 4. PLL Mode Selection Register

PLL_MODE[2:0]	R/W	0	DPLL operation mode. 0x0 = PLL mode, 0x1 = write phase mode, 0x2 = write frequency mode, 0x3 = GPIO inc/dec mode, 0x4 = synthesizer mode (DPLL disabled), 0x5 = phase measurement mode

Measuring Asynchronous Clocks

The PFD can measure the phase offset of two asynchronous clocks of the same frequency. However, because the two clocks will drift away from each other over time, the PFD will eventually saturate at ±0.86s of phase offset. For example, if there is 1PPM of frequency offset between the two measurement clocks (the frequency of the clocks is not important), the clock edges between the two clocks will drift away at approximately 1 microsec/sec. Thus, assuming the two edges were exactly aligned at the start of the measurement and the frequency offset is static (i.e., remains at 1PPM), this means after (1,000,000 * 0.86s) = 860,000s (~10 days), the PFD will saturate.

To avoid this, the offset value can be reset by toggling the PLL_MODE. However, this means that the input TDC will also restart its phase measurement from the following edge after returning to phase measurement mode.

Finer Measurement Resolution

The decimator can be used to average the phase detector values and thereby get a better resolution than 50ps. As shown in Figure 1, the decimator provides a 43-bit phase output to the DPLL loop filter but only the upper 36 bits are visible through the phase_status registers. Thus, the filter_status (see Table 5) has 7 bits more lsb resolution than the phase_status, or a resolution of 0.39ps. The filtered/averaged phase value can be read through the filter_status registers, which again refreshes every 100 microseconds. The filter_status can be enabled using the High Precision Mode (0xCD24 bit 7) in the GUI as shown in Figure 5. Once filter_status is enabled, the Channel can no longer be used in Write Frequency Mode while in Phase Measurement Mode. At this point, only Synthesizer Mode can be used with Phase Measurement Mode. Also notice from Figure 5 that the TDC Frequency (tdc_clk) and the TDC Multiplier are changed when High Precision Mode is enabled. This is critical in getting an improved resolution from filter_status. When only phase_status is used, the TDC Frequency is 625MHz. When filter_status is used, the TDC Frequency must not be an integer multiple of the input clock frequencies being measured.

Figure 5. Enabling High Precision Mode

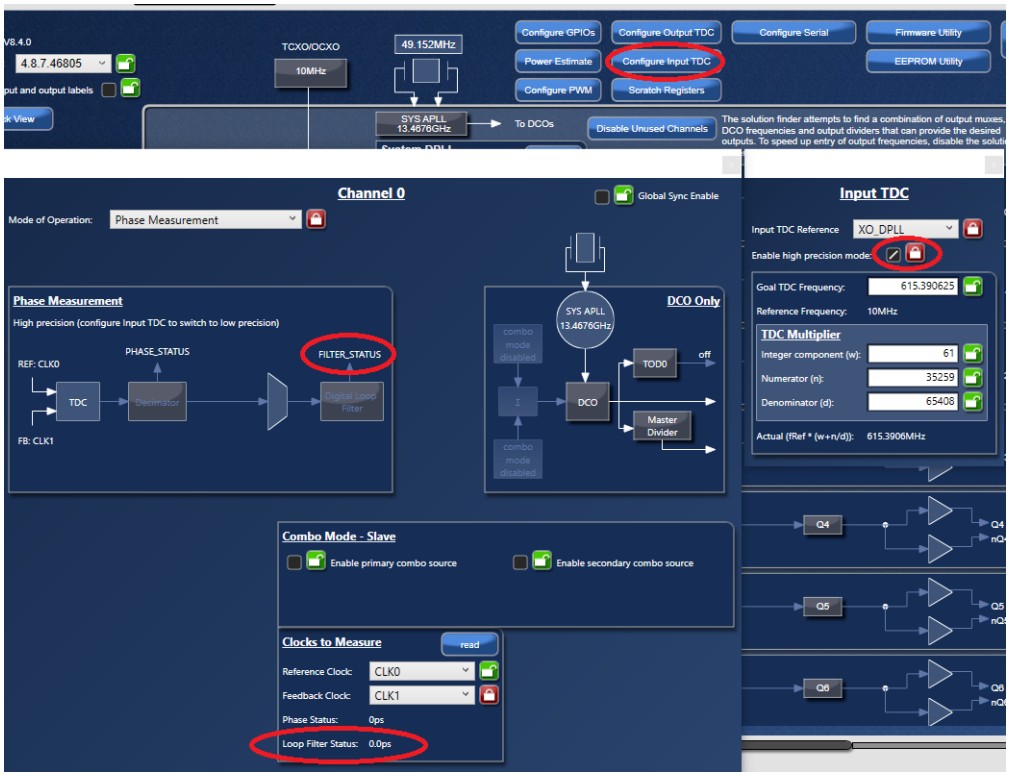


Table 5. DPLL Loop Filter Status Register

Bit Field Name	Field Type	Default Value	Description
FILTER_STATUS[47:0]	R/O	0	DPLL loop filter status. Fine phase measurement in units of 50/128 picoseconds.

In order to get a more precise decimated phase value from the filter_status, the loop filter must be set up such that it is transparent from the decimated phase input to the filter status output. In addition, the decimator needs to be set up as a low pass filter to average the toggling lsb of the phase word from the phase detector. For ClockMatrix, the bandwidth multiplier of the decimator and the bandwidth of the loop filter are pre-set when in phase measurement mode, such that the loop filter is transparent from the decimated phase input.

For the averaging of the phase values from the phase detector (i.e., to get better than 50ps resolution), it is also critical that the TDC Frequency (tdc_clk) is not synchronous (common multiple) to the input clocks. This setup is shown in the Fine Measurement Example. The TDC Frequency can be modified by using the following equation.

$$tdc\_clk = fref\left(w + \frac{n}{d}\right)$$

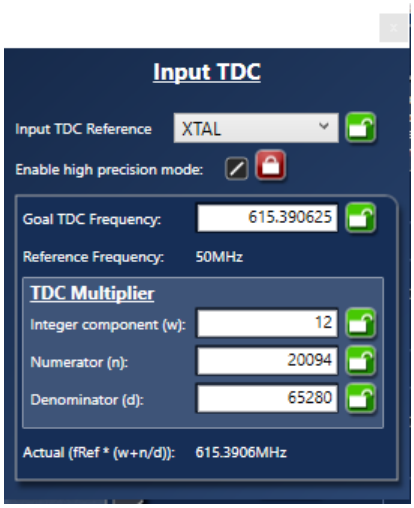
fref = The reference frequency (XTAL or TCXO/OCXO)
w = Integer portion of the divider (0xCD24 bits 6:0)
n = Numerator fractional portion of the divider (0xCD20:0xCD21)
d = Denominator fractional portion of the divider (0xCD22:0xCD23)

Fine Measurement Example

For measuring the phase between two 8kHz signals, the tdc_clk must be changed to a different frequency from 625MHz that is not an integer multiple of 8kHz. When the tdc_clk frequency is divided by an integer number to get the closest to 8kHz, there must be a frequency difference that is large enough to make the averaging work. The frequency offset by itself should not be an integer division of the 8kHz input frequency.

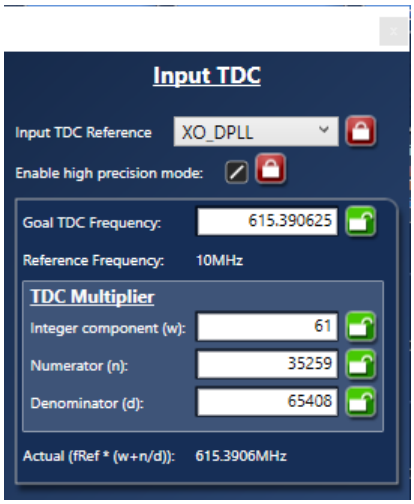
Example 1:

- Xtal frequency = 50MHz
- Input clock frequency of two inputs = 8kHz
- Tdc_clk nominal divide to 8kHz = 625MHz / 8kHz = 78125
- Desired sample frequency offset = 123Hz
- New Tdc_clk frequency = 78125 * (8000 – 123) = 615.390625MHz
  - Phase_status resolution = 1/32 * 1/615390625 = 50.781ps
  - Filter_status resolution = 50.781ps/128 = 0.39672464ps
- Tdc_clk : xtal ratio = 615.390625MHz / 50MHz = 12 + 20094/65280
- 0xCD24 = 0x8C
- 0xCD20 = 0x7E
- 0xCD21 = 0x4E
- 0xCD22 = 0x00
- 0xCD23 = 0xFF



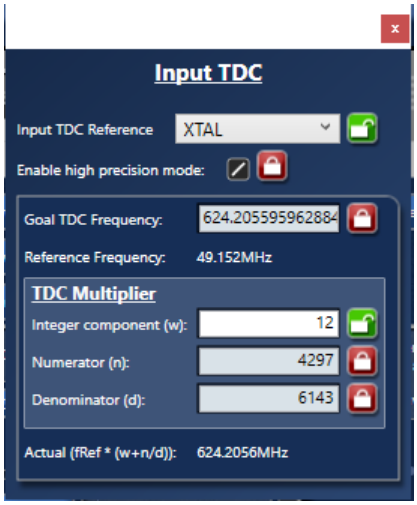
Example 2:

- OCXO frequency = 10MHz
- Input clock frequency of two inputs = 8kHz
- Tdc_clk nominal divide to 8kHz = 625MHz / 8kHz = 78125
- Desired sample frequency offset = 123Hz
- New Tdc_clk frequency = 78125 * (8000 – 123) = 615.390625MHz
  - Phase_status resolution = 1/32 * 1/615390625 = 50.781ps
  - Filter_status resolution = 50.781ps/128 = 0.39672464ps
- Tdc_clk : xtal ratio = 615.390625MHz / 10MHz = 61 + 35259/65408
- 0xCD24 = 0xBD
- 0xCD20 = 0xBB
- 0xCD21 = 0x89
- 0xCD22 = 0x80
- 0xCD23 = 0xFF



Example 3:

- XTAL frequency = 49.152MHz
- Input clock frequency of two inputs = 25MHz
- Tdc_clk nominal divide to 25MHz = 625MHz / 25MHz = 25
- Desired sample frequency offset = 31776.16148Hz
- New Tdc_clk frequency = 25 * (25000000 – 31776.16148) = 624.205595963MHz
  - Phase_status resolution = 1/32 * 1/624205595.963 = 50.063633ps
  - Filter_status resolution = 50.063633ps /128 = 0.39112213ps
- Tdc_clk : xtal ratio = 624.205595963MHz / 49.152MHz = 12 + 4297/6143
- 0xCD24 = 0x8C
- 0xCD20 = 0xC9
- 0xCD21 = 0x10
- 0xCD22 = 0xFF
- 0xCD23 = 0x17



Accuracy vs Precision

The Input TDC Reference Selection (XTAL or XO_DPLL) affects the accuracy, whereas the TDC Multiplier affects the precision.

For small phase offsets using phase measurement such as 1ns or 1ps, XTAL or XO_DPLL do not make a difference in accuracy. For large phase offsets such as 1µs or 1ms, XTAL or XO_DPLL makes a difference in accuracy (see Table 6).

Table 6. Accuracy Difference between XTAL and XO_DPLL for Various Phase Offsets

	XTAL	XO_DPLL
Phase Offset	50 ppm	5 ppm
1.00E-03	5.00E-08	5.00E-09
1.00E-06	5.00E-11	5.00E-12
1.00E-09	5.00E-14	5.00E-15
1.00E-12	5.00E-17	5.00E-18

The Input TDC "Enable high precision mode" affects the precision, not accuracy. Our TDC has a precision of 50ps, however, since we are decimating/averaging/filtering, we can get much better precision down to 1ps and generally improved quantization error. By ensuring the tdc_clk is not an integer multiple of the input reference clocks, then averaging will improve the quantization error. In general, we want the precision to be much better than the accuracy so we are not dominated by quantization error.

Settling Time

The decimator value of the Input TDC is calculated dynamically by the firmware. It will differ depending on the input frequency and the phase offset between the two inputs. For the initial measurement, it could take up to 15 seconds before the phase measurement has settled. Subsequent measurements should converge much quicker (few seconds). However, the accuracy of the measurement itself could be affected by noise such as the stability of the inputs (cycle to cycle jitter and wander), XO (frequency drift), or even the TDC itself. The noise from the TDC itself is a maximum of 90ps.

Output TDC

An output TDC can perform a single measurement of the phase offset between two output channels or between an output channel and a GPIO input. It can also be used to automatically align the outputs of two channels (see Automatic Output Alignment). The PFD has a default resolution of 50ps. Up to four independent, parallel measurements are supported using the output TDC.

Figure 6. Output TDC Conceptual Diagram (Single Instance; Up to Four Supported)

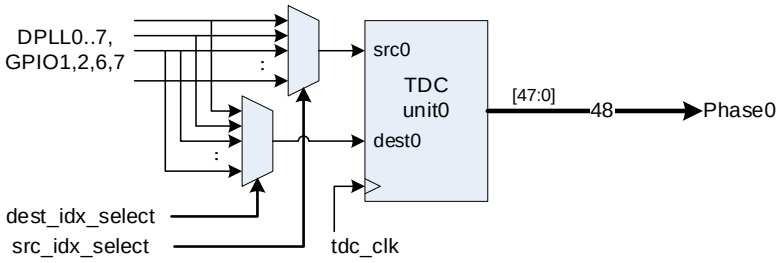
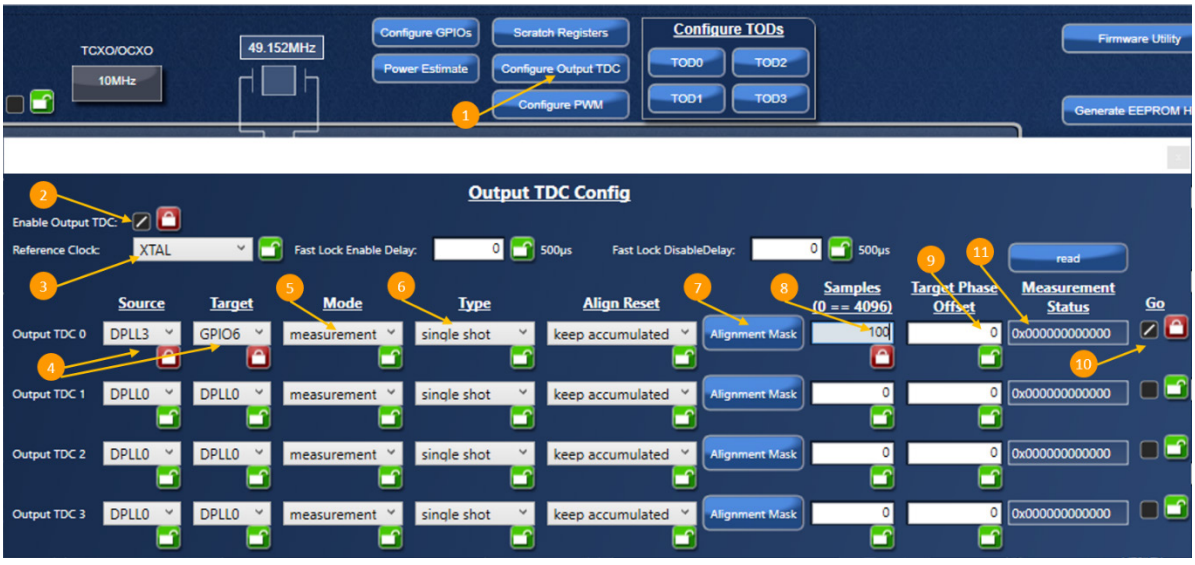


Figure 6 shows the concept of the setup. The reference clocks to the output TDC are selected from channels DPLL0 to DPLL7. In addition, GPIO1, GPIO2, GPIO6, or GPIO7 can be selected as one of the input reference clocks (for more information, see the relevant datasheet on which DPLLn outputs and GPIOn inputs are available). The source and target references can be selected based on Table 7, and is also shown in Step 4 of Figure 7.

Table 7. Output TDC Source and Target Registers

OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3 Bit Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
TARGET_INDEX[3:0]	R/W	0	Used in measurement mode to indicate the target clock. Indicates the target to measure against 'source_index'. 0x0 = DPLL0 0x1 = DPLL1 0x2 = DPLL2 0x3 = DPLL3 0x4 = DPLL4 0x5 = DPLL5 0x6 = DPLL6 0x7 = DPLL7 0x8 = GPIO6 0x9 = GPIO1 0xA = GPIO2 0xB = GPIO7
SOURCE_INDEX[3:0]	R/W	0	Used in measurement and alignment mode to indicate the source clock. Indicates the source to be used as the measurement reference. 0x0 = DPLL0 0x1 = DPLL1 0x2 = DPLL2 0x3 = DPLL3 0x4 = DPLL4 0x5 = DPLL5 0x6 = DPLL6 0x7 = DPLL7 0x8 = GPIO6 0x9 = GPIO1 0xA = GPIO2 0xB = GPIO7

Figure 7. Output TDC using Timing Commander



The output TDC measures the phase offset between the two clocks with a nominal resolution of 50ps (determined from tdc_clk). The phase values from each of the four TDC measurement units can be read through four different phase measurement registers (see Table 8 and Step 11 of Figure 7).

Table 8. Output TDC Phase Measurement Register

Bit Field Name	Field Type	Default Value	Description
PHASE[47:0]	R/O	0	Output TDC measurement. Signed 48-bit integer in picoseconds.

To determine if the value in the PHASE[47:0] register is valid (i.e., after a measurement has completed), a VALID bit should be checked before reading.

Table 9. Output TDC Valid Register

VALID	R/O	0	Indicates a valid measurement or alignment has met target phase offset. When go bit is set, valid is cleared. Measurement mode: Indicates when OUTPUT_TDCn_MEASUREMENT is valid. Alignment mode: Indicates when all the alignment targets are within the OUTPUT_TDC_CTRL_1.target_phase_offset. 0 = invalid 1 = valid

The output TDC uses tdc_clk to sample the input clocks. This clock can come from the XTAL I/O or XO_DPLL (see Table 10 and Step 3 of Figure 7).

Table 10. Sample Clock Selection for Output TDCs Register

REF_SEL	R/W	0	Select reference clock for output TDC. By default, a XTAL drives the output TDC. 0 = XTAL, 1 = XO_DPLL

Similar to the input TDC, the phase resolution is 1/32 of the period of the tdc_clk. By default, the tdc_clk is 625MHz and therefore the phase resolution is 1.6ns/32 = 50ps (note: the input TDCs and output TDC have their own tdc_clk). The accuracy of the measurement is determined by the selected source (XTAL or XO). Using an nCXO (i.e., via XO_DPLL or overdriving OSCI) will provide for more accuracy in the measurement compared to an uncompensated XO or XTAL.

The output TDC is disabled by default to save power when not in use (see Table 11 and Step 2 of Figure 7).

Table 11. Output TDC Enable Bit Register

ENABLE	R/W	0	Enable or disable output TDC. Output TDC is disabled by default to save power when not in use. Ready state is indicated by OUTPUT_TDC_CFG_STATUS.state. 0 = Disable output TDC, 1 = Enable output TDC

Once enabled, the state of the output TDC will reflect when it is ready for measurement.

Table 12. Output TDC State Register

STATE[1:0]	R/O	0	Indicates whether the output TDC is ready to be used. Output TDC is by default disabled. Need to enable with OUTPUT_TDC_CFG_GBL_2.enable. After enabling, it takes time for the output TDC clock to stabilize. Output TDC is ready for use when in Ready state. 0 = Disabled 1 = Initializing 2 = Ready

Once the output TDC instance's configuration is set, it must be manually triggered ("Go") to start (see Table 13 and Step 10 of Figure 7). There must be a minimum 1 second delay between the configuration being set and the trigger. The trigger must be the last register written for a particular TDC.

Table 13. Output TDC Trigger Register

GO	R/W	0	Start or stop output TDC operation. Write 1 to start output TDC operation. SCSR_OUTPUT_TDC0_STATUS.status can be used to check operational status. For 'type' = single shot, when the operation is complete, 'go' will be cleared to 0 and SCSR_OUTPUT_TDC0_STATUS.status will be set to 'Idle' on success and an error status on failure. For 'type' = continuous, on success, 'go' will not be cleared and the operation continues until user clears 'go' or an error is encountered i.e. 'go' will be automatically cleared). 0 = stop output TDC operation 1 = start output TDC operation

The status of the TDC measurement can be monitored to see if the current measurement is valid (i.e., complete).

Table 14. Output TDC Status Register

STATUS[3:0]	R/O	0	Status code. When output TDC is not enabled, this shows 'Disabled'. When OUTPUT_TDC_CTRL_4.GO is set and the configuration is valid, this transitions to 'In progress'. When the operation completes successfully, status transitions back to 'Idle' and OUTPUT_TDC_CTRL_4.GO will be cleared. When OUTPUT_TDC_CTRL_4.GO is set and there is an invalid configuration, then OUTPUT_TDC_CTRL_4.GO will be cleared and this will indicate the error condition encountered. 0 = disabled 1 = idle 2 = in progress 3 = error - invalid source/target 4 = error - non-uniform master divider freq 5 = error - start failed 6 = error - measurement timeout

Average Phase Measurement

As previously mentioned, the output TDC was designed for a single measurement. To improve the precision of the measurement result, a number of samples can be taken (i.e., averaged) instead of relying on a single measurement. By default, 4096 samples are taken and averaged. To take a single measurement, set SAMPLES[15:0] = 1 (see Table 15 and Step 8 of Figure 7).

Table 15. Output TDC Samples Register

Bit Field Name	Field Type	Default Value	Description
SAMPLES[15:0]	R/W	0	Unsigned 16-bit value indicating the number of samples to use for measurement. 0 = 4096 samples. When using more than one sample, the final measurement is an average.

Each sample is taken every 100 microseconds, with the final averaged result being placed in the PHASE[47:0] register (i.e., after (SAMPLES[15:0] * 100 microseconds)). To determine if the measurement sample has completed, the VALID bit should be checked.

Continuous Phase Measurement

The TDC can be configured to continuously take phase measurements, which will just repeat the single phase measurement settings (see Table 16 and Step 6 of Figure 7).

Table 16. Output TDC Type Selection Register

TYPE	R/W	0	Type of output TDC operation, single shot or continuous. In single shot mode, collect the number of samples (average if necessary) and clear 'go' when completed. The continuous mode is the same as single shot mode, except the operation will be repeated continuosly. To stop operation, clear 'go'. 0 = single shot 1 = continuous

In the case of continuous measurement when doing average phase measurements, averaging will still be performed only on the measurement values taken within the programmed sample window. Thus, the phase measurement register will reflect the [averaged] value of the *previous* sample window when the VALID bit is set.

Automatic Output Alignment

In addition to phase measurements, the output TDC provides a means to auto-align the outputs of two or more DPLL channels. This is for channels that are frequency synchronized or syntonized to the source DPLL channel, either by locking to the internal feedback clock or syntonized via the Combo Bus (see Table 17 and Step 5 of Figure 7). When alignment mode is selected, the target reference in Step 4 becomes unused.

Table 17. Output TDC Mode Register

MODE	R/W	0	Select mode of output TDC operation. Measurement mode takes the number of samples, averages it, and then stores it in OUTPUT_TDC0_MEASUREMENT. Auto alignment mode aligns the destinations in 'align_dest_mask' to 'source_index'. 0 = measurement 1 = auto align

The target phase offset for alignment is set via a configuration register, supporting a range of ±1.28ns in 10ps granularity. The resolution of the alignment will be determined by the configuration of the TDC measurement unit, but will be ≤ ±50ps (see Table 18 and Step 9 of Figure 7).

Table 18. Output TDC Target Offset Register

Bit Field Name	Field Type	Default Value	Description
TARGET_PHASE_OFFSET[7:0]	R/W	0	Target phase offset for alignment operation. In units of 10 picoseconds.

More than one DPLL channel can be aligned to the source DPLL. This is set via a destination DPLL configuration register (see Table 19 and Figure 8).

Table 19. Output TDC Alignment Mask Register

Bit Field Name	Field Type	Default Value	Description
ALIGN_DEST_MASK[7:0]	R/W	0	Used in alignment mode to indicate single or multiple DPLL to align with 'source_index'. Auto align DPLL destination mask index. In auto align mode, each set bit will be used as 'dest_index' for DPLLs to be auto aligned with 'source_index' DPLL. Bit 0 corresponds to DPLL 0, bit 1 DPLL 1, etc. 0b00000001 = DPLL 0 0b00000011 = DPLL 0 and DPLL 1

Figure 8. Output TDC Alignment Mask

For questions related to device configurations, please contact Renesas technical support.

Revision History

Revision Date	Description of Change
November 9, 2021	▪ Updated the second paragraph after Figure 3 ▪ Completed other minor changes
July 13, 2021	▪ Added a new section, Settling Time
September 2, 2020	▪ Updated Time-to-Digital Converter (TDC), Finer Measurement Resolution, and Fine Measurement Example ▪ Added a new section, Accuracy vs Precision
August 28, 2018	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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