Application Note

Capacitive Charge Pump using GreenPAK

AN-CM-243

Abstract

This application note presents how to make a capacitive charge pump using a GreenPAK IC and just a couple of low cost external components. A single stage charge pump may be configured as a voltage doubler or voltage inverter. The charge pump operates wit h input voltages 1.8 V to 5 V and load currents up to 145 mA. Overall performance peaks at input voltages 3 V to 5 V and output currents 1 mA to 5 mA when using Schottky external diodes. The main advantage of GreenPAK solution is the flexibility to shift the design focus to the high priority requirement, whether it is low quiescent power, low output ripple, high efficiency/low losses, low EMI or digital control.

This application note comes complete with design files which can be found in the References section.

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1 Terms and Definitions

BOM	Bill of materials
CMOS	Complementary metal oxide semiconductor
DFN	Dual-flat no-leads
DUT	Device under test
EIA	Electronic industries alliance
EMI	Electromagnetic interference
ESR	Equivalent series resistance
GPIO	General purpose input output
I^2C	Inter-integrated circuit
IC	Integrated circuit
IoT	Internet of things
LUT	Lookup table
MELF	Metal electrode leadless face
MLCC	Multi-layer ceramic capacitor
MOSFET	Metal oxide semiconductor field effect
NFET	transistor N-channel field effect transistor
PFET	P-channel field effect transistor
RDS_{ON}	Resistance drain-source while FET is ON
SOD	Small outline diode
SOT	Small outline transistor
SPI	Serial peripheral interface

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks withinthe IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics

[2] AN-CM-243 Capacitive Charge Pump using GreenPAK.gp, GreenPAK Design File, Renesas Electronics

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3 Introduction

Many battery-powered applications in the IoT market require additional voltage levels for powering specific interface circuits, sensors etc.

This application note presents how to make a capacitive charge pump using a GreenPAK™ IC and just a couple of low cost external components. A single stage charge pump may be configured as a voltage doubler or voltage inverter. Multistage charge pumps enable higher output voltages, both positive (voltage tripler, quadrupler etc) and negative (inverting doubler, tripler etc). The output of the circuit is a voltage source that is dependent upon the input voltage level. The maximum output current is in the milliamps range.

The GreenPAK power supply voltage is used as the charge pump input and the GreenPAK outputs a driving signal for the external pump capacitor. Control signals are optional to start/stop (power down) the charge pump or to control wake/sleep timing. Control signals can be digital signals wired to GreenPAK IO pins or serial communication commands.

One GreenPAK
IC can control multiple charge pumps with various output voltages. In the case of low input voltages, GreenPAK s may be cascaded to obtain a higher output voltage with fewer external components. Basic inverter and doubler circuits provide no output voltage regulation. The basic diagrams are shown in Figure 1.

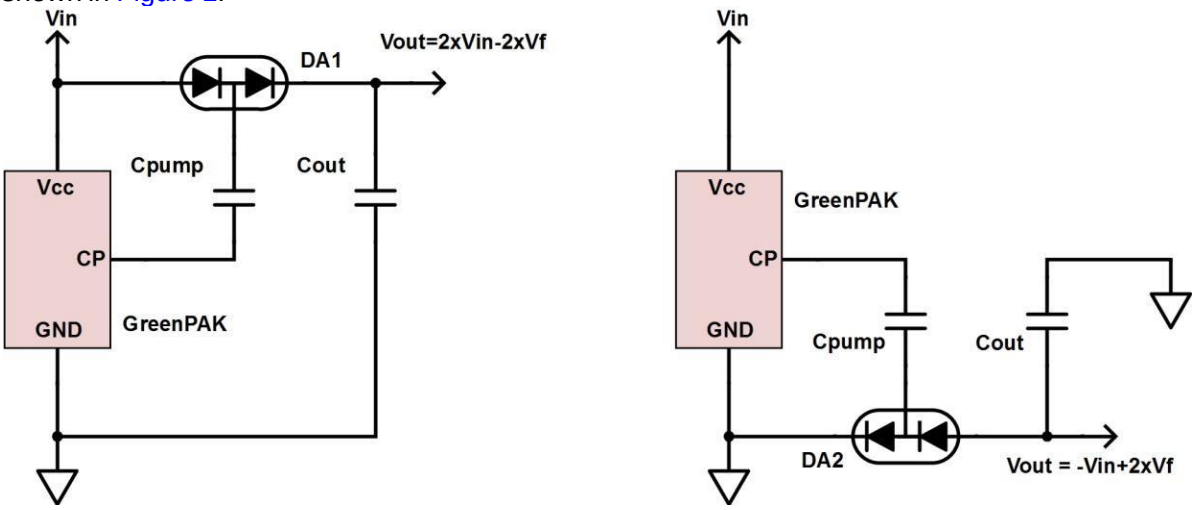

Figure 1: GreenPAK Based Capacitive Charge Pump Voltage Doubler and Voltage Inverter

3.1 Charge Pump Circuit Implementation

The charge pump implementation starts from a project's requirements. Basic requirements include: input voltage range (V_{INMIN} to V_{INMAX}), output voltage range (V_{OUTMIN} to V_{OUTMAX}), and maximum output current V_{OUTMAX}. Nominal examples for this can be 3.0 V to 3.6 V for the input, 4.5 V to 5.5 V for the output, and a 3-mA output current.

Minimum Input voltage V_{INMIN} – The power supply voltage of your GreenPAK at the lowest voltage value. For typical power supply voltages (5 V, 3.3 V or 1.8 V) the minimum voltage will be -10 % or - 5 % below the nominal value (4.5 V, 3 V and 1.71 V). For battery-supplied circuits the minimum input voltage will be the battery over discharge protection threshold; for lithium polymer (LiPo) batteries this is usually 2.5 V. In this application note, we will work within the GreenPAK power supply voltage ranges of 1.8 V to 5 V. Minimum input voltages must be above the GreenPAK operating supply voltage limit of 1.71 V.

Minimum Output voltage V_{OUTMIN} – The charge pump output, which may be positive (voltage doubler) or negative (inverter). Output voltages should not fall below this value at the minimum input voltage and full load (maximum output current).

Maximum Output current I_{OUTMAX} – The maximum average output current that the charge pump should supply to the output. In this application note, we will work with output currents up to 10 mA.

Maximum Input voltage V_{INMAX} – The power supply voltage of your GreenPAK at its highest value. For usual power supply voltages of 5 V, 3.3 V and 1.8 V the maximum voltage will be + 10 % or + 5 % above nominal; 5.5 V, 3.6 V and 1.89 V. For battery-supplied circuits the maximum input voltage will be the battery charging threshold; for LiPo batteries it is usually 4.3 V. Any maximum input voltage must not exceed the GreenPAK operating supply voltage limit of 5.5 V.

Maximum Output voltage V_{OUTMAX} – The output voltage should never exceed this limit at maximum input voltage and zero load (no output current). A GreenPAK voltage doubler can't deliver more than 10 volts at the output, so in applications where the limit is above 10 V, such as driving the gate of a power MOSFET, this requirement is irrelevant. In applications such as powering low voltage loads it may be critical.

Optional requirements

Voltage ripple limit V_{RIPPLE} – The peak to peak value. A charge pump produces triangular ripple on the output because of the periodic charge and discharge of the output capacitor. If the requirement is unknown, take 1 % of output voltage as a nominal value. For example, at 5 V output, 1 % is 50 mVpp. Usual values are 20 to 50 mVpp.

Power down control – A signal to enable/disable the output and to shut down the load and save quiescent power. This requirement is optional: if power down control is not required it will not be implemented and the charge pump will be active all the time.

Power Conversion Efficiency P_{EFF} – The ratio of output power delivered to the load to input power taken from the power supply. May be critical for low power applications.

Maximum Quiescent current I_{QSC} – The charge pump input current at zero load while the IC is active (not turned off). This may be critical for low power applications. If unknown, take 5 % of maximum output current. For example, at 3 mA output, 5 % is 0.15 mA. GreenPAK IC's are known for their low quiescent power consumption, many of which can even operate in the sub-µA quiescent current ranges when properly configured.

3.2 Charge Pump Circuit Operation

The operation of the circuit focuses on charging and boosting capacitors. During the charging phase, the GreenPAK pulls the driving output pin low and charges the pump capacitor to Vcc-Vol. D_1 is on while D_2 is off. During the boosting phase, the GreenPAK pushes the driving output high and the pump capacitor discharges to the output capacitor. D_1 is off and D_2 is on. During both stages the output capacitor is constantly being discharged into the load.

For this application note we will assume that capacitors are 1 µF or more and have low ESR, so we will consider the contribution of ESR to the Rout negligible. We will also assume the diodes are low power, high speed, low cost, small size diodes, so we will consider the switching losses also negligible.

In a voltage doubler circuit, if the load current continuously increases, the output voltage drops and at some point, reaches the input voltage, rendering the charge pump useless. At light loads, the output voltage drops quickly because of high dynamic resistance R_{DD} of the diodes. At high loads, R_{DD} is low and the charge pump output resistance becomes practically load independent.

$V_{OUT} = 2 * V_{IN} – 2 * V_D$ @ $2*I_{OUT} – R_{OUT}* I_{OUT}$

At zero load current and max input voltage the output voltage will reach its maximum value:

$$V_{OUTMAX} = 2 * V_{INMAX} – 2 * V_{D0}$$

Vd0 is roughly 0.4V for standard silicon diodes and below 0.2V for Schottky diodes. The voltage drop is dependent upon the necessary current running through the diode.

At max load current and min input voltage the output voltage will reach its minimum value:

$$V_{OUTMIN} = 2 * V_{INMIN} – 2 * V_D @ 2 * I_{OUTMAX} – R_{OUTMAX} * I_{OUTMAX}$$

Output voltage ripple increases with an increasing load current. It is negligible at zero load and reaches its maximum value at full load:

$$V_{RIPPLE} \approx 2 * I_{OUT} * ESRC_{OUT} + I_{OUT} * (1-D) * T / C_{OUT} \approx I_{OUT} / (2 * F_{OSC} * C_{OUT})$$

$$V_{RIPPLEMAX} = I_{OUTMAX} / (2 * F_{OSC} * C_{OUT})$$

The charge pump output resistance presents an equivalent of all resistive losses in the circuit:

$$R_{OUT} \approx 2 * (R_{SWH} + R_{SWL}) + 1 / (F_{OSC} * C_{PUMP}) + 4 * ESRC_{PUMP} + ESRC_{OUT}$$

Where R_{SWH} and R_{SWL} are the resistances of the output stage of GreenPAK pins used to drive the pump capacitor high (R_{SWH}) or low (R_{SWL}). R_{SWH} is higher than R_{WL} and both are dependent upon voltage, current and temperature. R_{SW} drops with supply voltage, raises with pin current and raises with temperature. It will reach its max value, R_{SWXMAX}, at V_{INMIN} and I_{OUTMAX}:

$$R_{OUTMAX} \approx 2 * (R_{SWHMAX} + R_{SWLMAX}) + 1 / (F_{OSC} * C_{PUMP})$$

4 Charge Pump Circuit Design

Forward biased diodes exhibit a static forward resistance R_D, defined as the ratio of DC voltage applied across diode V_{FWD} to determine the DC current flowing through the diode I_{FWD}. Diode resistance contributes to charge pump output resistance like any other resistance along the current path. At low charge pump output currents I_{OUT} < ~1 mA, diode resistance dominates a charge pump's output resistance. For small changes in forward voltage/current diode exhibits dynamic forward resistance R_{DFD}. Dynamic forward resistance is defined as the ratio of change in voltage to the change in current.

Both static and dynamic forward resistances of small signal diodes are high at low currents and drop fast as forward current increases. Roughly estimated $R_D[\Omega] = 600 / I_{FWD}$ [mA] and

R_{DFD} [Ω] = 40 / I_{FWD} [mA] for silicon diodes while R_D [Ω] = 300 / I_{FWD} [mA] and R_{DFD} [Ω] = 25 / I_{FWD} [mA] for Schottky diodes.

Static and dynamic forward resistances and R_{OUT} contributions are shown in Table 1. Note that the diode current is always double the charge pump output current when the diode is on, so R_D @ I_{FWD} = 2 I_{OUT} is approximately half of what it would be @I_D=I_{OUT}.

Table 1: Diode Parameters and Their Influence on R_{OUT} and V_{OUT}

I_{FWD} or I_{OUT} D = silicon	0.1 mA	0.2 mA	0.5 mA	1 mA	2 mA	5 mA	10 mA
V_{FWD}@I_{FWD} D=silicon (BAV99)	0.5 V	0.53 V	0.57 V	0.6 V	0.64 V	0.68 V	0.72 V
R_D@I_{FWD} Rd=V_{FWD}/I_{FWD}	5 kΩ	2.65 kΩ	1.14 kΩ	600 Ω	320 Ω	136 Ω	72 Ω
R_{OUT} contribution@I_{OUT}	10.6k Ω	4.56k Ω	2.4k Ω	1280 Ω	544 Ω	288 Ω	152 Ω
V_{OUT} contrib@I_{OUT} D=silicon	1.06 V	1.14 V	1.2 V	1.28 V	1.36 V	1.44 V	1.52 V
R_{DFD}@I_{FWD} R_{DFD}=dV_{FWD}/dI_{FWD}	300 Ω	133 Ω	60 Ω	40 Ω	13 Ω	8 Ω	4 Ω

I_{FWD} or I_{OUT} D = Schottky	0.1 mA	0.2 mA	0.5 mA	1 mA	2 mA	5 mA	10 mA
V_{FWD}@I_{FWD} D=Schottky (BAT54)	0.22 V	0.24 V	0.26 V	0.28 V	0.3 V	0.32 V	0.35 V
R_D@I_{FWD} Rd=V_{FWD}/I_{FWD}	2.2 kΩ	1.2 kΩ	520 Ω	280 Ω	150 Ω	64 Ω	35 Ω
R_{OUT} contribution@I_{OUT}	4.8 kΩ	2.5 kΩ	1.1 kΩ	600 Ω	256 Ω	140 Ω	75 Ω
V_{OUT} contrib@I_{OUT} D=Schottky	0.48 V	0.52 V	0.56 V	0.6 V	0.64 V	0.7 V	0.75 V
R_{DFD}@I_{FWD} R_{DFD}=dV_{FW}/dI_{FW}	200 Ω	66 Ω	40 Ω	20 Ω	10 Ω	6 Ω	3 Ω

This is further illustrated in Figure 2, which shows the output resistance vs load current graph for charge pumps with silicon or Schottky diodes measured on a real circuit. The dashed lines show the output resistance of a charge pump when all other resistances in the circuit are negligible (ideal case). For R_{OUT} contributions not mentioned in Table 1, please refer to Figure 2. The graph shows that at low load currents, diode resistance is high and dominates in R_{OUT}. Reducing other resistances in the charge pump circuit yields negligible gains. At high load currents the diode resistance becomes a minor contributor and considerable performance gains are achievable by altering other circuit parameters, such as reducing switch resistance and adjusting operating frequency.

Generally, R_{SW} for GreenPAKs tend to be between 20 Ω and 40 Ω per pin and can be reduced by paralleling driving pins. 8 pins wired together will yield R_{SW} between 2.5 Ω and 5 Ω. Equivalent switch resistances and R_{OUT} contributions for various pin mode options are shown in Table 2. 1x stands for "1x push pull" output mode, while 2x stands for "2x push pull" output mode. The number after "x" denotes the number of paralleled pins. For example, 2x2 stands for 2 pins in "2x push pull" mode wired in parallel. Note that Table 2 shows only 1, 2, 4 and 8 pins in parallel, while it is possible to wire any number of pins in parallel, up to available GPIO pins on selected GreenPAK. Values shown are for the 3 V to 5 V supply voltage range. For detailed data please refer to section "GreenPAK design" of this app note.

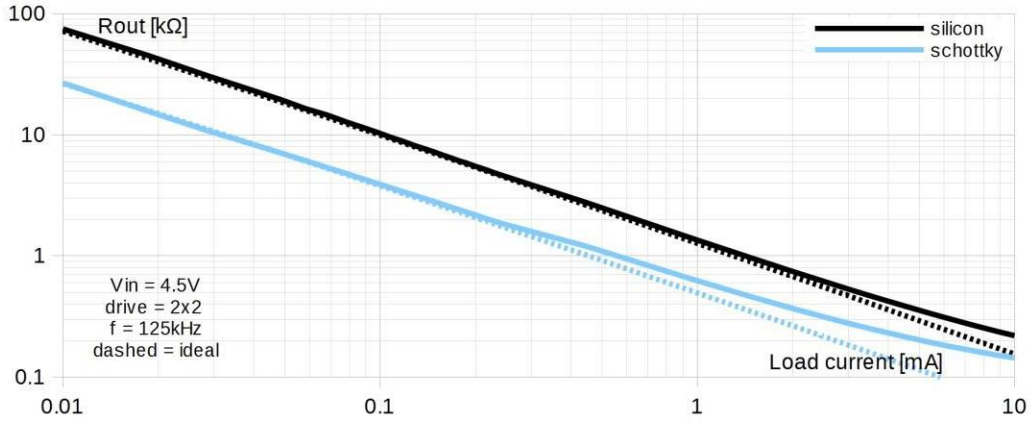

Figure 2: Diodes Contribution to Output Resistance

Table 2: Internal Switch Resistance Range

Pin Configuration	1 x 1	2 x 1	2 x 2	2 x 4	2 x 8
R_{SW} equivalent	40 Ω.. 80 Ω	20 Ω..40 Ω	10 Ω..20 Ω	5 Ω..10 Ω	2.5 Ω.. 5 Ω
R_{OUT} contribution	160 Ω.. 320 Ω	80 Ω..160 Ω	40 Ω..80 Ω	20 Ω..40 Ω	10 Ω.. 20 Ω

R_{CP} = 1 / F_{OSC} C_{PUMP} is the equivalent resistance of the charge pump circuit and can be reduced by increasing C_{PUMP} capacitance or by increasing the operating frequency. With high quality capacitors, such as a ceramic X7R, it is usually better to increase C_{PUMP} capacitance because increasing frequency increases switching losses and EMI. MLCC 1 µF capacitors are widely available in an EIA 0402 package (1.0 mm x 0.5 mm) with 6.3 V or 10 V voltage rating, priced below 0.5 ¢/pcs in

production quantities. If board space is a major concern, you can get 1 µF MLCC in a 0201 package (0.6 mm x 0.3 mm) at a slightly higher cost.

Going below a 1 µF capacitance value typically gains no significant reduction in size or cost of capacitors, so this application note uses 1 µF as default capacitance for both the pump capacitor and the output capacitor. As a quick reference the R_{OUT} contribution of the equivalent resistance of the charge pump circuit with 1 µF capacitors at various operating frequencies is shown in Table 3 below.

Table 3: Suitable Operating Frequencies

Operating Frequency [kHz]	12.5	25	31.25	62.5	125	250
$R_{CP} = 1 / F_{OSC}C_{PUMP}$, C_{PUMP} = 1 µF	80 Ω	40 Ω	32 Ω	16 Ω	8 Ω	4 Ω
OSC configuration predivider/second divider	25 kHz/2/1	25 kHz/1/1	2 MHz/8/8	2 MHz/8/4	2 MHz/8/2	2 MHz/8/1

4.1 Design Procedure

Step 1) The circuit design needs to assure that V_{OUTMIN} is within limits. Knowing V_{INMIN} and I_{OUTMAX}, we can calculate the budget for R_{OUTMAX}:

$$R_{OUTMAX} = (2 * V_{INMIN} – 2 * V_D @ I_{OUTMAX} – V_{OUTMIN}) / I_{OUTMAX}$$

$V_D@I_{OUTMAX}$ is available on the diode datasheet. Just make sure you read V_D at 2 * I_{OUTMAX} because the diode forward current is twice the output current. For a quick estimate, use Table 1 below. For example, V_{INMIN} = 3.0 V, V_{OUTMIN} = 4.5 V, I_{OUTMAX} = 1 mA, D = 4148 yields:

$$R_{OUTMAX} = (6.0 V – 1.28 V – 4.5 V) / 1 mA = 220 Ω$$

Now, select the pin configuration and operating frequency such that:

$$4 * R_{SW} + 1/ F_{OSC} * C_{PUMP} < R_{OUTMAX}$$

In our example R_{OUTMAX} is 220 Ω. Reading Table 2 and Table 3, 2 x 1 (single pin double drive) and 25 kHz make R_{OUTMAX} = 200 Ω < 220 Ω. To add some margin, if another GreenPAK GPIO pin is available, select 2 x 2 (2 pins double drive) and 25 kHz, making R_{OUTMAX} = 120 Ω.

If the R_{OUTMAX} budget is too small, pick a diode with a lower forward voltage drop, such as a Schottky. If that doesn't help, then you probably can't meet your requirements with a voltage doubler circuit and you need a different circuit, such as a voltage tripler. In the example above, if V_{OUTMIN} was 4.75 V instead of 4.5 V, R_{OUTMAX} would be -10 Ω, so silicon diodes would not be applicable. Using a Schottky diode, R_{OUTMAX} = (6 V – 0.6 V – 4.75 V) / 1 mA = 650 Ω.

Step 2) Check if output voltage ripple is in bounds:

$V_{RIPPLEMAX} = I_{OUTMAX} / (2 * F_{OSC} * C_{OUT}) = 1 mA / (2 * 25 kHz * 1 µF) = 20 mVpp$

if needed, reduce ripple by increasing output capacitance C_{OUT} or by increasing the switching frequency. Higher frequencies will lower output resistance and shorten startup time, but will also increase switching losses and quiescent current. If ceramic multilayer capacitors are used, increasing C_{OUT} will marginally improve output resistance and will not affect switching losses or quiescent current, but it will increase startup time.

Step 3) Check if V_{OUTMAX} is within limits (if specified):

$$V_{OUTMAX} = 2 * V_{INMAX} – 2 * V_{D0} = 2 * 3.6 V – 2 * 0.4 V = 6.4 V$$

In our example, V_{OUTMAX} should be below 5.5 V, so to meet this requirement we need to reduce V_{OUTMAX}. One way to do it is by adding a linear regulator to the charge pump output. The charge

pump can also be shut down though use of a GreenPAK ACMP block that is set to the desired output voltage.

4.2 Quick and Easy Design in Three Simple Steps

In this quick & easy design procedure we use dynamic forward resistance to quickly find suitable options for pin configuration and operating frequency. Use this design procedure to quickly estimate if your requirements can be effectively met by a GreenPAK charge pump solution.

Start with $C_{PUMP} = C_{OUT} = 1\mu F$ X7R, D = silicon

Step 1) estimate R_{DFD} for selected diode type at maximum I_{OUT};
for example, at $I_{OUT} = 1$ mA, $R_{DFD} = 40 / 1 = 40\ \Omega$ or read from Table 1

Step 2) select pin configuration from Table 2 to match R_{SW} and R_{DFD}: 2 x 1 = 20..40 Ω

Step 3) select frequency from Table 3 to match R_{CP} and R_{DFD}: F_{OSC} = 25 kHz $R_{CP} = 40\ \Omega$

Step 4) If needed, increase C_{OUT} to meet ripple specs.

4.3 Operating Frequency Selection

Commercial charge pump ICs usually operate at a fixed frequency. GreenPAK integrated oscillators, frequency predividers/dividers and counter blocks enable a user to set almost any desired operating frequency. Careful choice of operating frequency brings performance benefits such as low ripple, high efficiency, low quiescent current and reduced emissions.

The higher the frequency, the shorter the period between two pumps and the smaller amount of charge you need to pump during each period. Operating frequency directly affects the size of capacitors and startup time but also the losses in the circuit, such as switching losses in rectifiers and the quiescent current of the charge pump circuit.

If you want to keep the circuit as small as possible, go for high operating frequency. If you want to keep the quiescent current as low as possible, go for low operating frequency.

GreenPAKs offer various options for operating frequency, depending upon the part selected. Base frequencies range from the LF oscillator at around 2 kHz to the Ring oscillator at 25 MHz or 27 MHz. Other frequency options are possible using clock predividers or additional CNT/DLY blocks. To keep the GreenPAK block complexity at a minimum, the best option is to select one of the available oscillator blocks and use the internal clock predivider/divider. Using only these blocks, the only available option for a duty cycle is 50 %. Note that for some divider options, those that include a factor of /3, clock duty cycle may not be 50 %.

Ring oscillator frequencies of 25 MHz or 27 MHz are too high for charge pump operation. LF OSC frequencies are too low and they cut deep into audible spectrum, so they are not suitable either, except maybe for very special requirements like tiny output powers and extremely low quiescent current.

4.4 Capacitors Calculation and Selection

Capacitors are the main energy transfer component of the charge pump circuit. Sizing and selection of capacitors for a charge-pump circuit directly affects overall charge pump performance.

Class 2 surface mount multilayer ceramic capacitors MLCC with X7R or similar dielectrics are suitable for charge pumps because of their small size, low cost, very low ESR, low leakage and good temperature stability. They can provide capacitance up to 10 µF at competitive cost; more than adequate for charge pumps that can be realized with GreenPAKs. Tantalum and aluminum

electrolytic capacitors are not suitable because of their high ESR, bigger size and higher cost. Low-ESR electrolytic capacitors are available, but they are also inferior to MLCC.

Ceramic capacitors with a Y5V, Z5U or similar dielectric are not suitable for use in charge pump applications because of their poor stability. Although they provide higher initial capacitance than the X7R type, they exhibit wide capacitance tolerance and vary significantly with temperature and applied voltage. A Z5U capacitor may decline to between 10 % to 20 % of its nominal value in certain conditions, so you may need to select a 4.7 µF capacitor instead of 1 µF.

Capacitor Class 1 with NP0, COG or similar dielectrics exhibit smaller capacitance values, bigger size and higher cost than X7R, so they are not the first choice for general charge pump applications. They feature higher stability and lower ESR than X7R. Consider Class 1 capacitors for delicate applications and high operating frequencies.

The most important factors that cause capacitance to deviate from its nominal value are initial tolerance, temperature, applied voltage, frequency dependence and aging. Usual ΔC/C worst case values are presented in Table 4.

Table 4: Capacitance Change ΔC/C

Cause	Class 2 (X7R, X5R)	NP0, COG
Initial tolerance	±5 %, ±10 %, ±20 %	±0.5 % .. ±5 %
Temperature -50 °C .. +85 °C	±15 %	±0.5 %
Applied voltage	-3 % @ 50 % Vr, -6 % @ 75 % Vr, -10 % @9 0 % Vr	negligible
Frequency	-3 % @ 10 kHz, -6 % @ 100 kHz, -10 % @ 1 MHz	negligible
Aging -2.5 % per decade hour	~10 % @ 1 year, ~15 % @ life (100 yrs)	negligible
Total	-25 % .. -50 %	-1 % .. -5 %

Capacitance decreases with increased temperature, operating voltage, frequency and age. This degradation results in lower capacitance than expected and higher ripple voltages and currents. Total capacitance degradation for X7R dielectric may range from -25 % for a ±5 % capacitor in convenient conditions to -50 % for a ±20 % capacitor at high temperature, high frequency and low voltage margin at the end of service life. For other types of dielectric figures differ – for Z5U or Y5V total degradation may be -90 % or more.

Selecting capacitors with lower initial tolerance and with a rated voltage significantly above the operating voltage minimizes capacitance degradation.

When using capacitors with a Class 2 dielectric, check the spec of the capacitor to make sure your design will meet specifications. For quick reference, add 50 % to calculated capacitance value to account for total degradation.

4.5 Output Capacitor

Output capacitance C_{OUT} must be high enough to keep output ripple within limits at all working conditions. On the other hand, we want to pick a smaller value capacitor to keep the circuit size small. The minimum value for an output capacitor is calculated according to formula:

$$C_{OUTMIN} = I_{OUT} * D * T / V_{RIPPLE}$$

In this application note we use a duty cycle of D=50 %, so:

$$C_{OUTMI} = I_{OUT} / (2 * F_{OSC} * V_{RIPPLE})$$

For example, at I_{OUT} = 1 mA, V_{RIPPLE} = 20 m V, F=25 kHz, D = 50 %:

C_{OUTMIN} = 1 mA / 2 * 25 kHz * 20 m V = 1 µF

When substituting the value for F_{OSC}, the designer should check the frequency tolerance and choose a minimum frequency across the full temperature range, instead of using the nominal value. In the example above, a 25 kHz clock may vary in mass production up to 21.905 kHz, so C_{OUTMIN} will be 1.14 µF instead of 1 µF.

Add 30% to 100% to account for capacitance degradation and round up to the next available value; for the example above that would be C_{OUT} = 2.2 µF.

Figure 3 shows measured values of output peak-to-peak ripple against load current at four characteristic operating frequencies. Output and pump capacitors are 1 µF each. Measurements show that output ripple is not dependent on the type of diodes in the circuit (silicon or Schottky), nor dependent on the input voltage level or the GreenPAK internal switch resistance (pin configuration). To be accurate: ripple dependency on these characteristics is negligible. That's because, during the charging phase, the output diode is off, and the output capacitor is the only component connected to the load. Ripple raises with load current and falls with operating frequency in a linear fashion.

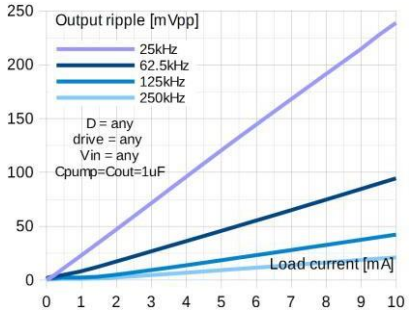

Figure 3: Output Ripple vs Load Current

For the voltage doubler the maximum voltage on the output capacitor is at zero load:

$V_{OUTMAX} = 2 * V_{INMAX} – V_{D10} - V_{D20}$

For the voltage inverter, maximum voltage on the output capacitor is again at zero load:

$V_{OUTMAX} = V_{INMAX} – V_{D10} - V_{D20}$

MLCC capacitors are available with voltage ratings 4 V, 6.3 V, 10 V and 16 V. Add 20 % margin to V_{OUTMAX} above and select capacitors with first voltage rating covering that value. For our voltage doubler example, for V_{INMAX} = 3.6 V and Schottky diodes, V_{OUTMAX} = 6.8 V, 20 % margin makes V_{OUTMAX} 8.16 V, so a 10 V rated capacitor is the right choice.

4.6 Pump Capacitor (Flying Capacitor) Selection

Ripple voltage on the pump capacitor

$V_{RIPPLECP} = 2 * I_{OUT} * D * T / C_{PUMP} + I_{OUT} * ESRC_{PUMP}$

In this application note we use a duty cycle D = 50 % and neglect ESR, so:

$V_{RIPPLECP} = I_{OUT} / F_{OSC} * C_{PUMP}$

For $C_{PUMP} = C_{OUT}$, and a duty cycle D = 50 %, ripple on the pump capacitor will be double the output ripple.

One approach for sizing the pump capacitor is to leave enough ripple to cover load transients. A rule-of-thumb for this approach is to design ripple at 100 mV to 500 mV or 5 % to 10 % of capacitor voltage. In our example VC_{PUMP} = 3 V, $V_{RIPPLECP}$ = 160 mV:

$C_{PUMP} = I_{OUT} / F_{OSC} * V_{RIPPLECP}$ = 1 mA/ 25 kHz * 160 mV = 250 nF

This approach may introduce relatively large output resistance $R_{CP} = 1 / F_{OSC} C_{PUMP}$, in our example $R_{CP} = 1 / 25$ kHz * 250 nF = 160 Ω. Increasing C_{PUMP} capacitance reduces output resistance, but also reduces C_{PUMP} ripple and degrades response to load transients, so select the capacitance of the pump capacitor to meet your design priorities.

Just like the output capacitor, capacitance of the pump capacitor is subject to degradation by operating voltage, aging and other factors, so add appropriate margins when selecting capacitance. In the example above 250 nF would round up to 330 nF or 470 nF.

Another consideration is cost; a pump capacitor C_{PUMP} is usually kept the same type and value as the output capacitor to reduce the BOM.

For the voltage doubler, the maximum voltage across the pump capacitor is $VC_{PUMPmax} = V_{IN} – V_{D0} - V_{OL}$ or, to simplify the equation by neglecting V_{OL}, $VC_{PUMPmax} = Vi_{INMAX}$. For the inverter circuit, the maximum voltage on the pump capacitor is $VC_{PUMPmax} = V_{OH} – V_{D0}$, again simplified to $VC_{PUMPmax} = V_{INMAX}$. Add 20 % margin to V_{INMAX} and select a capacitor with the first voltage rating covering that value. For our voltage doubler example, for $V_{INMAX} = 3.6$ V, 20 % margin makes 4.32 V so a 6.3 V rated capacitor is the right choice.

4.7 Diode Selection

A single stage charge pump circuit, either a doubler or inverter, requires 2 diodes connected in series. An optimal choice for both size and cost are double diode packages. However, manufacturers usually launch single diodes first to the market and a double diode package may be unavailable. So, if you aim for cutting edge performance, check the single diodes table further in this app note. They come in tiny 3 pin SMD packages like SOT23 and SC-70, both of which are suitable for use with GreenPAK ™s. Popular options are shown in Table 5.

Table 5: Popular Double Diodes

Silicon	V_R	I_{FWD}	V_{FWD}@ 10mA	IL_{MAX}	C_D	t_{RR}	Package (Case)	Cost
BAV99L	100 V	215 mA	855 mV	1 uA	1 pF	6 ns	SOT-23 3 x 2.4	2.5 ¢
BAV99W	100 V	215 mA	855 mV	1 uA	1 pF	6 ns	SOT-323 2.1 x 2.1	3.5 ¢
BAV99T	85 V	75 mA	855 mV	2 uA	1 pF	4 ns	SOT-523 1.8 x 1.8	5 ¢
MBD7000	100 V	200 mA	820 mV	1 uA	1 pF	4 ns	SOT-23 3 x 2.4	2.8 ¢
BAV99QA	90 V	170 mA	855 mV	0.5 uA	1.5 pF	4 ns	DFN1010D 1.1 x 1	5.5 ¢
BAV199	85 V	140 mA	1000 mV	5 nA	2 pF	3 us	SOT-23 3 x 2.4	4 ¢
Schottky	**V_R**	**I_{FWD}**	**V_{FWD}@ 10mA**	**IL_{MAX}**	**C_D**	**t_{RR}**	**Package (Case)**	**Cost**
BAT54SL	30 V	200 mA	400 mV	2 uA	7 pF	5 ns	SOT-23 3 x 2.4	3.8 ¢
RB548W	30 V	100 mA	450 mV	0.5 uA	10 pF		SOT-416 1.6 x 1.6	17.2 ¢
BAT54ST	30 V	200 mA	400 mV	2 uA	10 pF	5 ns	SOT-523 1.8 x 1.8	5.2 ¢
DB3X313F	30 V	130 mA	300 mV	50 uA	10 pF	1.5 ns	SOT-23 3 x 2.4	5.5 ¢
DB3J316	30 V	100 mA	300 mV	15 uA	6 pF	0.8 ns	SC-85 2.1 x 2.0	7.3 ¢
DB3J314	30 V	30 mA	400 mV	0.3 uA	3 pF	1 ns	SC-85 2.1 x 2.0	7.3 ¢
BAS40-04	40 V	200 mA	500 mV	100 nA	5 pF	5 ns	SOT-23 3 x 2.4	8.5 ¢

Table 5 presents main characteristics of selected diodes affecting the circuit performance.

The Reverse Breakdown Voltage V_R must be higher than the output voltage for boosting charge pumps. For inverting charge pumps, it must be higher than $V_{INMAX} – V_{OUTMAX}$. For example, for a 5 V to -5 V inverting charge pump, the Reverse Breakdown Voltage must be higher than 10 V. It is reasonable to add a safety margin of around 20 % and make it 12 V. For silicon diodes, V_R is relatively high, over 50 V, but for Schottky diodes this parameter can be critical because there are ultra-low voltage Schottky diodes on the market with V_R as low as 10 V or less.

Diodes in the charge pump circuit conduct an average current equal to the output current by conducting 50 % of the time at Id = 2 * I_{OUT}. Maximum Forward Current I_{FWD} (DC or average) of each diode must be higher than charge pump output current doubled. Adding 20 % safety margin is a good practice. For example, for 10 mA charge pump output current, select diodes with at least 10 mA * 2 + 20 % = 24 mA maximum forward current.

Forward Voltage V_{FWD} is the source of conducting losses. It reduces the maximum output voltage and charge pump efficiency. Schottky diodes exhibit lower forward voltage drop than silicon diodes at the tradeoff of a lower breakdown voltage and higher price. For easy comparison, forward voltages presented in Table 5 are at 10 mA diodes forward current.

Reverse Leakage Current ILmax is an important parameter at very low output currents and raises drastically at high temperatures. For most diodes, reverse leakage can be neglected at charge pump output currents over 1 mA. However, if you design a charge pump for operation in the microamp range and want to keep the pump and output capacitances as low as possible, you need to consider leakage, especially if the circuit will operate at high temperatures.

C_D is diode reverse capacitance. Values presented are at reverse bias V_R = 1 V. Reverse capacitance drops with reverse voltage. Select low C_D diodes when operating at high frequency.

Reverse Recovery Time t_{RR} can be neglected at low operating frequencies in the kHz range. Long reverse recovery times mean high switching losses. For Schottky diodes and high-speed switching diodes, reverse recover is a couple of nanosecs - the best you can get, so it's ok at high frequencies. Low leakage diodes exhibit reverse recovery time in the microsecond range, which is unacceptable for operating frequencies above 100 kHz.

Packages (Case) are presented in the Table 4 and Table 5 by usual designation, followed by the size of the footprint in millimeters. For detailed package specifications check the relevant datasheets.

Cost shown is approximate cost at production quantities > 1 kpcs. Prices change without prior notice, so refresh this column (or a part of it) when starting a design.

There are design cases where two single diodes are preferred to double diode option. For example, Schottky double diodes are not available in ultra-small DFN packages at a low cost. So, if circuit size is the ultimate concern, two single diodes are the best option. Here is Table 6 presenting single diodes:

Table 6: Popular Single Diodes

Silicon	V_R	I_{FWD}	V_{FWD}@10 mA	IL_{MAX}	C_D	t_{RR}	Package (Case)	Cost
LL4148	75 V	150 mA	750 mV	25 nA	4 pF	4 ns	Mini MELF 3.7 x 1.6	1.7 ¢
BAS16GW	100 V	215 mA	855 mV	30 nA	1.5 pF	4 ns	SOD123 3.7 x 1.7	2 ¢
1N4148WL2	100 V	150 mA	700 mV	25 nA	1.5 pF	4 ns	DFN10062L 1 x 0.6	2.6 ¢
LL3595	125 V	200 mA	800 mV	5 nA	8 pF	3 us	Mini MELF 3.7 x 1.6	5.5 ¢

Silicon	V_R	I_{FWD}	V_{FWD}@10 mA	IL_{MAX}	C_D	t_{RR}	Package (Case)	Cost
Schottky	**V_R**	**I_{FWD}**	**V_{FWD}@10 mA**	**IL_{MAX}**	**C_D**	**t_{RR}**	**Package (Case)**	**Cost**
BAT54GW	30 V	200 mA	400 mV	2 uA	10 pF	-	SOD123 3.7 x 1.7	3 ¢
NSR0530	30 V	500 mA	280 mV	200 uA	10 pF	-	SOD-323 2.5 x 1.2	3.5 ¢
RB520S30	30 V	200 mA	350 mV	2 uA	10 pF	-	SOD-523 1.6 x 0.8	4 ¢
DB2S316	30 V	100 mA	300 mV	15 uA	6 pF	1 ns	SSMini2 1.6 x 0.8	4 ¢
DB2S314	30 V	30 mA	400 mV	0.3 uA	3 pF	1 ns	SSMini2 1.6 x 0.8	4 ¢
RB521S30L2	30 V	100 mA	350 mV	10 uA	19 pF	-	DFN10062L 1 x 0.6	5 ¢

5 GreenPAK Design

The GreenPAK design is simply an oscillator wired to one or more output pins used to drive the pump capacitor. The design procedure comes down to programming the oscillator block and setting the pin parameters. The key to a successful design is selecting the right parameters.

The power down feature is already available on the oscillator block, so it is just wired to the input pin.

5.1 Oscillator Design

Operating frequency is already selected during the external charge pump circuit design, so we just need to set OSC parameters accordingly.

Control pin mode: set to “Power Down” to enable external shutdown of the charge pump.

OSC power mode: set to “Force Power On”, otherwise oscillator might never start in simple design.

Clock selector: set to “OSC” because we want to use internal clock. If your application requires tight tolerance for operating frequency, GreenPAK offers external clock option.

Fast start-up option: enable/disable depending on your application requirements. Disable for lower quiescent current and slower startup, enable for faster startup at higher quiescent current.

- Disable: A few usec to a half cycle delay before OSC0 Starts up.
- Enable: Less start-up delay. Consumes additional power. (700 nA at 5.0 V V_{DD}).

OSC Frequency / predivider / second divider: set according to Table 3. An example for 125 kHz operating frequency is shown in Figure 4.

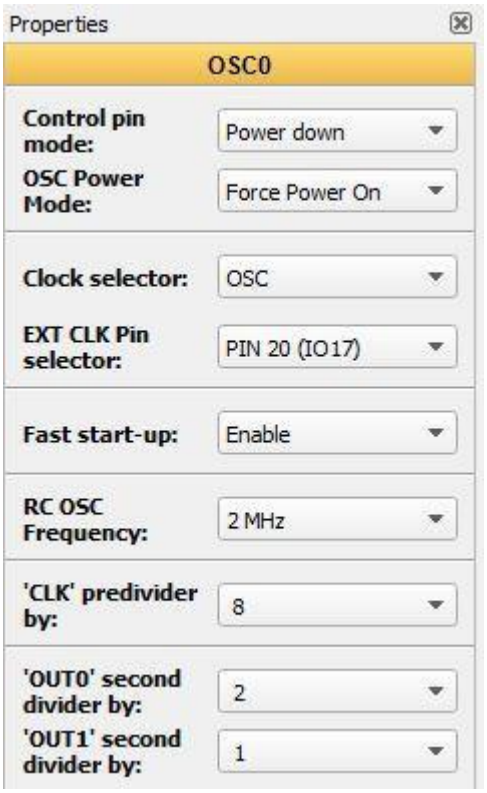

Figure 4: OSC Settings

5.2 Output Pins Design

A charge pump design is based on using output stages of GreenPAK I/O pins as charge pump switches. GreenPAK output structures are CMOS, so when the pin output is low, the NFET connecting the pin to ground is ON. When the output is high the PFET connecting the pin to V_{DD} is ON. Both FETs exhibit RDS_{ON} which causes losses in the charge pump circuit and contributes to charge pump output resistance.

RDS_{ON} is dependent upon supply voltage, pin current and ambient temperature and its initial value is subject to manufacturing tolerance. NFETs and PFETs have different resistances. Dependencies are complex and interrelated. Generally, RDS_{ON} decreases with supply voltage, increases with pin current, and increases with temperature. As a result, switch resistance may range from ~ 20 Ω to almost ~ 100 Ω.

GreenPAK I/O pins can be configured for single or double drive capacity. For the charge pump application, we need the resistance to be as low as possible for better efficiency, so the double drive option is preferred. Typical and worst-case values for I/O pins configured as a double drive push-pull digital output are shown in Table 7.

Table 7: Internal Switches Detailed Characteristics

Power Supply Voltage	5 V ±10 %		3.3 V ±10 %		1.8 V ±5 %	
	typ	max	typ	max	typ	max
NFET resistance R_{SWL}	18 Ω	30 Ω	25 Ω	40 Ω	45 Ω	80 Ω
PFET resistance R_{SWH}	22 Ω	36 Ω	35 Ω	50 Ω	60 Ω	90 Ω
R_{SWL}+ R_{SWH}	40 Ω	66 Ω	60 Ω	90 Ω	105 Ω	170 Ω
Average (R_{SWL}+ R_{SWH}) / 2	20 Ω	33 Ω	30 Ω	45 Ω	52.5 Ω	85 Ω

Typical values are for nominal supply voltages (5 V, 3.3 V or 1.8 V), a pin current of 3-5 mA and room temperature T_A = 25 °C. Max values are for minimum supply voltage (4.5 V, 3.0 V or 1.71 V), high pin current (>10 mA) and high temperature.

For some specific applications, single drive pin configuration might be the right option. To get a rough estimate of the switch resistance in single drive "1x push pull" cases, double the resistances in the table above.

Programming the pins in GreenPAK Designer is easy: just set "I/O selection" to "Digital output" and "Output mode" to "2x push pull".

For charge pump output currents above 5 mA, average drive pin current is above 10mA. The maximum average or DC current (through a pin) is defined in GreenPAK datasheet "Absolute Maximum Conditions" section; it is in 10 mA range. For example, SLG46533 lists 16 mA for "2x push pull" and 11 mA for "1x push pull". Determine your maximum drive current by doubling maximum output current and use enough pins to cover the requirement. For example, at an output current of 10 mA, the pin current will be 20 mA and SLG46533 will need 2 pins in parallel to stay within absolute limits.

Always keep all paralleled pins the same type. Mixing "2x push pull" output mode pins with "1x push pull" or "open drain" output mode pins is a bad idea. Transition times might differ, and pins might end up driving shoothrough current into each other in short pulses. Although this will probably not damage the GreenPAK it will cause additional losses and dramatically raise quiescent current. This effect is load-independent so current will pulse at zero load just like any other load.

For driving the pump capacitor select pin or pins as near as possible to GreenPAKs GND pin and as near as possible to each other. This will ease the PCB layout design and reduce emissions and noise. In the case of paralleled pins, keeping them close will avoid imbalance in circuit parasitics which may cause drive overlap at transitions.

When using multiple pins on GreenPAKs with split internal power rails, share the load over power rails. For example, SLG46533 power rails are divided in two sides. I/O pins 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, and I/O pins 9, 10, 11, 12, 13, 14, 15, 16 and 17 are connected to another. If you use 4 pins to drive a charge pump capacitor, pick 2 pins from each group; for example, IO5+IO8 and IO9+IO10.

Refer to the "Layout Considerations" section of this application note for more info on output pins.

5.3 GreenPAK Design schematic

Figure 5 shows the basic design with only one pin used for drive. One block, two pins, two wires … it doesn't get simpler than that, and it still includes the shutdown feature. Such design simplicity is enabled by GreenPAK's built-in features. The basic design fits into any GreenPAK, including the smallest, lowest cost SLG46108. To increase drive strength, add pins and wire them to OSC output. The design will still fit into any GreenPAK.

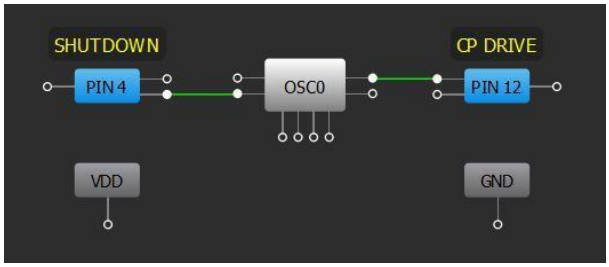

Figure 5: System Diagram

Figure 6 shows the design with 4 pins drive and two shutdown inputs: one directly connected, just like in the basic design and another via I^2C. They are wired through an OR gate so each one can

shut down the charge pump independently. If priority logic for shutdown commands is needed, change LUT0 accordingly. This design requires any of the GreenPAK ICs with I^2C capabilities.

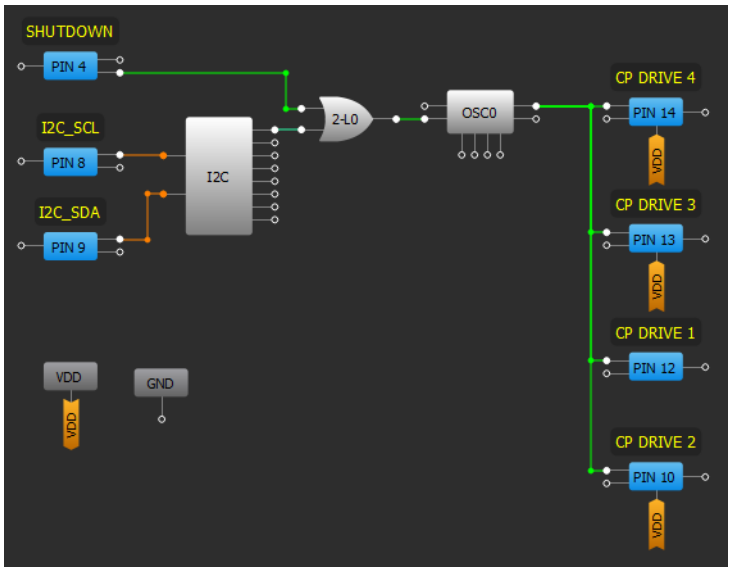

Figure 6: GreenPAK Design with Alternate Shutdown

5.4 Powerdown Feature

The GreenPAK oscillator block features a powerdown input. When the Power down control pin is HIGH, the OSC will turn off and minimize current consumption. Wiring this OSC input to a GPIO pin programed as a “Digital input” enables active-high external shutdown. If active-low powerdown is needed, place a logic inverter gate between the GPIO pin and OSC Power down control.

You can add pull up or pull-down resistors to the shutdown input, if needed: 10 KΩ, 100 KΩ or 1 MΩ are available options. To set the input thresholds, you can program shutdown input for low voltage, standard digital input or Schmitt trigger input.

Note that with the designed presented above, during powerdown of the voltage doubler, the charge pump is not switching but load will be supplied through the forward bias diodes: $V_{OUT} = V_{IN} – 2 * V_{FWD}$, $I_{OUT} = V_{OUT}/ RL$, $I_{IN} = I_{OUT}$. So, the powerdown command will powerdown the charge pump, but it will not powerdown the load and it will not stop the current drawn from input power supply. This may be a problem for some applications. There is no such issue with the voltage inverter, because both diodes are zero biased in powerdown and there is no power on the load.

“Full shutdown” of voltage doubler charge pump requires a small modification to the basic schematic, as shown in Figure 7. Instead of powering the charge pump from the input voltage, wire the input to GreenPAK GPIO pin (or multiple pins) marked CPPS (Charge Pump Power Supply) in Figure 7. The maximum average current through CPPS will be equal to charge pump output current I_{OUTmax}, so use more pins if I_{OUTmax} is high. Set CPPS pin(s) to mode “2x push pull” and drive it from the shutdown input (inverted if needed, depending on the polarity of shutdown input). As a result, the output voltage during shutdown will be zero and input current will be negligible.

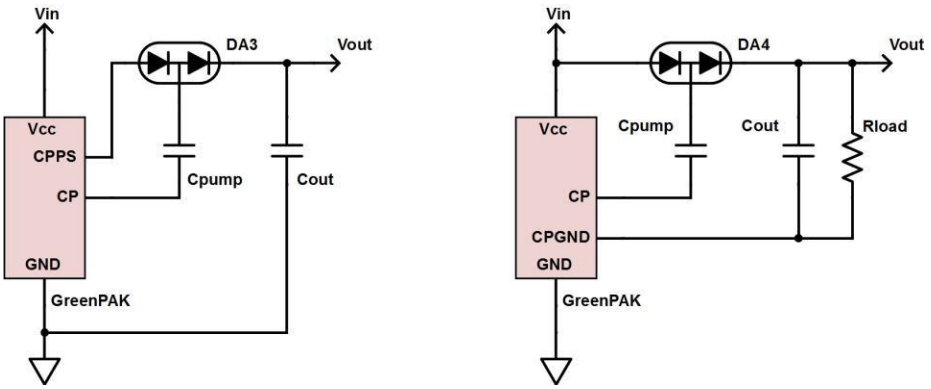

Figure 7: Voltage Doubler with Full Shutdown

The downside of this solution is that charge pump output resistance will increase because new R_{SWH} is introduced in the circuit during the charge phase. That resistance causes power losses in GreenPAK, degrading the GreenPAK power budget. Introduced resistance may be reduced by paralleling pins. Since this pin is not switching like the CP pin, there is no need to worry about transient pulses. If you use a GreenPAK, with integrated PMOS switches like the SLG46116 or SLG46117 you can cut the power supply of the charge pump. In that case, introduced output resistances and power losses will be negligible.

If your load does not have to be ground referenced, you may cut the negative end of the power supply instead of positive, as shown in Figure 7 right side. The advantage of this circuit is that you can use “4x open drain” capable pin(s) for CPGND. They provide more current capacity and add less output resistance than “2x push pull”. On the downside, during shutdown, load will float at the input voltage instead of GND and, during operation, load ground will change potential depending upon the load current. However, “full shutdown” is accomplished: voltage across the load is zero and no current is drawn from input power supply.

6 Circuit Performance

Circuit performance specification: C_{PUMP} = C_{OUT} = 1 µF X7R, D = Schottky,

T_A = 25 °C, F_{OSC} = 125 kHz unless otherwise noted.

Table 8: Circuit Performance Specifications

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Supply Voltage		1.71	---	5.5	V
I_{QSC}	Quiescent current	R_L = ∞, 25 kHz	8	11	14	µA
I_{SHDN}	Shutdown current (Note 1)	SLG46533	0.31	0.57	0.89	µA
F_{OSC}	Oscillator frequency 25 kHz OSC 2 M OSC	selectable (Note 2)	0.048 -3.4% -9.4%	 25 / 2 n 2000 / 2 n	2000 4.7% 14.4%	kHz
I_{OUT}	Output current (Note 3)		5	10	45	mA
R_{OUT}	Output resistance	I_{OUT} = 10 mA	118	-	250	Ω
V_{EFF}	Voltage conversion efficiency	R_L = ∞ (Note 4)	199	199.9	-	%
P_{EFF}	Power conversion efficiency	R_L = 5 KΩ	84	90	92.5	%
V_{TH}	Shutdown input threshold		See Table 8 Table 9 Table 10	V		
T_A	Operating Temperature		-40	25	85	°C

Electrical Characteristics (5 V ±10 % V_{DD}) C_{PUMP} = C_{OUT} = 1 µF X7R, D = Schottky,

T_A = 25 °C, F_{OSC}= 125 kHz unless otherwise noted.

Table 9: Electrical Characteristics 5 V

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Supply Voltage		4.5	5	5.5	V
I_{QSC}	Quiescent current	R_L = ∞, 25 kHz	13	14	15	µA
I_{SHDN}	Shutdown current (Note 1)	SLG46533	-	0.89	-	µA
F_{OSC}	Oscillator frequency 25kHz OSC 2M OSC	selectable (Note 2)	0.048 -2.51% -5.44%	 25 / 2 n 2000 / 2 n	2000 3.89% 9.7%	kHz
I_{OUT}	Output current (Note 3)		5	10	45	mA
R_{OUT}	Output resistance	I_{OUT} =10 mA	-	118	170	Ω
V_{EFF}	Voltage conversion efficiency	R_L = ∞ (Note 4)	199	199.9	-	%
P_{EFF}	Power conversion efficiency	R_L = 5 KΩ	-	92.5	-	%
V_{TH}	Shutdown input threshold High State, Device Shutdown Low State, Device Operating	selectable (Note 5)	 1.15 0.77	 2.68 1.96	 - -	V

Electrical Characteristics (3.3 V ±10 % V_{DD}) C_{PUMP} = C_{OUT} = 1 µF X7R, D = Schottky,

T_A = 25 °C, F_{OSC} = 125 kHz unless otherwise noted.

Table 10: Electrical Characteristics 3.3 V

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Supply Voltage		3.0	3.3	3.6	V
I_{QSC}	Quiescent current	R_L = ∞, 25 kHz	10	10.5	11	µA
I_{SHDN}	Shutdown current (Note 1)	SLG46533	-	0.57	-	µA
F_{OSC}	Oscillator frequency 25kHz OSC 2M OSC	selectable (Note 2)	0.048 -2.01% -3.40%	 25 / 2 n 2000 / 2 n	2000 2.43 % 4.94 %	kHz
I_{OUT}	Output current (Note 3)		5	10	45	mA
R_{OUT}	Output resistance	I_{OUT} = 10 mA	-	125	185	Ω
V_{EFF}	Voltage conversion efficiency	R_L = ∞ (Note 4)	199	199.9	-	%
P_{EFF}	Power conversion efficiency	R_L = 5 KΩ	-	90	-	%
V_{TH}	Shutdown input threshold High State, Device Shutdown Low State, Device Operating	selectable (Note 5)	 1.06 0.67	 1.81 1.31	 - -	V

Electrical Characteristics (1.8 V ±5 % V_{DD}) C_{PUMP} = C_{OUT} = 1 µF X7R, D = Schottky,

T_A = 25 °C, F_{OSC} = 125 kHz unless otherwise noted.

Table 11: Electrical Characteristics 1.8 V

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Supply Voltage		1.71	1.8	1.89	V
I_{QSC}	Quiescent current	R_L = ∞, 25 kHz	8	8	8	µA
I_{SHDN}	Shutdown current (Note 1)	SLG46533	-	0.31	-	µA
F_{OSC}	Oscillator frequency 25 kHz OSC 2M OSC	selectable (Note 2)	0.048 -2.76% -3.23%	 25 / 2 n 2000 / 2 n	2000 3.42% 3.10%	kHz
I_{OUT}	Output current (Note 3)		5	10	45	mA
R_{OUT}	Output resistance	I_{OUT} = 10 mA	-	160	250	Ω
V_{EFF}	Voltage conversion efficiency	R_L = ∞ (Note 4)	199	199.9	-	%
P_{EFF}	Power conversion efficiency	R_L = 5 KΩ	-	84	-	%
V_{TH}	Shutdown input threshold High State, Device Shutdown Low State, Device Operating	selectable (Note 5)	 0.94 0.52	 1.06 0.76	 - -	V

Note 1 I_{SHDN}: specified for SLG46533, see relevant datasheet for other parts; I_{SHD} considers leakage and other parasitics outside GreenPAK negligible.

Note 2 Selectable frequencies are derived by dividing 25 kHz or 2 MHz: 25 kHz / 2 n or 2 MHz / 2 n, n=0..9

Note 3 Column “min”: single pin 2x drive, “typ”: 2 pins in parallel 2x drive, “max”: multiple pins in parallel 2x drive

Note 4 Voltage efficiency defined as V_{OUT} / V_{IN}. For voltage inverter this goes up to 100 %, for voltage doubler it must be above 100 % (otherwise output voltage is lower than input) and goes up to 200 % if full doubling is achieved.

Note 5 GreenPAK input levels may be programmed for Logic Input (min HIGH-Level and max LOW-Level shown in column typ) or Low-Level Logic Input (min HIGH-Level and max LOW-Level shown in column min). The third option is a Logic Input with Schmitt Trigger, see GreenPAK datasheet for associated voltage levels.

7 Testing & Results

A voltage doubler charge pump external circuit was assembled on a breadboard and connected to the GreenPAK Universal Development Board with a SLG46533 GreenPAK. SLG46533 has enough GPIO pins to test multiple pins in parallel. A programmable voltage source is connected to the charge pump input. A programmable load is connected to the charge pump output. Two professional high accuracy multimeters were connected to measure input and output parameters.

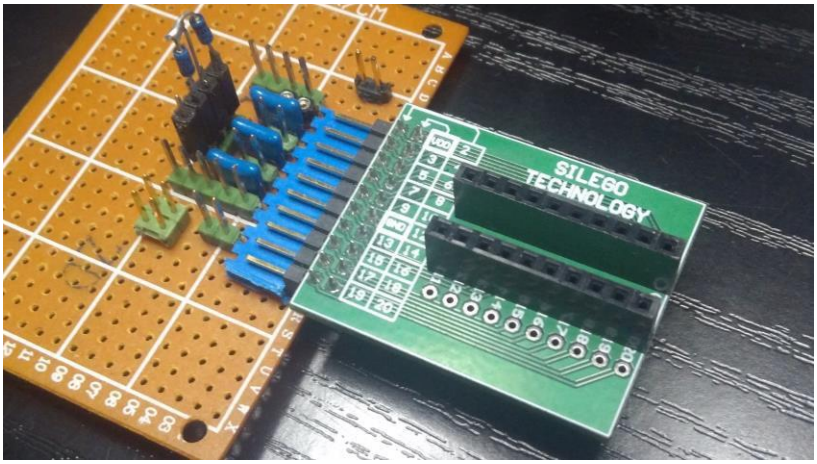

Figure 8: GreenPAK Charge Pump Test Setup Photo

For final measurements the GreenPAK Universal Development Board is removed because it introduces effects in the circuit that impact the measurement results, such as the series resistance of the analog switches. Several GreenPAK ICs are programmed for different charge pump configurations and connected to the test circuit via a socket adapter, as shown in the Figure 8.

Complete test setup schematics are shown in Figure 9. Note that GreenPAK I^2C Bridge is not used for the charge pump circuit, but to generate an external shutdown signal.

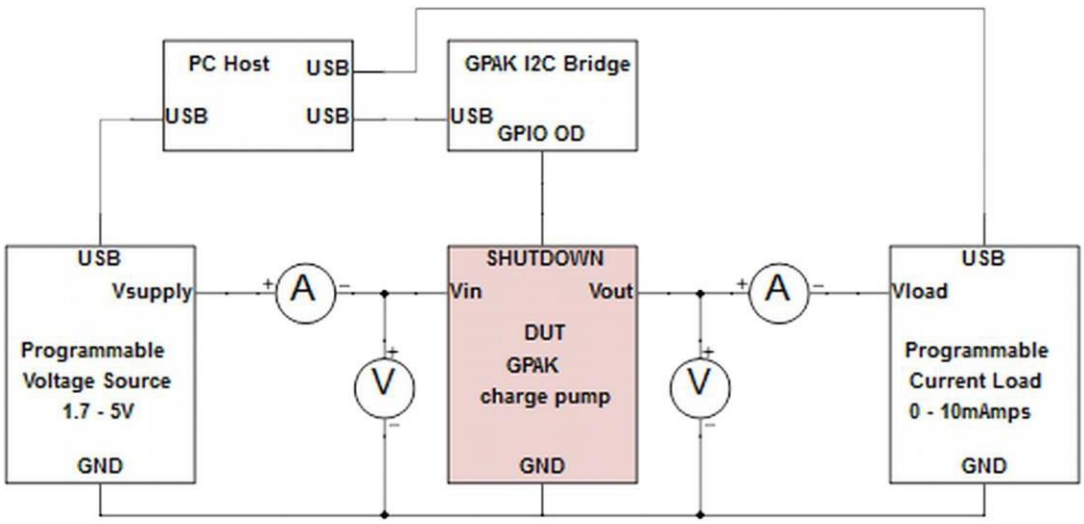

Figure 9: Test Setup

Since the testing includes various pin configurations, the GreenPAK design for DUT devices is adapted accordingly so that configuration may be changed by digital signals sent from an automated

test setup. The GreenPAK design is presented in Figure 10 and it is intended only for testing purposes.

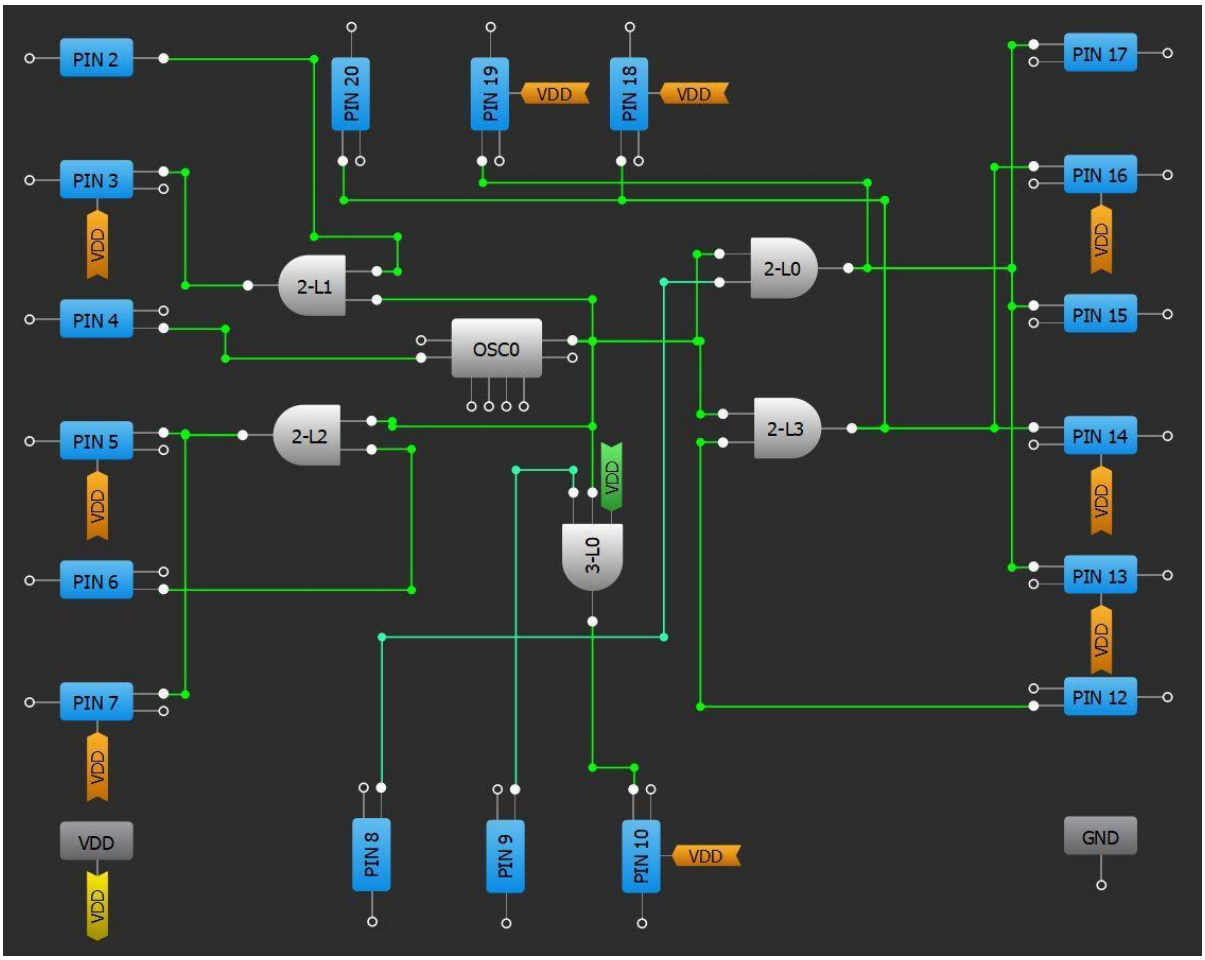

Figure 10: GreenPAK Design for DUT

7.1 Graphs

Measurements were obtained for two popular low-cost diode options: standard silicon fast switching diodes 1N4148 and Schottky diodes BAT42. Results are presented graphically:

All Graphs: C_{PUMP}= C_{OUT}= 1 µF X7R ceramic multilayer; T_A=25 °C

Graphs vs Load Current, parameter: V_{IN}; F=125 kHz; drive = 2 pin 2x

1..4) Output voltage vs Load current @ V_{IN} = 4.5 V, 3.3 V, 2.5 V and 1.8 V

5,6) Output resistance vs Load current @ V_{IN} = 4.5 V, 3.3 V, 2.5 V and 1.8 V

7..10) Efficiency vs Load current @ V_{IN} = 4.5 V, 3.3 V, 2.5 V and 1.8 V

11,12) Voltage efficiency vs Load current @ V_{IN} = 4.5 V, 3.3V, 2.5 V and 1.8 V

Graphs vs VIN;

1) Quiescent current vs V_{IN} @ drive = 2 x 1, 2 x 2, 2 x 4, 2 x 7; I_{OUT} = 0; F=25 kHz;

2) Quiescent current vs V_{IN} @ drive = 2 x 1, 2 x 2, 2 x 4, 2 x 7; I_{OUT} = 0; F=125 kHz;

3) Supply current vs V_{IN} @ shutdown; f = any; drive = any; D = any

4) Output voltage vs Input voltage @ drive = 1 x 1, 2 x 2, 2 x 2; I_{OUT} =1 mA, F=125 kHz

5,6) Output resistance vs V_{IN} @ drive = 2 x 1, 2 x 2, 2 x 4, 2 x 7 pin

5 V input Graphs, parameter: drive; F=125 kHz;

1..4) Output voltage vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =4.5V

5,6) Output resistance vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =4.5V

7..10) Efficiency vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =4.5 V

11,12) Voltage efficiency vs Load current @ drive = 1 x 1,1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =4.5 V

3 V 3 input Graphs, parameter: drive; F=125 kHz;

1..4) Output voltage vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 3.3 V

5,6) Output resistance vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 3.3 V

7..10) Efficiency vs Load current @ drive = 1x1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 3.3 V

11,12) Voltage efficiency vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 3.3 V

2 V 5 input Graphs, parameter: drive; F=125 kHz;

1..4) Output voltage vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 2.5 V

5,6) Output resistance vs Load current @ drive = 1 x 1,1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 2.5 V

7..10) Efficiency vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 2.5 V

11,12) Voltage efficiency vs Load current @ drive = 1 x 1,1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} = 2.5 V

1 V 8 input Graphs, parameter: drive; F=125 kHz;

1..4) Output voltage vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =1.8 V

5,6) Output resistance vs Load current @ drive = 1 x 1,1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =1.8 V

7..10) Efficiency vs Load current @ drive = 1 x 1, 1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =1.8 V

11,12) Voltage efficiency vs Load current @ drive = 1 x 1,1 x 2, 2 x 2, 2 x 4, 2 x 7; V_{IN} =1.8 V

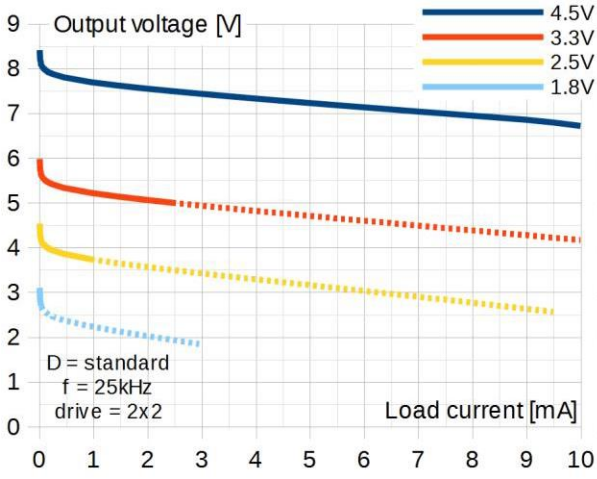

Figure 11: Output Voltage vs Load Silicon

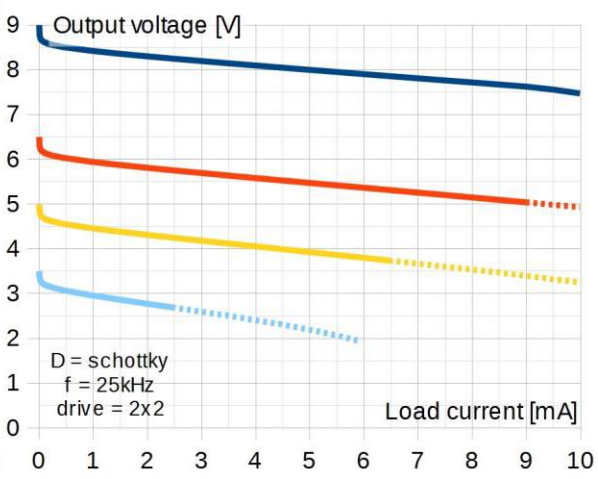

Figure 12: Output Voltage vs Load Schottky

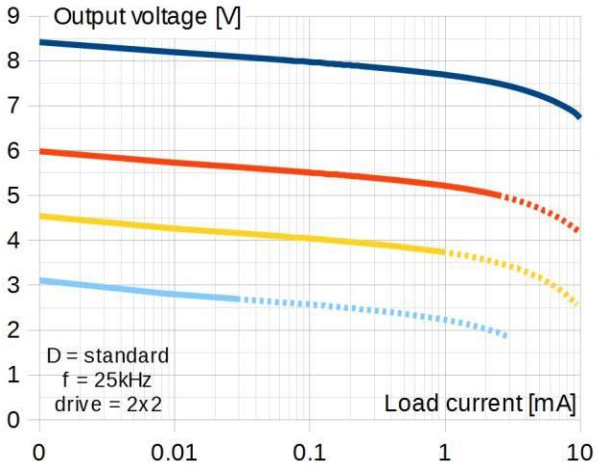

Figure 13: Output Voltage vs Load Silicon SC:LG

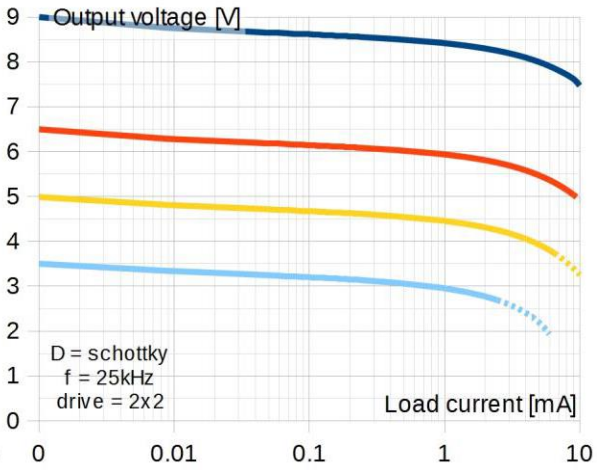

Figure 14: Output Volt. vs Load Schottky SC:LG

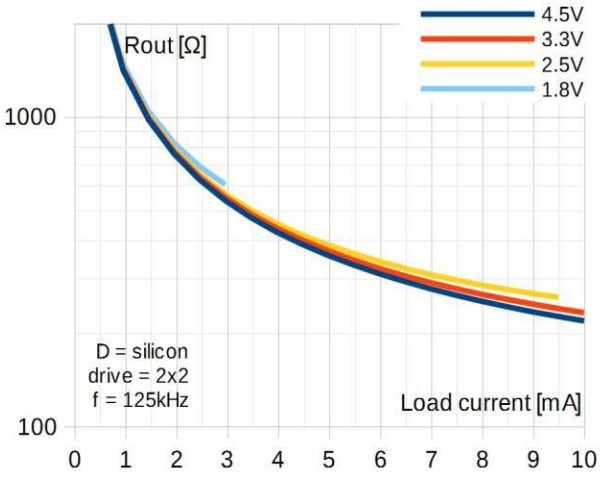

Figure 15: Output Resistance vs Load Silicon

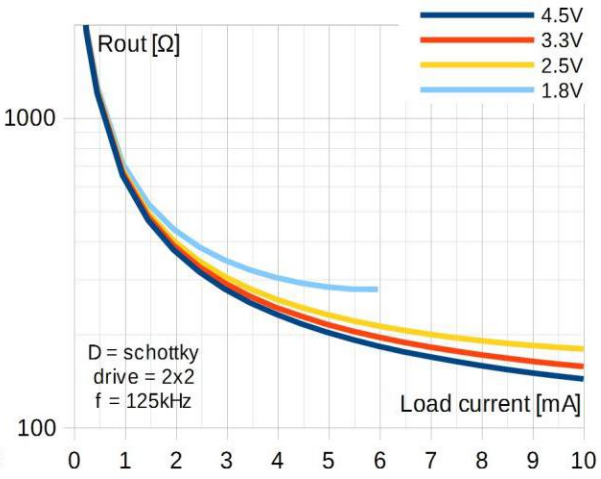

Figure 16: Output Resistance vs Load Schottky

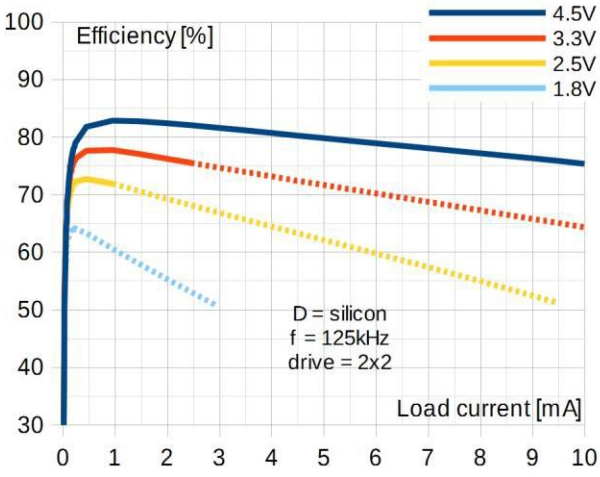

Figure 17: Efficiency vs Load Current Silicon

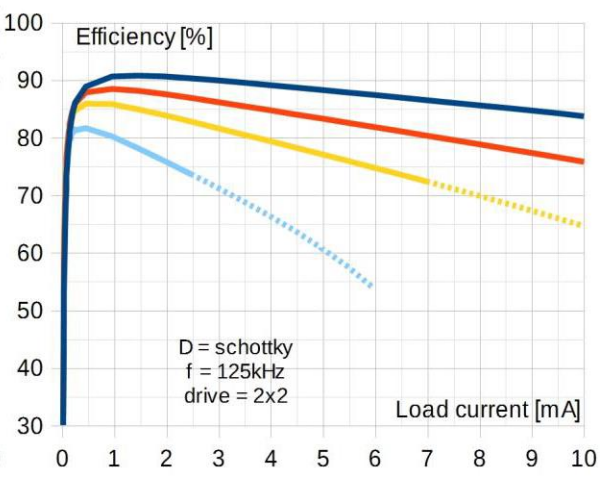

Figure 18: Efficiency vs Load Current Schottky

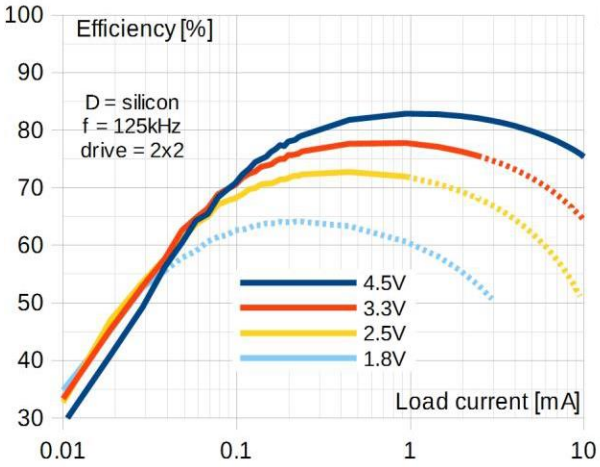

Figure 19: Efficiency vs Load Silicon SC:LG

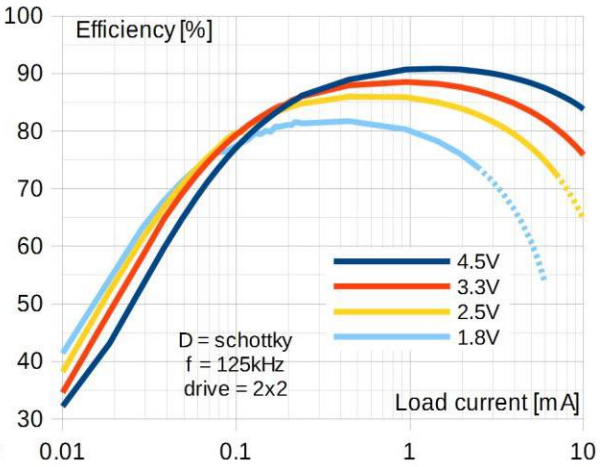

Figure 20: Efficiency vs Load Schottky SC:LG

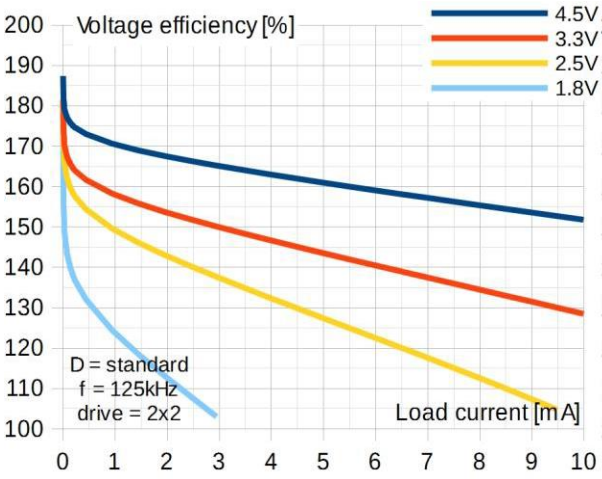

Figure 21: Voltage Efficiency vs Load Silicon

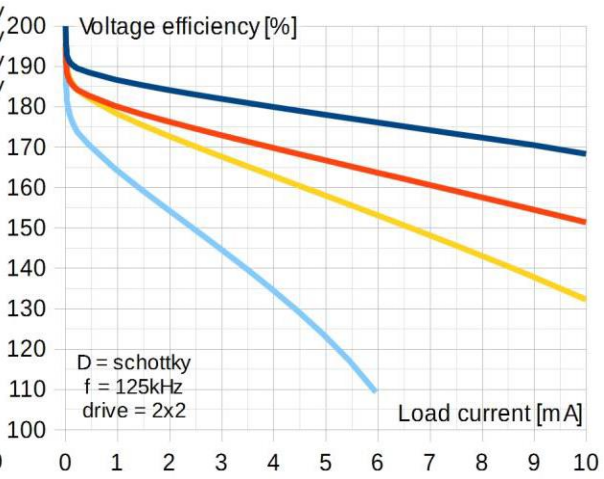

Figure 22: Voltage Efficiency vs Load Schottky

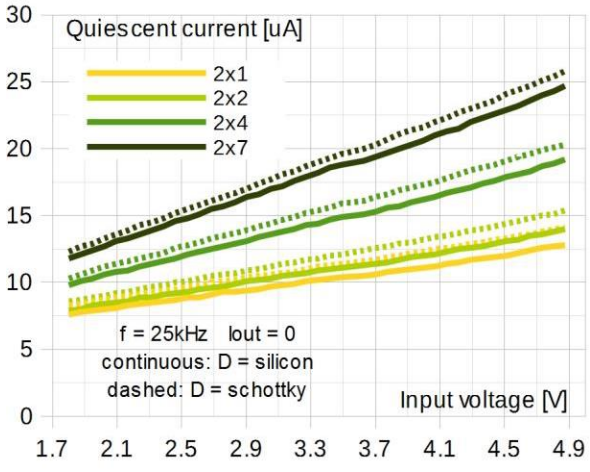

Figure 23: Quiescent Current vs V_{IN} 25 kHz

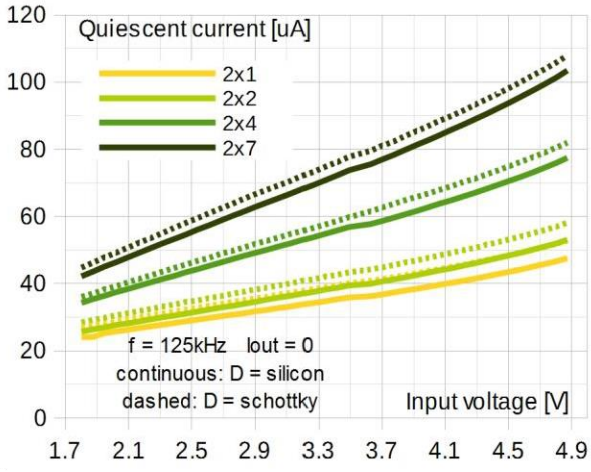

Figure 24: Quiescent Current vs V_{IN} 125 kHz

CPUMP = COUT = 1 µF F = 125 kHz T = 25 °C

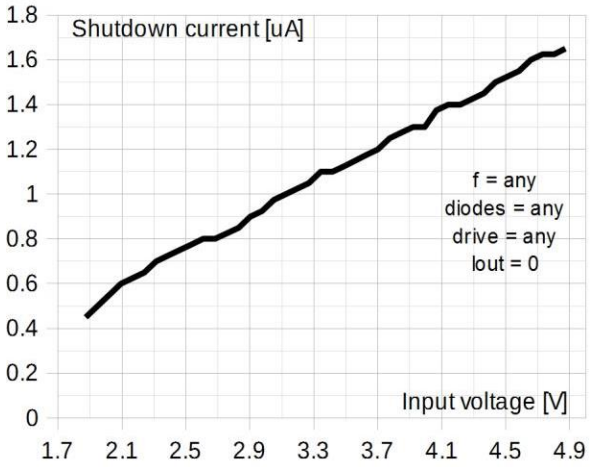

Figure 25: Shutdown Current vs V_{IN}

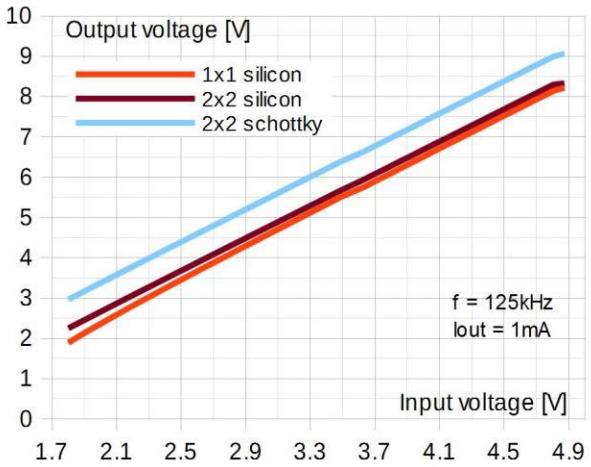

Figure 26: Output Voltage vs V_{IN}

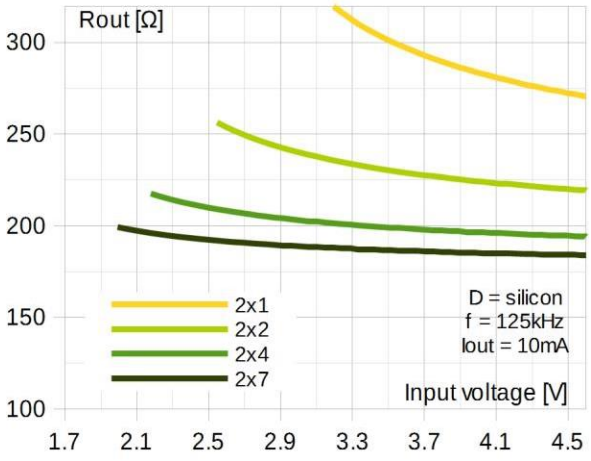

Figure 27: Output Resistance vs V_{IN} Silicon

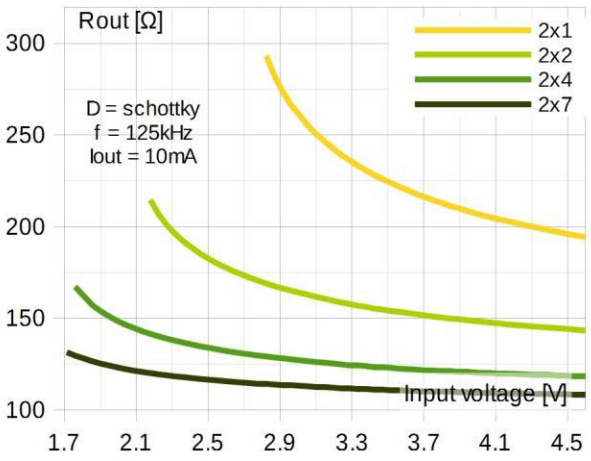

Figure 28: Output Resistance vs V_{IN} Schottky

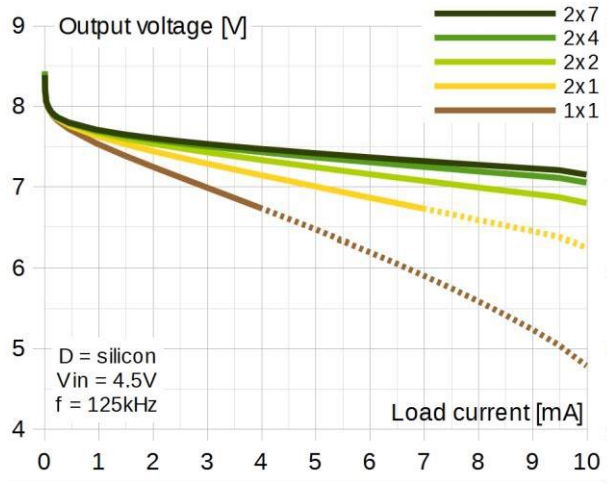

Figure 29: Load Regulation 5 V Silicon

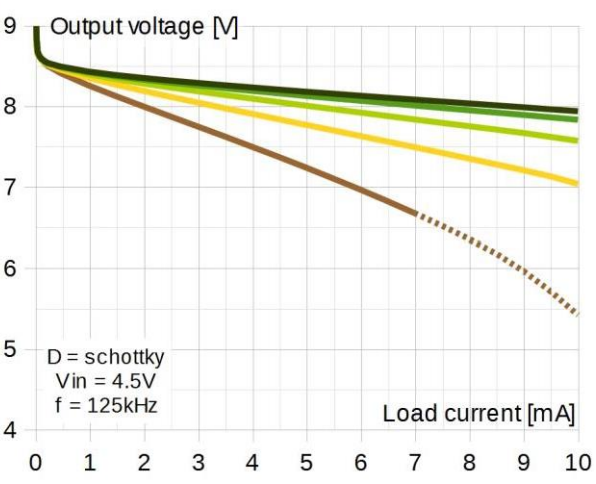

Figure 30: Load Regulation 5 V Schottky

5 V input V_{IN} = 4.5 V C_{PUMP} = C_{OUT} = 1 µF

F = 125 kHz T = 25 °C dashed: V_{EFF} < 150 %

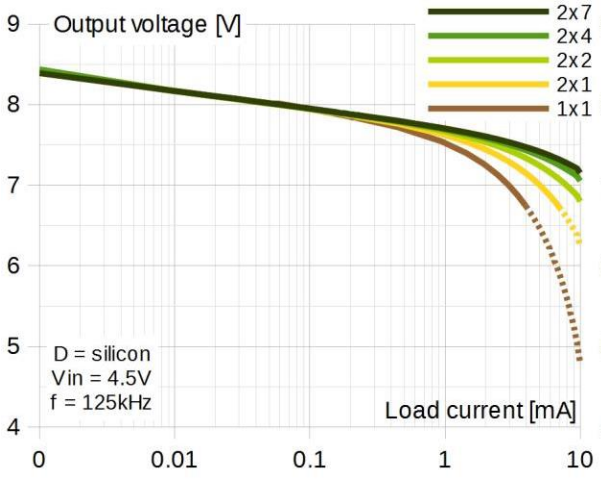

Figure 31: Load Regulation 5 V Silicon SC:LG

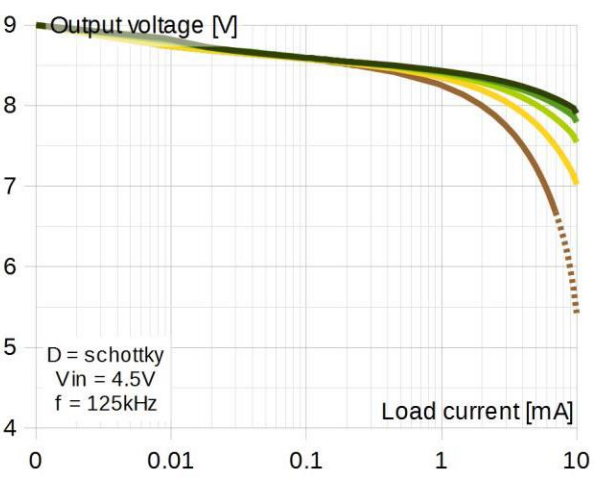

Figure 32: Load Regulation 5 V Schottky SC:LG

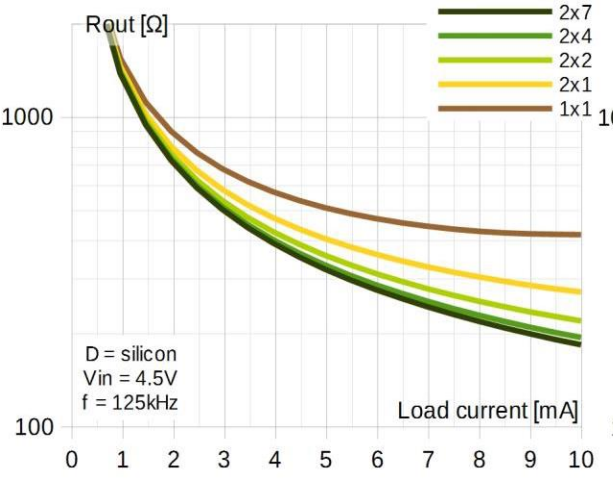

Figure 33: Output Resistance 5 V Silicon

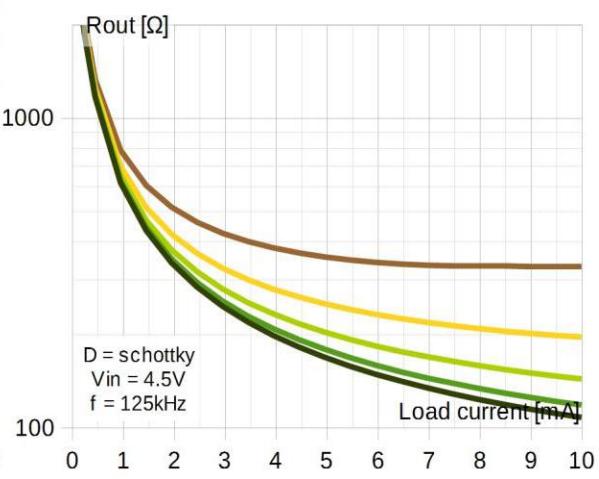

Figure 34: Output Resistance 5 V Schottky

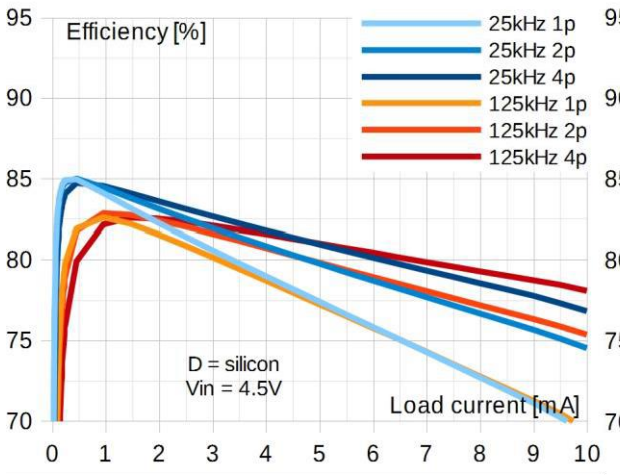

Figure 35: Efficiency 5 V Silicon

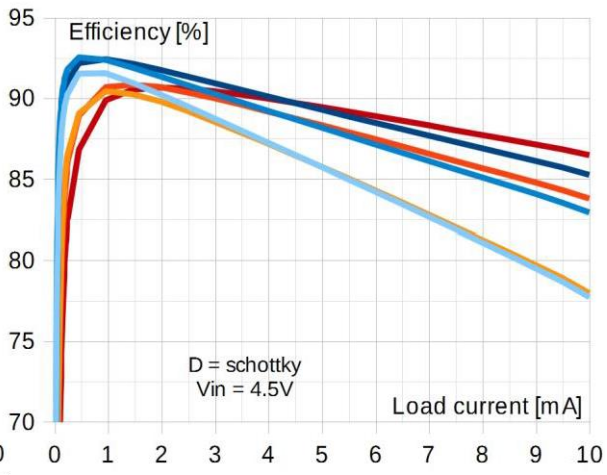

Figure 36: Efficiency 5 V Schottky

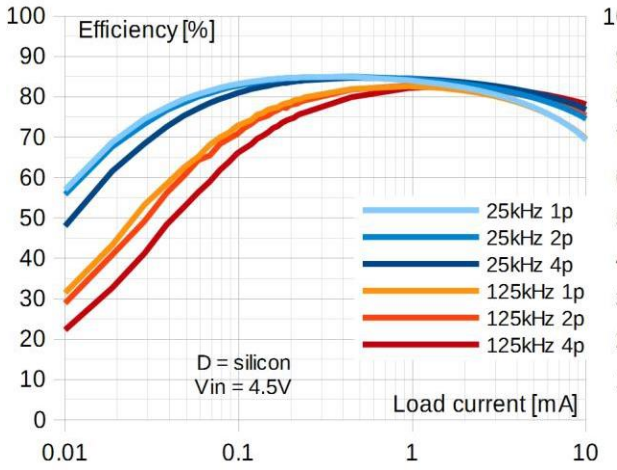

Figure 37: Efficiency 5 V Silicon SC:LG

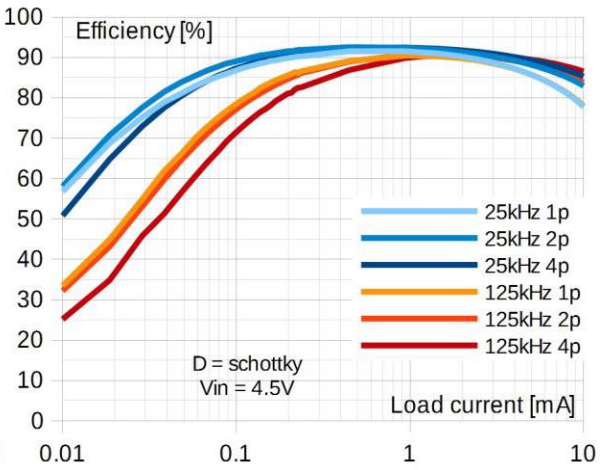

Figure 38: Efficiency 5 V Schottky SC:LG

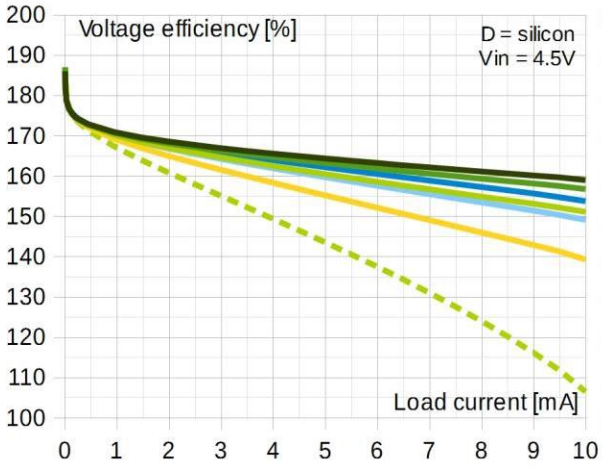

Figure 39: Voltage Efficiency 5 V Silicon

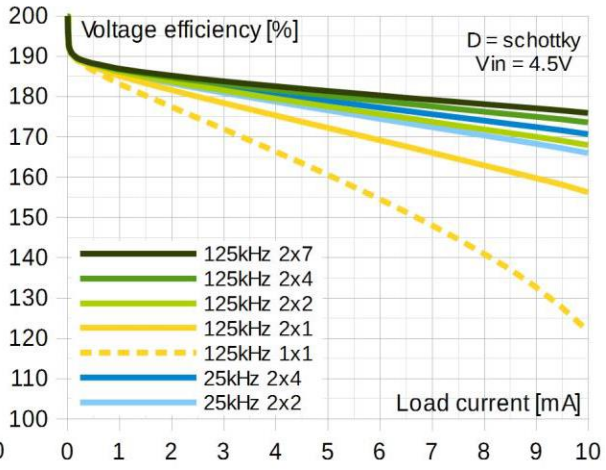

Figure 40: Voltage Efficiency 5 V Schottky

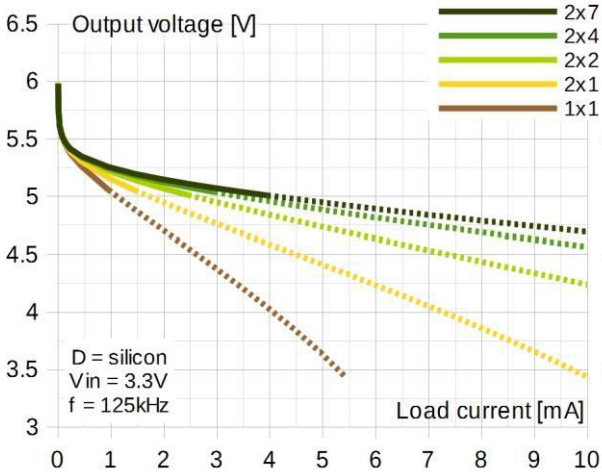

Figure 41: Load Regulation 3.3 V Silicon

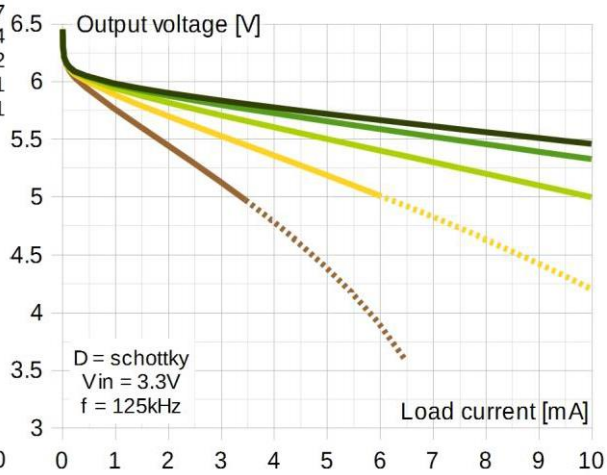

Figure 42: Load Regulation 3.3 V Schottky

3.3 V input V_{IN} = 3.3 V C_{PUMP} = C_{OUT} = 1 µF F = 125 kHz T = 25 °C dashed: V_{EFF} < 150 %

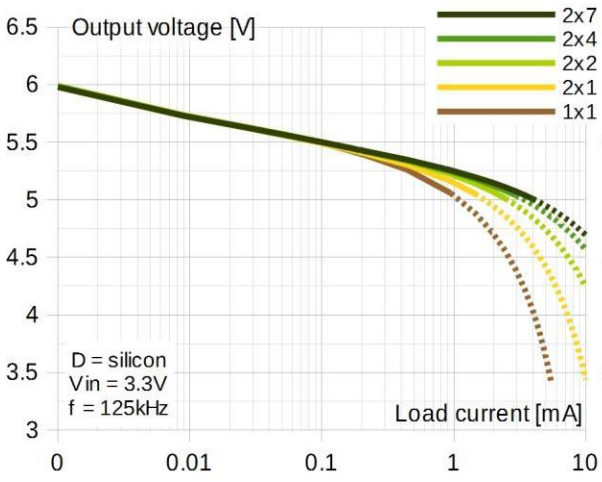

Figure 43: Load Regulation 3.3 V Silicon SC:LG

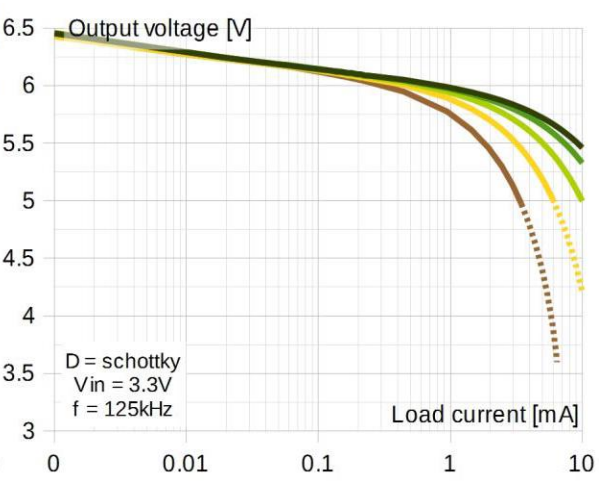

Figure 44: Load Regulation 3.3 V Schottky SC:LG

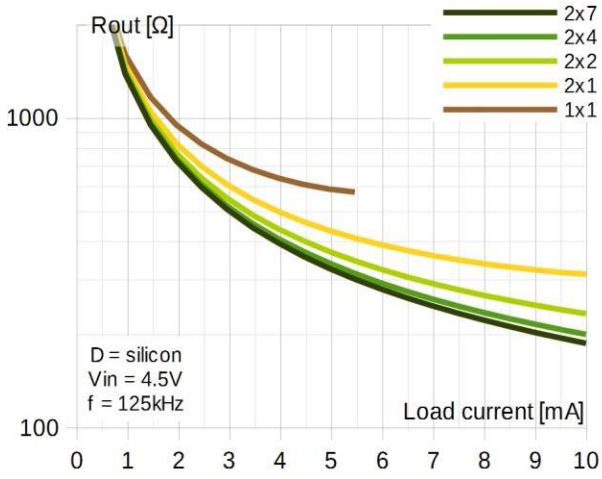

Figure 45: Output Resistance 3.3 V Silicon

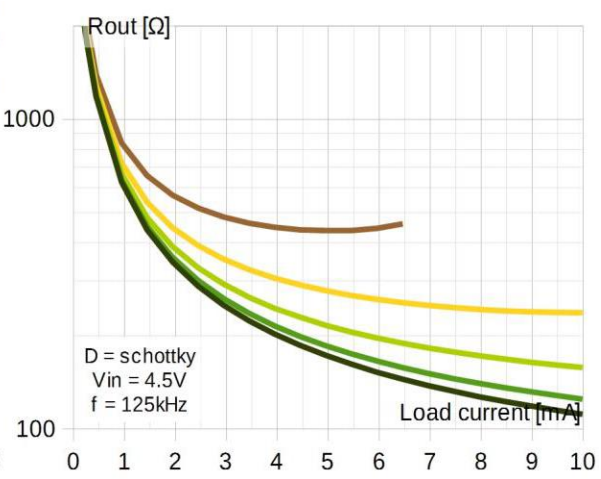

Figure 46: Output Resistance 3.3 V Schottky

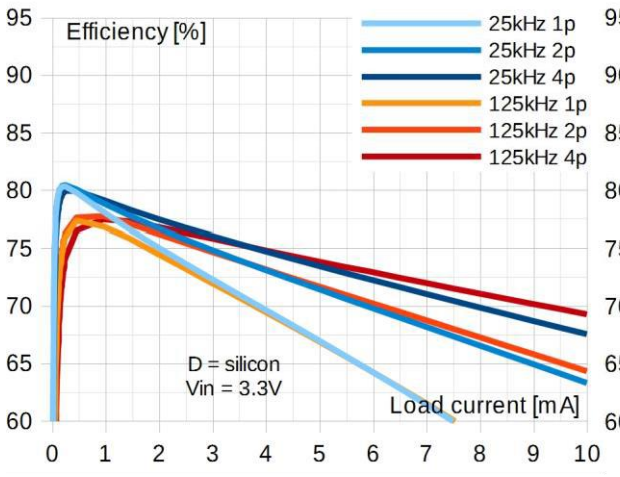

Figure 47: Efficiency 3.3 V Silicon

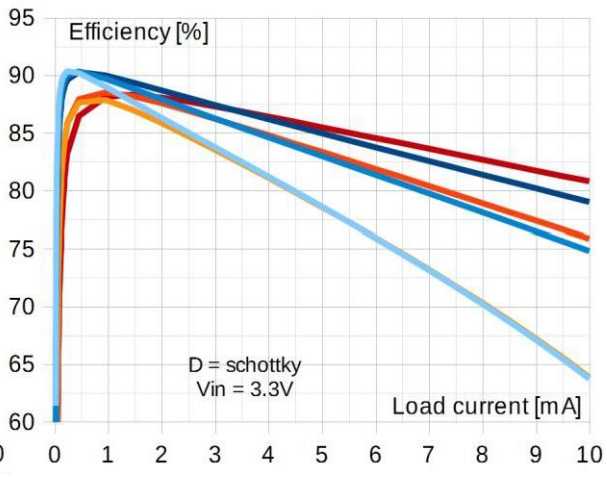

Figure 48: Efficiency 3.3 V Schottky

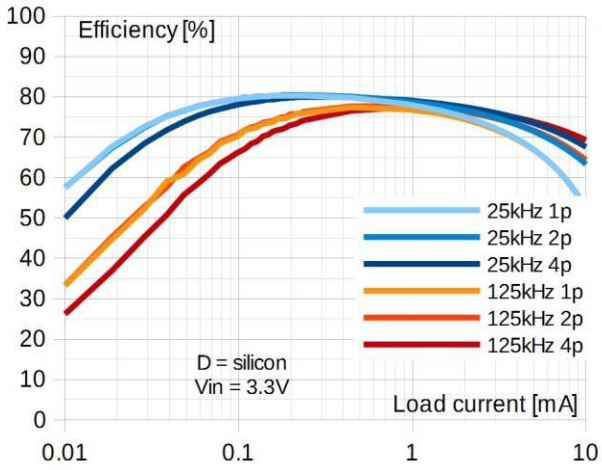

Figure 49: Efficiency 3.3 V Silicon SC:LG

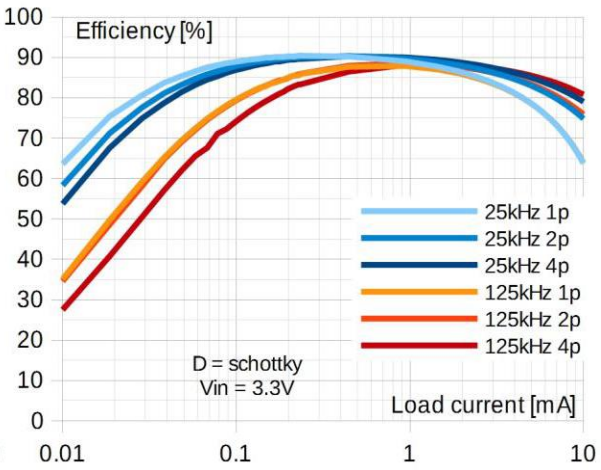

Figure 50: Efficiency 3.3 V Schottky SC:LG

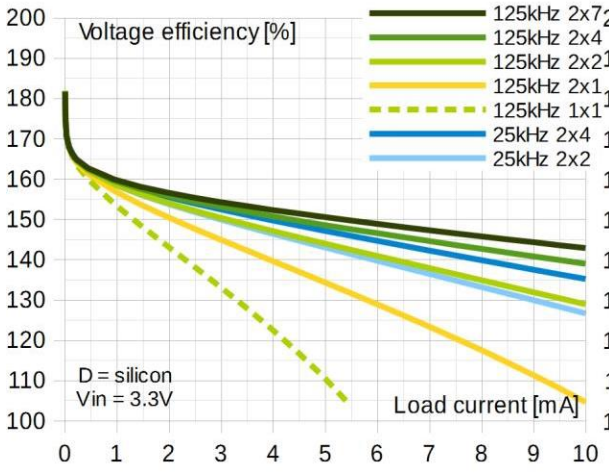

Figure 51: Voltage Efficiency 3.3 V Silicon

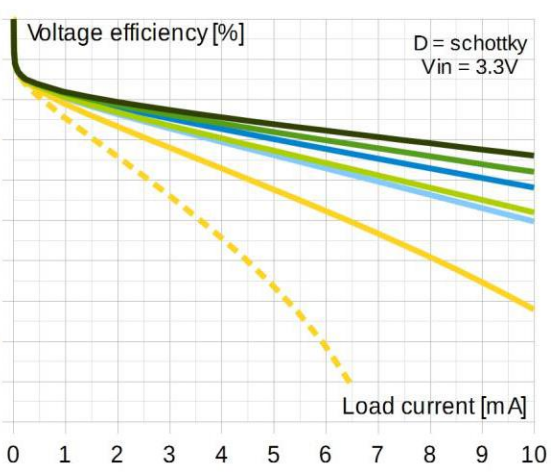

Figure 52: Voltage Efficiency 3.3 V Schottky

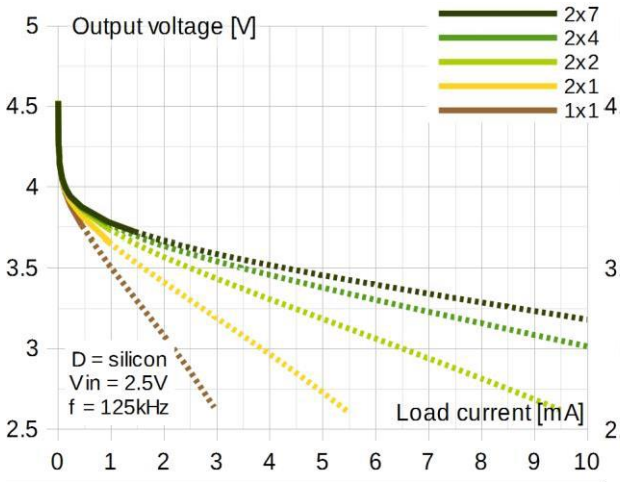

Figure 53: Load Regulation 2.5 V Silicon

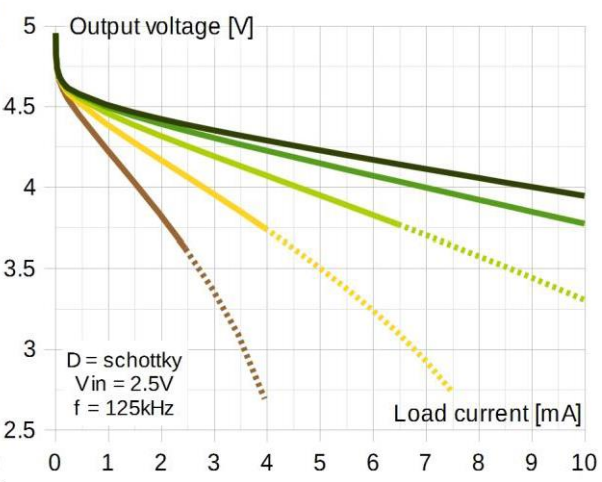

Figure 54: Load Regulation 2.5 V Schottky

2.5 V input V_{IN} = 2.5 V C_{PUMP} = C_{OUT} = 1 µF F = 125 kHz T =25 °C dashed: V_{EFF} < 150 %

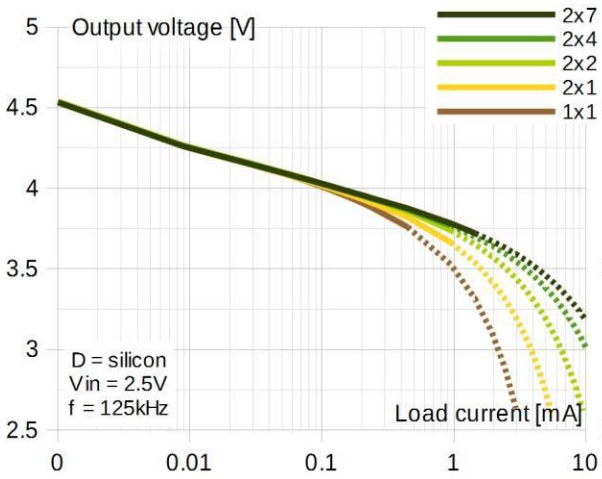

Figure 55: Load Regulation 2.5 V Silicon SC:LG

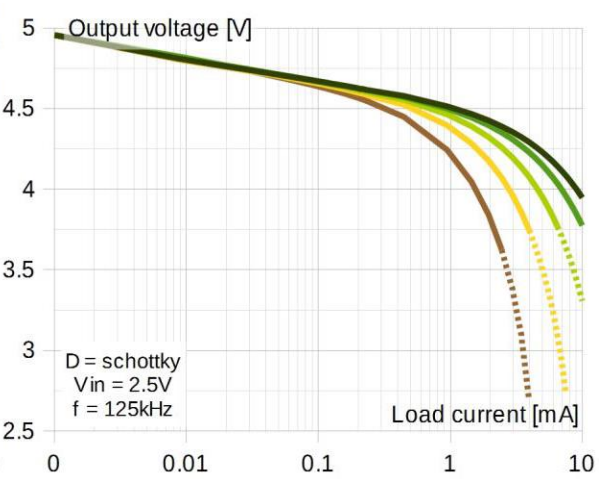

Figure 56: Load Regulation 2.5 V Schottky SC:LG

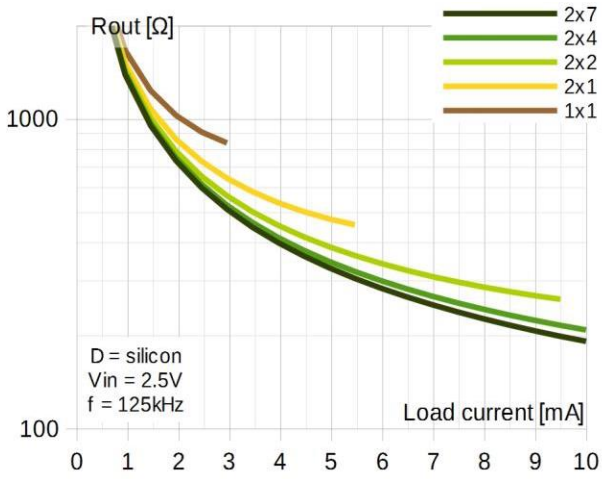

Figure 57: Output Resistance 2.5 V Silicon

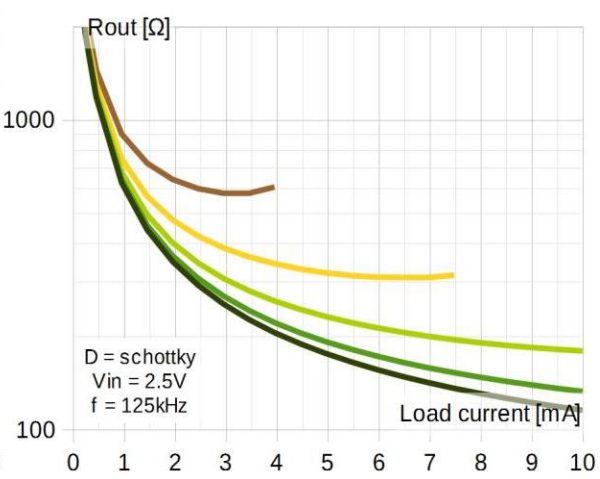

Figure 58: Output Resistance 2.5 V Schottky

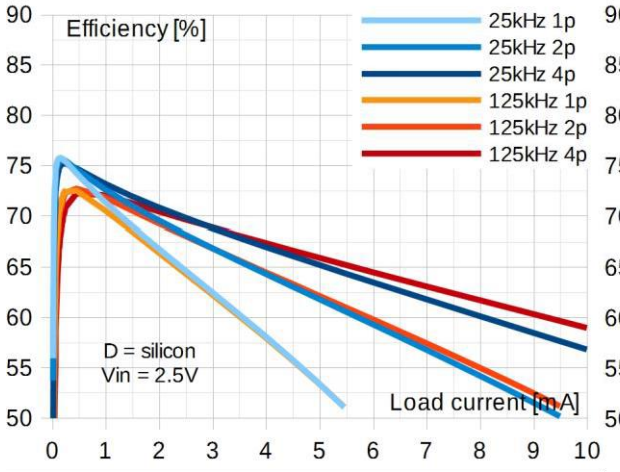

Figure 59: Efficiency 2.5 V Silicon

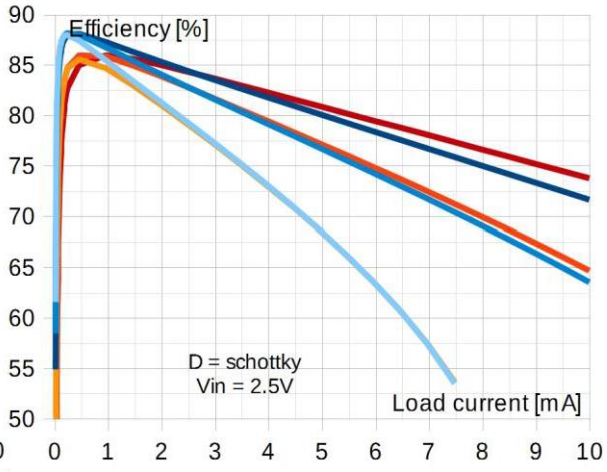

Figure 60: Efficiency 2.5 V Schottky

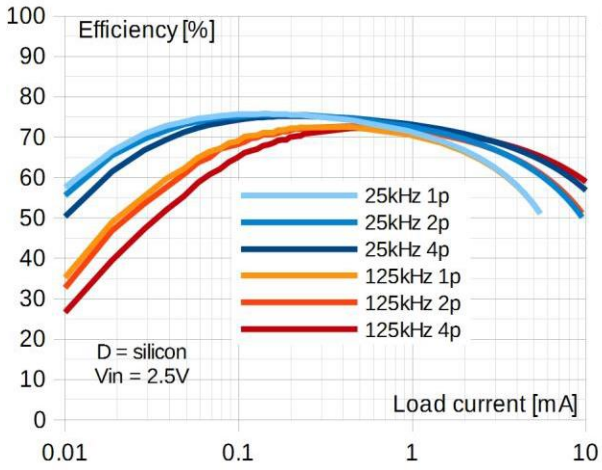

Figure 61: Efficiency 2.5 V Silicon SC:LG

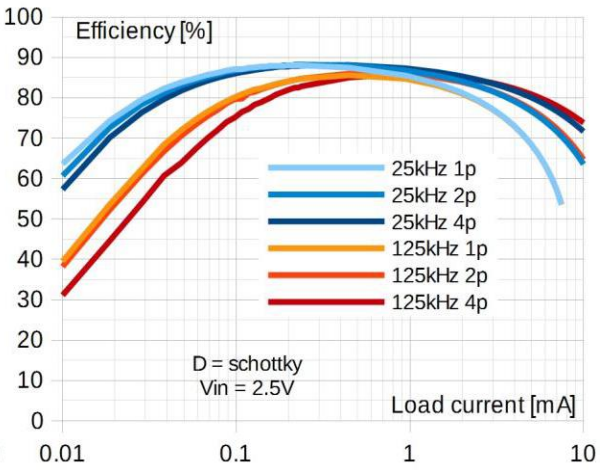

Figure 62: Efficiency 2.5 V Schottky SC:LG

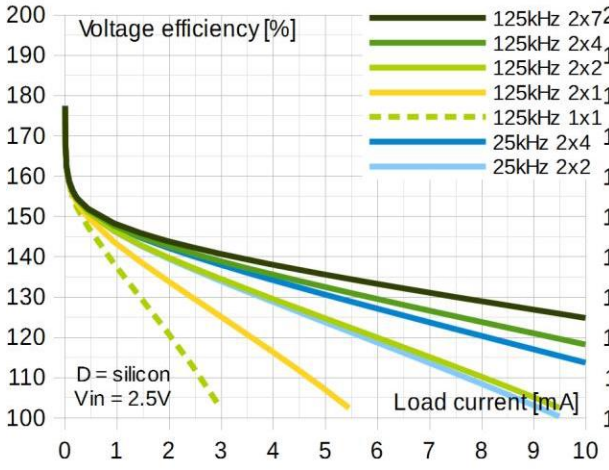

Figure 63: Voltage Efficiency 2.5 V Silicon

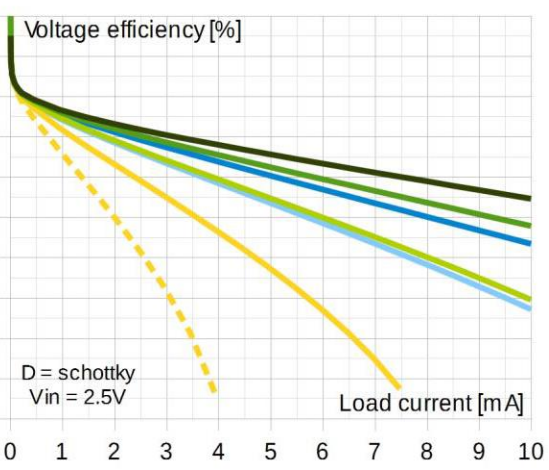

Figure 64: Voltage Efficiency 2.5 V Schottky

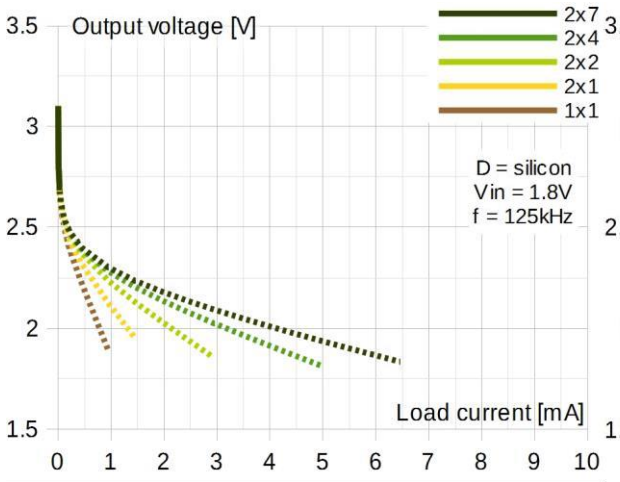

Figure 65: Load Regulation 1.8 V Silicon

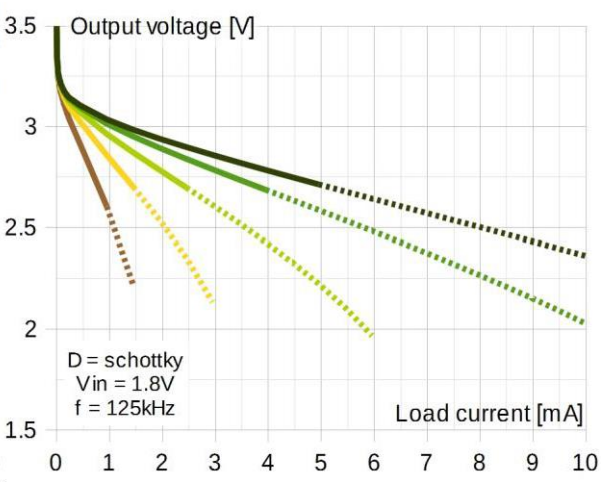

Figure 66: Load Regulation 1.8 V Schottky

1.8 V input V_{IN} = 1.8V C_{PUMP} = C_{OUT} = 1 µF F = 125 kHz T = 25 °C dashed: V_{EFF} < 150 %

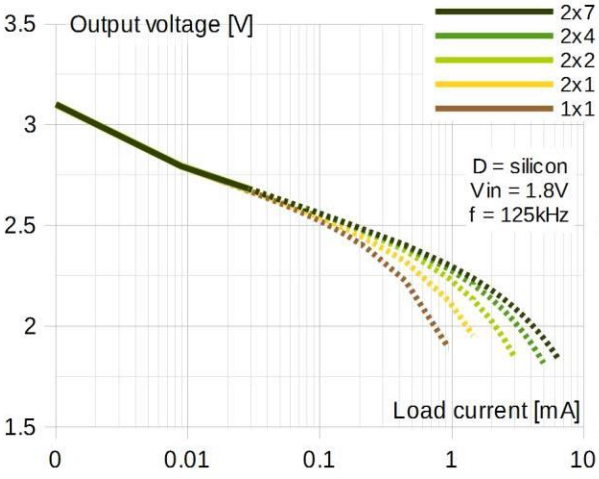

Figure 67: Load Regulation 1.8 V Silicon SC:LG

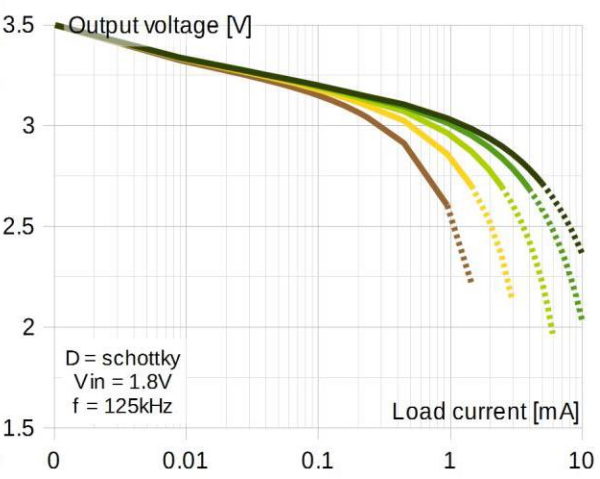

Figure 68: Load Regulation 1.8 V Schottky SC:LG

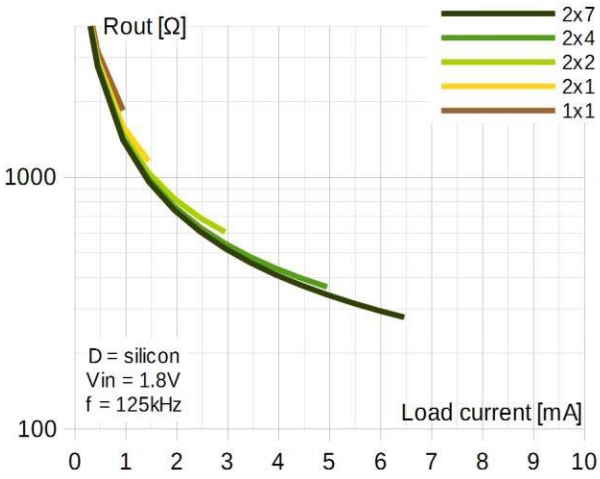

Figure 69: Output Resistance 1.8 V Silicon

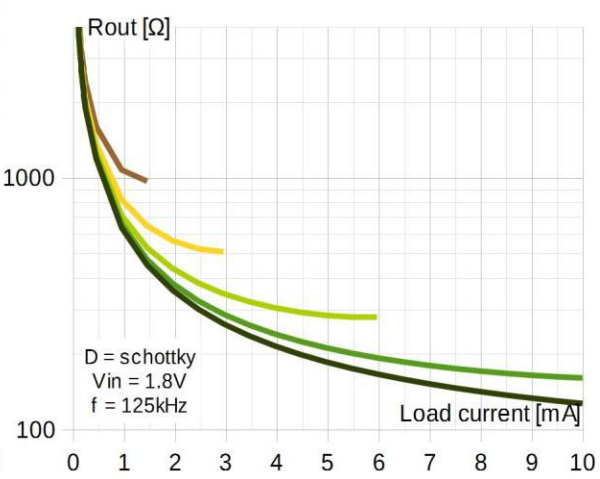

Figure 70: Output Resistance 1.8 V Schottky

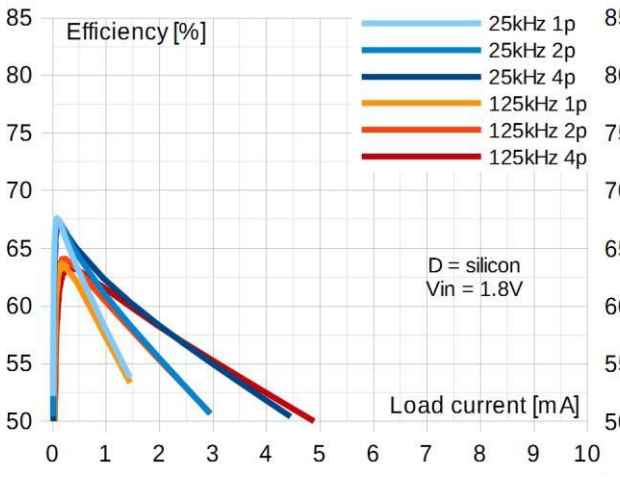

Figure 71: Efficiency 1.8 V Silicon

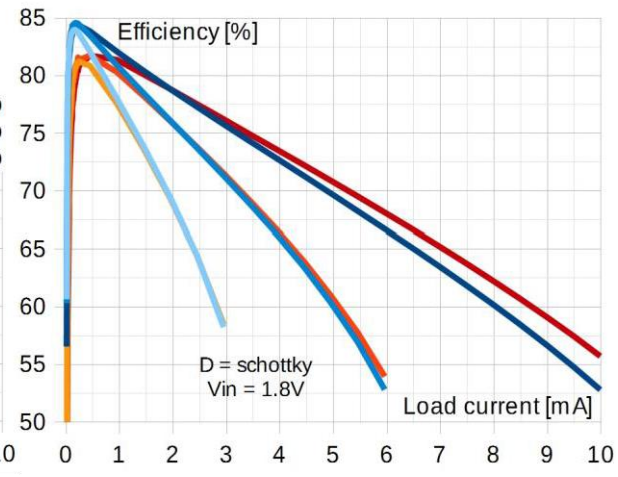

Figure 72: Efficiency 1.8 V Schottky

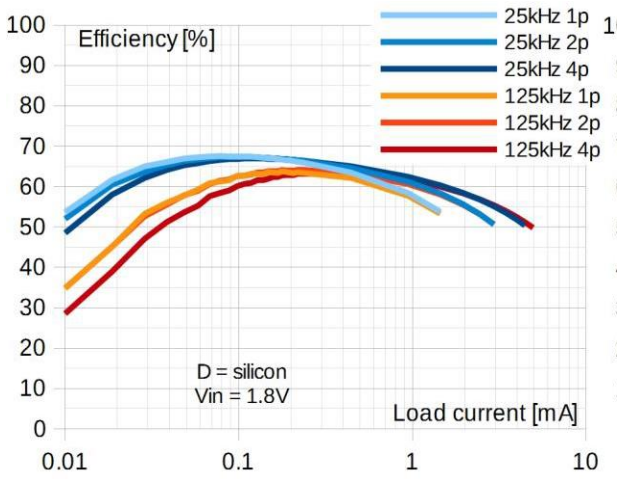

Figure 73: Efficiency 1.8 V Silicon SC:LG

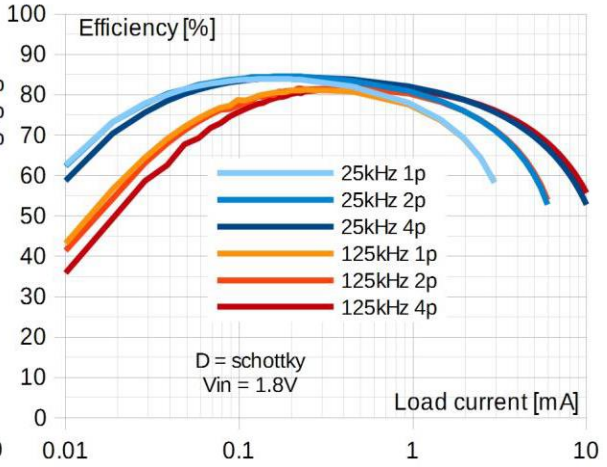

Figure 74: Efficiency 1.8 V Schottky SC:LG

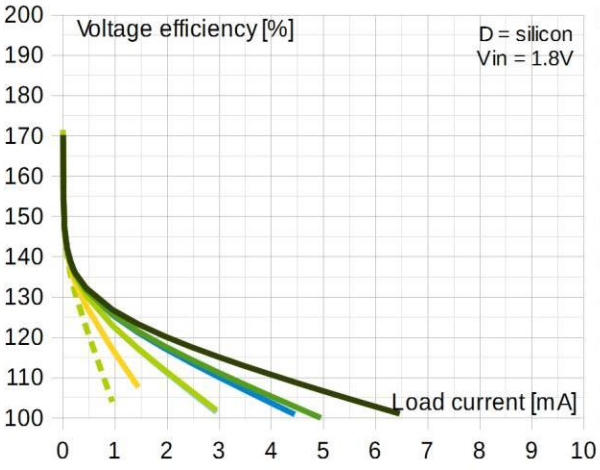

Figure 75: Voltage Efficiency 1.8 V D = Silicon

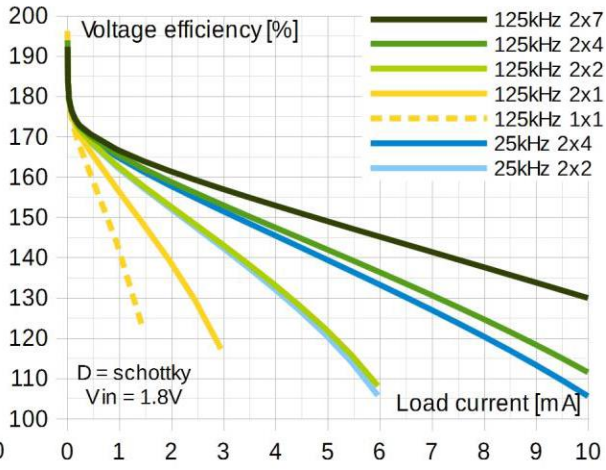

Figure 76: Voltage Efficiency 1.8 V D = Schottky

8 Layout Considerations

As with any switching power supply circuit, good layout practice is encouraged. Some layout considerations are applicable to all charge pump designs, while some are specific for those that incorporate GreenPAKs.

8.1 General Layout Recommendations

Mount all components (GreenPAK, capacitors and diodes) as close together as possible to minimize stray inductance and capacitance. Use short, wide traces to connect the external components to the charge pump to minimize trace resistance and inductance.

If applicable, use a large ground plane to minimize noise leakage into another circuitry.

Place capacitors as close to the charge pump as possible, preferably on the same side of the board as the GreenPAK.

Keep the resistance connection between board ground and the GND pin of the GreenPAK as low as possible. In the case of the ground plane, use multiple vias to connect GND to a ground plane of the board. Otherwise, apply thick traces and/or copper pour.

Keep the resistance connection between board power supply and V_{DD} pin of the GreenPAK as low as possible. A high impedance V_{DD} connection is not as bad as high impedance GND connection, but it will still degrade charge pump performance considerably.

8.2 Specific Layout Recommendations for GreenPAK

GreenPAK is a mixed signal integrated circuit; when part of the GreenPAK is used to run a charge pump circuit, interference with the rest of the GreenPAK design may arise at high charge pump output currents and high operating frequencies. To keep the mixed signal circuit performance high, exceptional care should be devoted to layout.

Select the pins closest to GreenPAK GND pin for driving the charge pump. If multiple pins are used in parallel, select neighboring pins and wire them all together before wiring to the external capacitor. The best option is to wire them together below the GreenPAK. If that is not possible, try to keep the

wires between driving pins and the pump capacitor (or the meeting node) as short as possible, but with matching thickness and length.

In a mixed signal design, keep charge pump driving pins away from sensitive analog pins to avoid capacitive coupling. Insert one GreenPAK output pin between charge pump pins and sensitive analog pins for decoupling. Connect the “decoupling pin” to GND in GreenPAK design. If needed, extend the “decoupling wire” to further shield the noisy “pumping” connection.

When using multiple pins on GreenPAKs with split internal power rails, share the load over power rails. For example, if 4 pins are driving the pump capacitor, take 2 of those from each rail, keeping them all close together and close to GND. That way, the internal voltage drop from GreenPAK power pins (V_{DD} and GND) to each output pin structure will be lower than if you group all the driving pins on one power rail.

When using pins from both sides of GND pin (both rails as noted above), if decoupling is needed, apply two decoupling pins, one to each side.

9 Optional Design Modifications and Optimizations

9.1 Replacing Diodes with Synchronous Switching MOSFETs

External diodes may be replaced by MOSFETs or analog switches to reduce voltage loss (increase output voltage) and improve efficiency. Unlike diodes, those parts require control and drive and since they are switching out of the input power supply range; external drive circuitry must be added. Driving external FETs increases the component count, cost and size of the design making it less competitive. It also introduces new source of switching losses to control, like gate drive loss, that will take away part of the benefits gained. However, if voltage efficiency is the primary concern this topology is preferable, since it enables voltage efficiencies better than commercial charge pump ICs. If you plan to run the pump at high operating frequencies and/or low input voltages, be sure to select low input capacitance FETs, since switching losses may increase significantly.

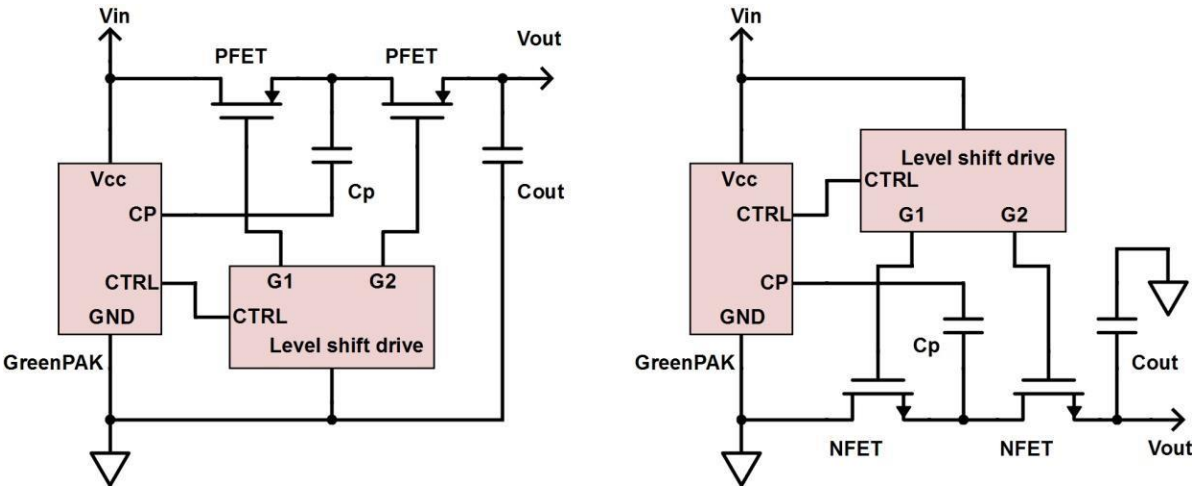

Figure 77: Replacing Diodes with Synchronous Switching MOSFETs

9.2 External Drive for Pump Capacitor

In applications where a limited number of pins are available, or high output current is required, adding a buffer to drive a pump capacitor reduces output resistance at a reasonable cost. In this configuration, GreenPAK is not used to drive the pump capacitor, so output current of the charge pump is not limited by GreenPAK current capacity anymore. It is limited by current capacities of the diodes and FETs in the circuit. A simple, high performance and cost-effective way to implement a current buffer is using complementary MOSFETs in a push pull arrangement. GreenPAK can drive both FETs directly. Make separate gate drive signals for NFET and PFET and introduce some dead time to ensure they are not both on during the transitions.

To keep the efficiency high, select low RDS_{ON} FETs. If size is a top priority select a MOSFET array with a NFET/PFET pair. To keep quiescent current low, select low input capacitance FETs.

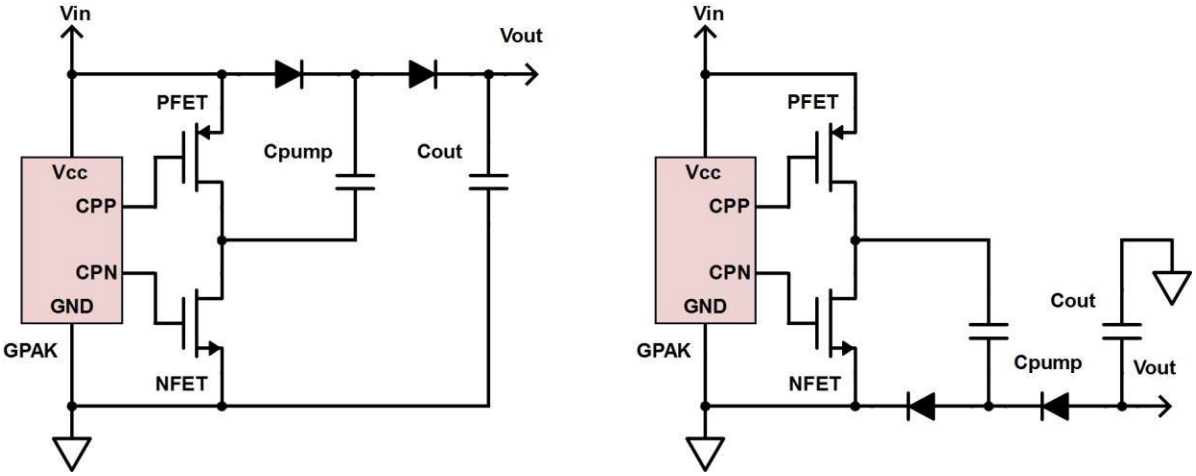

Figure 78: Pump Capacitor Current Buffer

9.3 Bleeder Resistor Deletes Output Voltage Peak at Light Loads

Load regulation may be improved simply and cost-effectively by introducing one bleeder resistor. Output voltage will peak when at no load, so wiring a megohm range resistor to the output will ensure output voltage will never exceed a certain level. This would also degrade efficiency, especially at light loads, and increase quiescent current. Note however that the bleeder resistor doesn't help with input voltage variation, which will be reflected to the output with bleeder in circuit. In a voltage doubler circuit a bleeder between the output, will cut the dissipated power to 25 %.

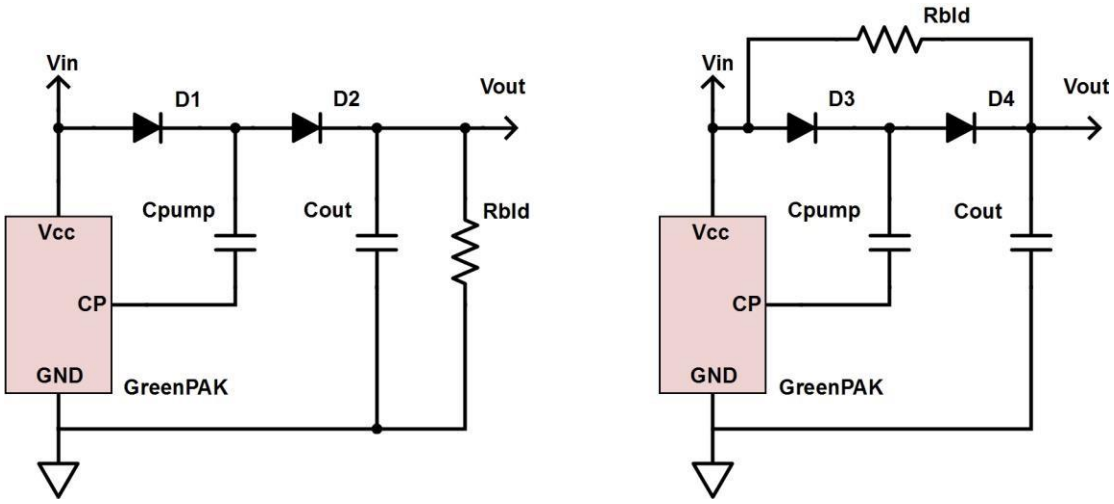

Figure 79: Introducing Bleeder Resistor Deletes Output Voltage Peak at Light Loads

9.4 Reusing GreenPAK Pins for Multiple Outputs

If multiple outputs are required, the same pins may be reused for all charge pumps, provided all pumps switch at the same frequency. In the case of the doubler + inverter shown in Figure 80, pump capacitor current from two charge pumps offset each other, so the resulting average pin current is actually lower than in the case of only one charge pump. If load currents are equal on outputs, pump currents cancel each other and current pulses through CPP pin only during transitions.

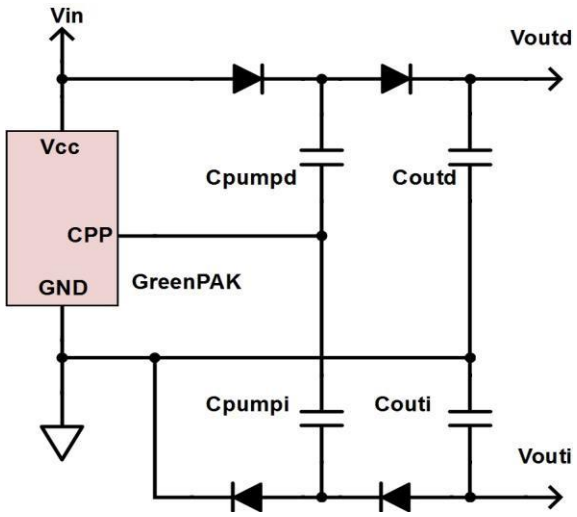

Figure 80: Reusing Pins for Multiple Pumps

Note that for output currents above 5 mA multiple pins must be used because, at zero load with one output, 2 * I_{OUT} current will flow through CPP pin(s). Paralleled pins can be used to drive both pumps.

10 GreenPAK Part Selection

Once you decide to use GreenPAK as a charge pump circuit there are many options available depending upon your application requirements. A quick selection guide is presented in Table 12.

Data in the table is valid for a charge pump circuit design like the demo circuit presented in this app note, containing only the charge pump and a couple of logic gates. If surplus blocks are utilized to add other functions, current consumption may increase, depending upon the design.

Green shaded fields emphasize performance marks outscoring comparable parts. SLG46108 is emphasized because it is the smallest and lowest cost GreenPAK. Table 12 evaluates the following metrics:

Maximum current:

I_{OUT} – maximum output current for inverter and doubler

I_{OUTDFS} – maximum output current for doubler with full shutdown, for parts with PFET it is assumed that PFET is used for powerdown

GPIO pins – maximum current through GPIO pin and pin count, for dual supply GreenPAKs shown as a + b where a and b represent pin count on first and second supply

Power pins – maximum current through V_{DD} and GND power pins, per chip side (The GreenPAK's power rails are divided in two sides). Maximum total current through V_{DD} or GND power pin is double the figure displayed in the table, provided it is split equally to the two sides.

Current draw:

I_{QSC} – Quiescent current drawn with charge pump running and zero load at V_{IN} = 3.3 V

I_{SHDN} – Shutdown current drawn with charge pump off at V_{IN} = 3.3 V

Table 12: GreenPAK Part Selection

	Maximum Current			Power Pins		Supply	I2C	Current Draw		PFET
	I_{OUT}	I_{OUTDFS}	GPIO pins	V_{DD}	GND	V_{IN}		I_{QSC}	I_{SHDN}	
	mA	mA		mA	mA	V		µA	µA	Amps
SLG46108	25	15	10 mA 5 p	45	90	1.71 .. 5.5	---	5.6	0.52	---
SLG46110	59	34	17 mA 7 p	73	92	1.71 .. 5.5	---	4.8	0.80	---
SLG46116/117	51	51	17 mA 6 p	73	92	1.71 .. 5.5	---	4.8	0.80	1.25 A
SLG46120	76	51	17 mA 9 p	73	92	1.71 .. 5.5	---	4.7	0.80	---
SLG46121	2 x 34	2 x 17	17 mA 4+4	73	92	1.71 .. 5.5	---	4.7	0.80	---
SLG46127	42	42	17 mA 5 p	73	92	1.71 .. 5.5	---	4.8	0.80	2 x 2 A

	Maximum Current			Power Pins		Supply	I2C	Current Draw		PFET
SLG46140	90	45	21 mA 9 p, 43 mA 2 p 4x	45	45	1.71 .. 5.5	---	0.5	0.16	---
SLG46169/170	55	35	10 mA 11 p	45	84	1.71 .. 5.5	---	5.1	0.80	---
SLG46533	90	45	16 mA 15 p	45	86	1.71 .. 5.5	yes	6.0	0.57	---
SLG46534/536	72	45	16 mA 9 p	45	86	1.71 .. 5.5	yes	7.9	0.75	---
SLG46535	2 x 32	2 x 16	16 mA 4+4	45	86	1.71 .. 5.5	yes	7.9	0.75	---
SLG46537/531	90	45	16 mA 15p	45	86	1.71 .. 5.5	yes	7.6	0.75	---
SLG46538/532	2 x 45	2 x 22	16 mA 6+8	45	86	1.71 .. 5.5	yes	7.9	0.75	---
SLG46620	90	45	14 mA 15 p, 28 mA 2 p 4x	45	69	1.71 .. 5.5	---	0.9	0.37	---
SLG46621	2 x 45	2 x 22	14 mA 7+8, 28 mA 1+1 4x	45	69	1.71 .. 5.5	---	0.9	0.37	---
SLG46721/722	85	45	10 mA 17 p	45	84	1.71 .. 5.5	---	5.1	0.80	---
SLG46580/2/3	146	146	43 mA 8 p	73	152	2.3 .. 5.5	yes	0.4	0.17	0.6 A

Notes:

Data for GPIO pins are for “2x push pull” output mode. Only SLG46140, SLG46620 and SLG46621 feature 4x push pull pins.

SLG46580/2/3 feature a “2x push pull” output mode, but the pin’s performance (switch resistance and current capacity) is similar to “4x push pull” output mode for other parts.

SLG46116/117 and SLG46127 PFETs have a 50 mΩ to 100 mΩ RDS_{ON}, depending upon the supply voltage. SLG46580/2/3 feature 1, 2 or 4 PFETs with RDS_{ON} of 250 mΩ, 0,5 Ω and 1 Ω.

Data for current draw is for the lowest consumption oscillator. For the SLG46140, SLG46620 and SLG46621 this is the LF OSC, for SLG46580/2/3 that’s 2.048 kHz OSC. For all others 25 kHz RC oscillator.

Note the versatility of SLG4658x parts. Those parts offer the highest output current/ power, lowest switch resistance per pin, lowest quiescent/shutdown current, including both I2C communication and integrated PFET power switch(es) while other parameters match other GreenPAK parts.

10.1 Quick Part Selection

Part selection involves many parameters, and due to the many different GreenPAKs available, picking the right part is not straightforward. To ease the selection process, a quick selection table is presented in Table 13.

If you just need the basic charge pump features, check the first column. Cells in that column contain the best parts per criteria shown in Table 12. If you need more features, like I2C, a dual supply, or an integrated power switch they are not available with the parts in the first column, so consider the parts in the other columns.

Table 13: Quick Part Selection

Selection Criteria	Basic Features Only	With I2C Options	With Dual Supply	With Integrated Power Switch
Highest performance	SLG46580/2/3	SLG46580/2/3	SLG46538	SLG46580/2/3
Ultra-low power	SLG46140 0.7 µA @ 3.3 V	SLG46533 6.6 µA @ 3.3 V	SLG46621 1.3 µA @ 3.3 V	SLG46116/7 5.3 µA @ 3.3 V
Lowest cost	SLG46108	SLG46534	SLG46121	SLG46116/7
Smallest size	SLG46108 1.0 mm x 1.2 mm	SLG46533/4/7 2.0 mm x 2.2 mm	SLG46121 1.6 mm x 1.6 mm	SLG46116/7 1.6 mm x 2.5 mm

Current consumption is shown at 3.3 V. For parts available in different packages the smallest package is shown.

11 Key Advantages and Commercial Viability

If you already have a GreenPAK IC in your circuit performing other functions, with at least one unused pin, then it is absolutely commercially viable to implement a GreenPAK charge pump solution because it will take just a couple of additional diodes and capacitors. The total cost of such a solution comes down to cents, 5 to 10 times less than a specialized charge pump IC.

A GreenPAK charge pump solution is also competitive if it is applied solely as a charge pump. In this case, select low cost GreenPAKs, such as the SLG46108, and you can reach a cost 2 times less than specialized charge pump IC solutions.

One GreenPAK can control multiple charge pump circuits. The cost of each additional charge pump comes down to additional external components, which is a couple of cents. With commercial charge pump ICs, each pump comes at full price. With a GreenPAK solution for multiple charge pumps, parameters of each circuit may be programmed independently. Multiple outputs with the same voltage level might be required if separate on/off control is needed or to avoid cross regulation effects.

With several GreenPAKs it is possible to control the charge pump circuit via serial communication. Some offer SPI, while others offer I^2C. On/off control, operating frequency, wake/sleep regime are some parameters that can be set via serial comms.

Key advantages of a GreenPAK charge pump solution:

- lower cost,
- smaller size,
- multiple outputs with the same IC,
- programmable operating frequency,
- serial communication control,
- lower quiescent current,
- surplus logic and analog blocks for additional functions.

A GreenPAK solution offers similar or better performance and some additional features at a fraction of the price.

For the solution presented in this application note to be commercially viable certain requirements must be within a performance level range that is achievable by a GreenPAK solution. That range is dependent on supply voltage; for exact data please refer to graphs in this application note. General requirements are summarized as follows:

- output current in the milliamps range (< 10 mA)

- voltage efficiency > 180 % for doubler, < 80 % for inverter

- power conversion efficiency < 90 %

- output resistance > 100 Ω.

The required output current must be in the milliamps range, because for output currents over 10 mA circuit performance drops markedly on behalf of the RDS_{ON} of the GreenPAK output stage MOSFETs.

Circuit performance out of stated specs can be achieved by modifying the design as specified in the “Design modification” section of this application note. For example, if top efficiency is required, diodes have to be replaced with external switches, and such a solution may perform same or better than specialized charge pump ICs with integrated MOSFET switches.

12 Conclusion

This application note presented that a high performance, small size capacitive charge pump can be built easily using a GreenPAK IC and just a couple of low cost external components .GreenPAK charge pumps operate with input voltages from 1.8 V to 5 V and load currents up to 145 mA. Overall performance peaks at input voltages of 3 V to 5 V and output currents 1 mA to 5 mA when using Schottky diodes.

There are certain “basic charge pump” feature sets where proposed GreenPAK solution offers lower cost, smaller size or lower quiescent current than specialized ICs. Other applications where a GreenPAK based charge pump solution is preferable compared to specialized charger ICs are applications needing specific functions not available in specialized ICs. The surplus circuitry in GreenPAK, unused in the basic design of the charge pump circuit, can be utilized in those applications to implement such specific functions. Specific functions could be directly or closely related to charge pump function, but may just as well be completely independent hardware functions of the target device, such as reset logic for an external IC or system.

This application note does not cover all performance ranges of capacitive charge pumps, but GreenPAKs offer a configurable solution to cover them when coupled with appropriate external design.

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