# Application Note

## ADC Current Sense

### AN-CM-291


## Abstract

*This application note describes how to implement an analog-to-digital converter (ADC) in the SLG46855V to measure current drawn by a load. The correlating ADC code can be read from the counter data via I2C. It also details some accuracy analysis of the read ADC value.*

*This application note comes complete with design files which can be found in the References section.*

# Contents



# Figures



# Tables



 

# 1 Terms and Definitions

| | |
|---|---|
| ADC | Analog to digital converter |
| DAC | Digital to analog converter |
| PWM | Pulse width modulation |

# 2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure™ Software Hub | Renesas, Software Download and User Guide

[2] AN-CM-291 ADC Current Sense.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG46855V, Datasheet

[6] AN-1177, Flexible Range ADC with I2C Interface, Application Note

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# 3 Introduction

In this application note we will describe how to implement an 8-bit analog-to-digital converter (ADC) in the SLG46855V [5] that can sense load current and interface with an MCU via I2C. This design can be used for various current sensing applications such as ammeters, fault detection systems, and fuel gauges.

# 4 ADC Architecture

The ADC is essentially comprised of an analog comparator and a Digital-to-Analog Converter (DAC). The comparator senses the input voltage vs. the DAC output voltage, and subsequently controls whether to increment or decrement the DAC input code, such that the DAC output converges to the input voltage. The resulting DAC input code becomes the ADC digital output code.

In our implementation, we create a DAC using a pulse-width modulation (PWM) controlled resistor network. We can easily create a precise digitally controlled PWM output using GreenPAK. The PWM when filtered becomes our analog voltage and thus serves as an effective DAC. A distinct advantage of this approach is that it is easy to set the voltages which corresponds to zero code and full scale (equivalently offset and gain) by simply adjusting resistor values. For example, a user wants to ideally read zero code from a temperature sensor with no current (0 µA) corresponding to 4.3 V, and full-scale code at 1000 µA corresponding to 3.9 V (Table 1). This is easily implemented by simply setting a few resistor values. By having the ADC range match the sensor range of interest, we make greatest use of the ADC resolution.

**Table 1: Example Code to Current Comparison**

| Code (Dec) | Current (µA) | $V_{SENSE}$ (V) |
|---|---|---|
| 0 | 0 | 4.3 |
| 125 | 500 | 4.1 |
| 255 | 1000 | 3.9 |

A design consideration for this architecture is that an internal PWM frequency needs to be much faster than the ADC update rate to prevent underdamped behavior of its control loop. At the very least it should be longer than the ADC data counter clock divided by 256. In this design, the ADC update period is set to 1.3312 ms.

# 5 Internal Circuit

The flexible ADC is based on the design presented in AN-1177 [6]. The clock speed is increased from 1 MHz to 12.5 MHz in order to clock the ADC counter since the SLG46855 has a 25 MHz clock available. This allows a much faster update rate for finer sample resolution. The LUT clocking the ADC data clock is changed so it will pass through the 12.5 MHz signal when the PWM DFF is low.

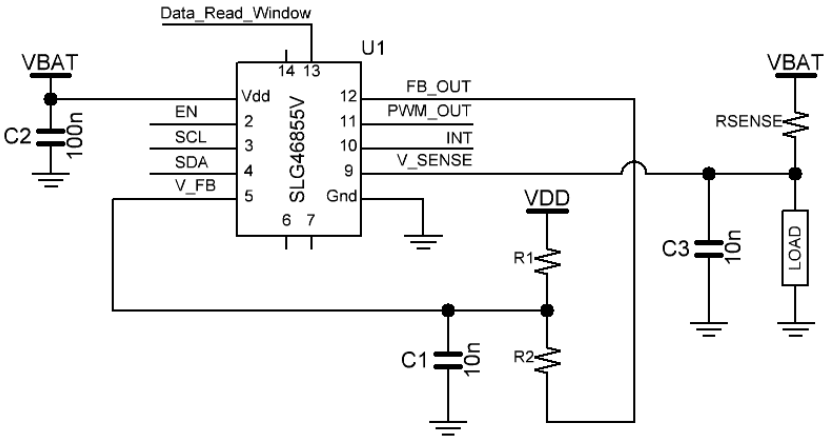


**Figure 1: External Circuit Schematic**

# 6 External Circuit

An external resistor and capacitor network are used to convert a PWM into an analog voltage as shown in the circuit schematic in Figure 1. The values are calculated for maximum resolution for the maximum current the device will sense. To achieve this flexibility, we add resistors R1 and R2 in parallel to VDD and ground. A resistor divider divides down VBAT to the low side of voltage range. The divider ratio for an expected minimum VBAT can be solved using the following equation:

Equation 1:

$$Divider = 1 - \frac{I_{MAX} \times R_{SENSE}}{V_{BAT\ MIN}}$$

# 7 I2C Read Instructions

Table 1 describes the I2C command structure to read back the data stored in CNT0. The I2C commands require a start bit, control byte, word address, read bit, and stop bit.

**Table 2: I2C Structure**

| Information | Data (Hex) |
|---|---|
| Start Bit | [ |
| Control Byte/Slave Address | 0x10 (Write); 0x11 (Read) |
| Word Address/CNT0 Counted Value | 0xA5 |
| Read Bit | R |
| Stop Bit | ] |

An example I2C command to read back the CNT0 counted value is written below:

[0x10 0xA5] [0x11 R]

The counted value that is read back will be the ADC code value. As an example, an Arduino code is included in the ZIP file of this application note on the website.

 

# 8 Results

To test the accuracy of the ADC current sense design, the measured values at a given load current and VDD level were compared to a theoretical value. The theoretical ADC values were calculated with the following equation:

Equation 2:

$$ADC\ Value = \left(1 - \frac{I_{LOAD} \times R_{SENSE} - V_{BAT} + V_{BAT} \times Divider}{V_{BAT} \times (Divider - 1)}\right) \times 256$$

The $I_{LOAD}$ that correlates with an ADC value is found with the following equation:

Equation 3:

$$I_{LOAD} = \frac{V_{BAT}\ (Div - 1)\left(1 - \frac{ADC\ Value}{256}\right) + V_{BAT} - V_{BAT} \times Div}{R_{SENSE}}$$

For the following results I used these component values:

**Table 3: Component Values for Test Circuit**

| Component | Nominal Value | Measured Value |
|---|---|---|
| $R_{SENSE}$ | 400Ω | 381Ω |
| $R_1$ | 10kΩ | 11.87kΩ |
| $R_2$ | 100kΩ | 89.94kΩ |
| $R_{LOAD}$ | 50kΩ (potentiometer) | N/A |
| $C_1$ | 10nF | 9.26nF |
| $C_2$ | 10nF | 9.47nF |

The resolution of the ADC value to $I_{LOAD}$ conversion can be calculated by using equation 3 with the measured values in Table 2 and the ADC value set to 1. With a $V_{BAT}$ of 3.9 V the resolution is 4.96 µA/div.

In order to optimize the ADC current sense circuit to a minimum VDD level of 3.6 V with a maximum current of 1100 µA and a 381 Ω sense resistor, the ideal divider coefficient would be 0.884, based on equation 1. With the values given in Table 2, the actual divider has a divider coefficient of 0.876. Since this is slightly less, it will allow for a slightly larger load current range so the ADC values are close to the full range but will not overflow. The actual divider value is calculated with the following equation:

Equation 4:

$$Divider = \frac{R2}{R1 + R2}$$

Below are the measurements taken of the circuit at three voltage levels: 4.3 V, 3.9 V, and 3.6 V. Each level displays a graph displaying the difference between the measured and theoretical ADC values. Theoretical values are rounded to the closest whole integer. There is a summary graph to compare the differences at the three voltage levels. Afterwards there is a graph displaying the correlation between the theoretical ADC values and load current at the different voltage levels.

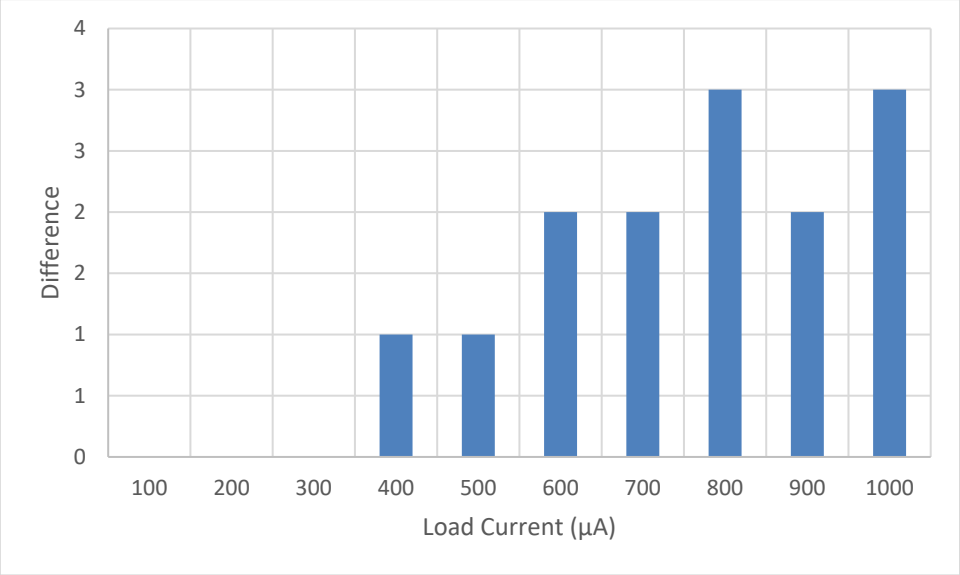


**Figure 2: Difference Between Measured and Theoretical ADC Values, VDD = 4.3 V**

**Table 4: Measured Values with VDD = 4.3 V**

| Load Current (µA) | ADC Code Measured | ADC Code Theoretical | Difference | Expected $V_{SENSE}$ |
|---|---|---|---|---|
| 100 | 18 | 18 | 0 | 4.2619 |
| 200 | 37 | 37 | 0 | 4.2238 |
| 300 | 55 | 55 | 0 | 4.1857 |
| 400 | 74 | 73 | 1 | 4.1476 |
| 500 | 93 | 92 | 1 | 4.1095 |
| 600 | 112 | 110 | 2 | 4.0714 |
| 700 | 130 | 128 | 2 | 4.0333 |
| 800 | 149 | 146 | 3 | 3.9952 |
| 900 | 167 | 165 | 2 | 3.9571 |
| 1000 | 186 | 183 | 3 | 3.919 |

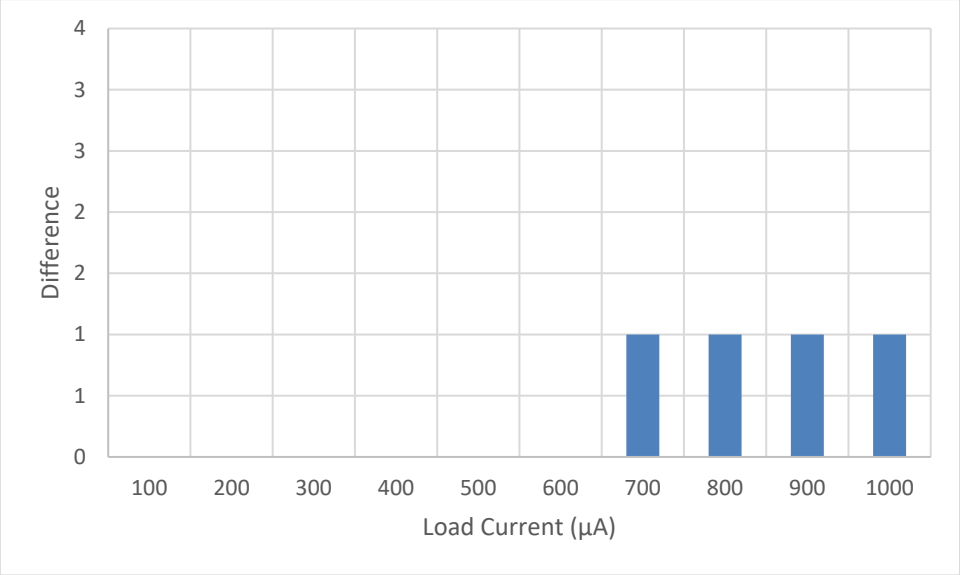


**Figure 3: Difference Between Measured and Theoretical ADC Values, VDD = 3.9 V**

**Table 5: Measured Values with VDD = 3.9 V**

| Load Current (µA) | ADC Code Measured | ADC Code Theoretical | Difference | Expected ACMP VIN |
|---|---|---|---|---|
| 100 | 20 | 20 | 0 | 3.8619 |
| 200 | 40 | 40 | 0 | 3.8238 |
| 300 | 61 | 61 | 0 | 3.7857 |
| 400 | 81 | 81 | 0 | 3.7476 |
| 500 | 101 | 101 | 0 | 3.7095 |
| 600 | 121 | 121 | 0 | 3.6714 |
| 700 | 142 | 141 | 1 | 3.6333 |
| 800 | 162 | 161 | 1 | 3.5952 |
| 900 | 183 | 182 | 1 | 3.5571 |
| 1000 | 203 | 202 | 1 | 3.519 |

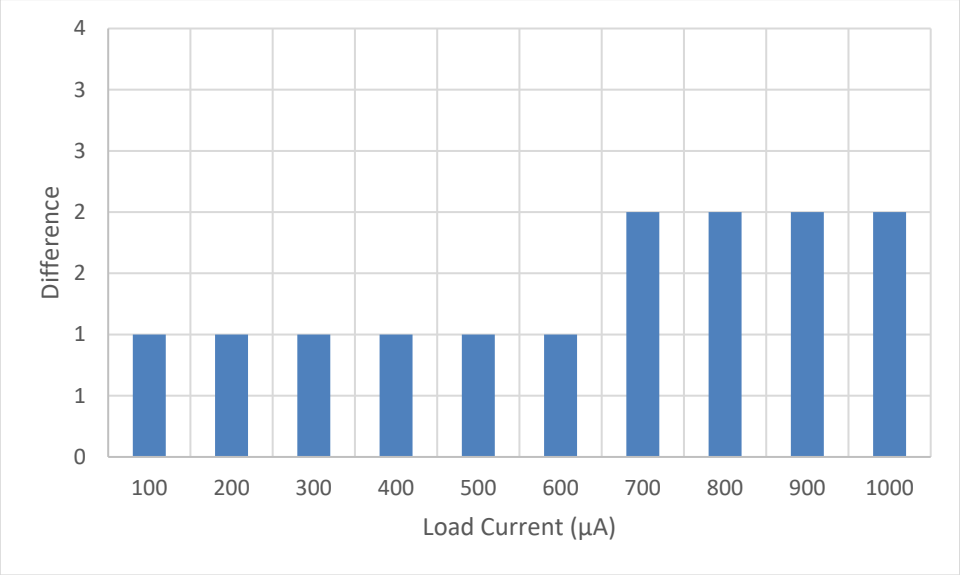


**Figure 4: Difference Between Measured and Theoretical ADC Values, VDD = 3.6 V**

**Table 6: Measured Values with VDD = 3.6 V**

| Load Current (µA) | ADC Code Measured | ADC Code Theoretical | Difference | Expected ACMP VIN |
|---|---|---|---|---|
| 100 | 23 | 22 | 1 | 3.5619 |
| 200 | 45 | 44 | 1 | 3.5238 |
| 300 | 67 | 66 | 1 | 3.4857 |
| 400 | 88 | 87 | 1 | 3.4476 |
| 500 | 110 | 109 | 1 | 3.4095 |
| 600 | 132 | 131 | 1 | 3.3714 |
| 700 | 155 | 153 | 2 | 3.3333 |
| 800 | 177 | 175 | 2 | 3.2952 |
| 900 | 199 | 197 | 2 | 3.2571 |
| 1000 | 221 | 219 | 2 | 3.219 |

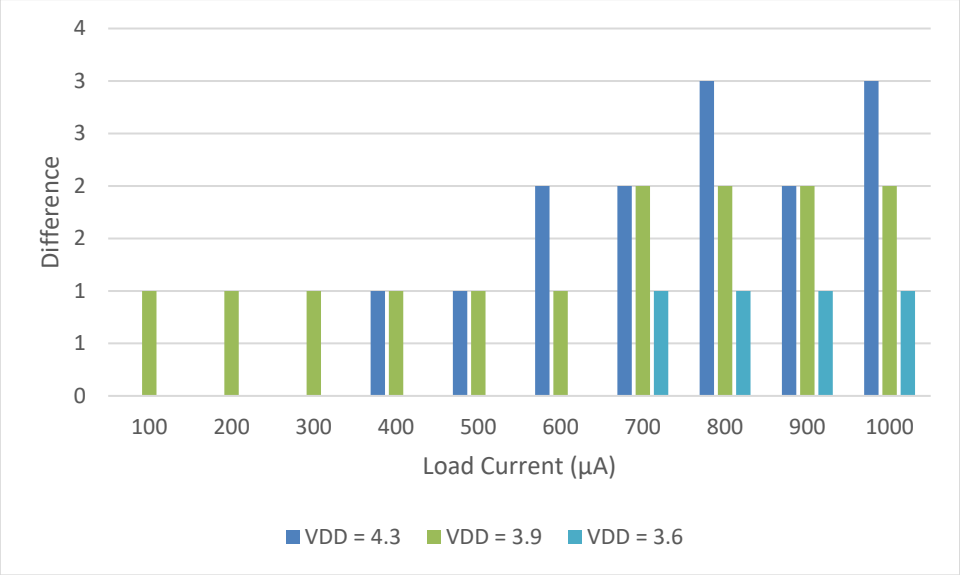


**Figure 5: Summary Graph of Differences between Measured and Theoretical ADC Values**

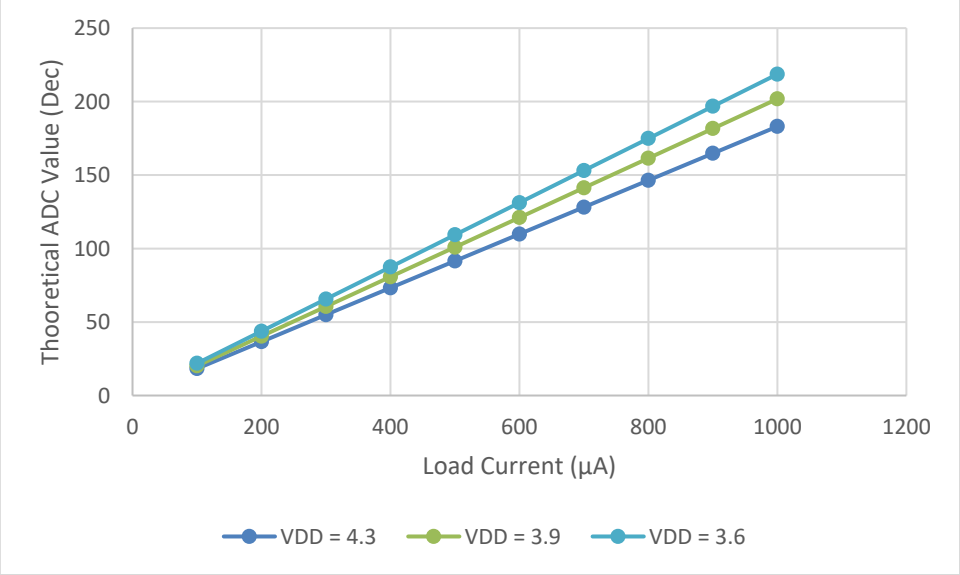


**Figure 6: Graph of Correlation between Theoretical ADC values and Load Current**

# 9 Conclusions

The device was tested at three voltage levels: 3.6 V, 3.9 V, and 4.3 V. The range of these voltages models a full lithium ion battery that discharges to its nominal level. Of the three voltage levels, it is observed that the device typically was more accurate at 3.9 V for the chosen external circuit. The difference between the measured and theoretical ADC values was only 1 decimal value off at load currents of 700 - 1000 µA. At the given voltage range, the measured ADC values were 3 decimal points above nominal conditions at the worst case. Further adjustments to the resistor divider can be made to optimize different VDD voltage levels.

# Appendix A

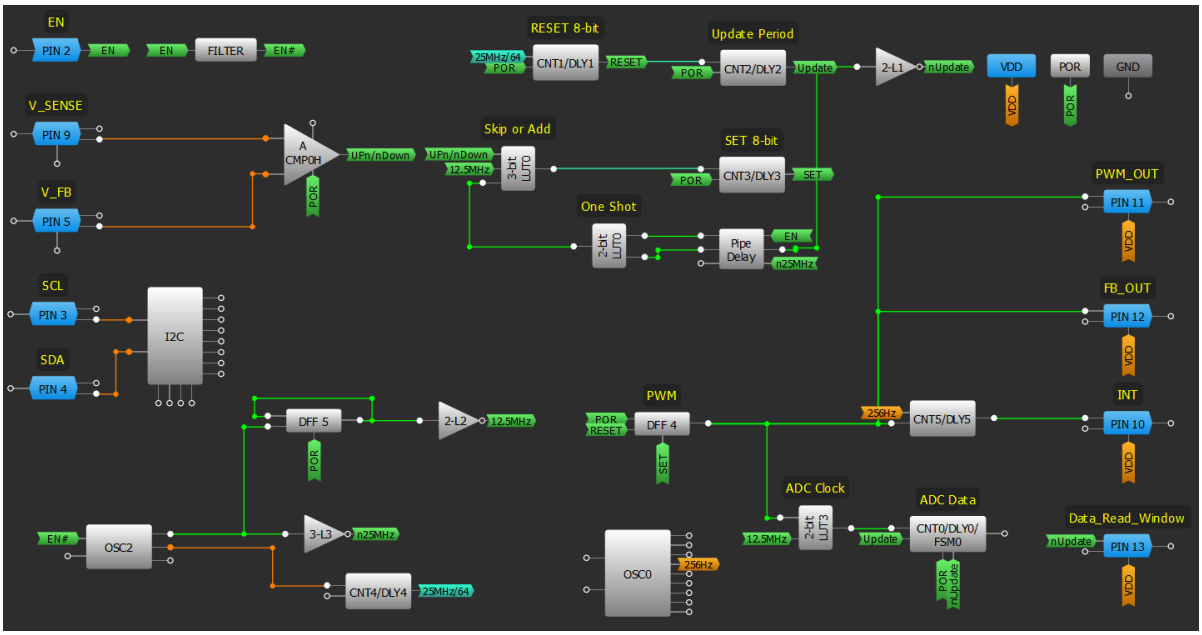


**Figure 7: View in GreenPAK Designer**

# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 23-Oct-2019 | Initial version |

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