Application Note

Alternative Single Wire Data Transmission using GreenPAK

AN-CM-294

Abstract

This application note introduces an alternative method of single wire data transmission using GreenPAK IC's. The proposed method is illustrated by a pair of transmitting parallel-to-serial converters that transmit the code to the corresponding receiving serial-to-parallel converters by a single-wire line.

This application note comes complete with design files which can be found in the References section.

Contents

Figures

Tables

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1 Terms and Definitions

DFF	D flip-flop
LUT	Lookup table
OSC	Oscillator
IC	Integrated circuit
CNT	Counter
DLY	Delay
DC	Duty cycle
P DLY	Programmable delay
FILTER	Internal RC filter
LED	Light emitting diode
DO	Digital output
Clock	Clock signal
Data	Data signal
VDD	Supply voltage
GND	Ground

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure™ Software Hub | Renesas, Software Download and User Guide

[2] AN-CM-294 Another Way of Single Wire Data Transmission using GreenPAK.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] AN-1186 Cyclic Redundancy Check Generator Unit for 1-wire Protocol, Application Note

[6] AN-1029 Adding nSETnRESET to DFF's, Application Note

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3 Introduction

Single-wire data transmission line is advantageous when operating numerous components of an electronic device, and high speed operation not required. At the same time, good flexibility of the system is required to quickly modify the design when needed. A partial list of advantages of this data transmission method includes reduced number of conductors, reduced size and cost of the final electronic product, increased reliability, etc. The purpose of this application note is to introduce an alternative method of single wire data transmission using GreenPAK IC's. In order to illustrate this method, new designs of transmitting and receiving converters by a single-wire line are presented. Compared to the existing methods (AN-1186), the proposed method seems simpler.

4 Main Idea of Method

Let us start with the classic integrating RC-element (Figure 1) and its properties. The integrating RC-element can be used in digital circuits to change the pulse length, or, more precisely, generate or extend the pulse duration, process the pulses using the integral law, etc. Let us take advantage of these properties of the integrating RC-element.

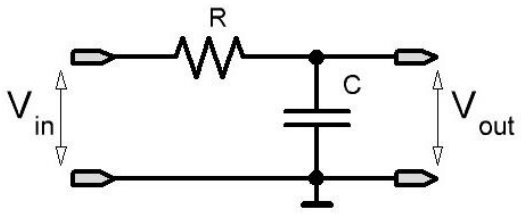

Figure 1: Integrating RC – Element

The voltage across the capacitor cannot be changed instantly. Its charge and discharge time depend on the capacitance value C, and the resistance of the resistor R. The charge/discharge time can be calculated using the time constant of the RC element according to the formula:

Equation 1:

$$\boldsymbol{\tau} = RC$$

Then applying a long pulse to the input of the integrating element, the capacitor will have time to fully charge and discharge. But if the pulse is short, much shorter than the time constant $\boldsymbol{\tau}$, then the capacitor C voltage will hardly change. In order to transmit the serial code, we need to have two data lines – “Data” and “Clock”. If to transmit “Data” with broad pulses that have time to recharge the capacitor of the RC element, and transmit “Clock” with narrow, short pulses that cannot pass through the integrating element, then it will be possible to combine these two lines into one. Thus, the integrating RC-element will serve as a separator for the signal receiver (Figure 2). It is necessary to take the “Clock” signal before the RC element with only the rising edge being important, and the “Data” signal after the RC element. If you now correctly generate the transmission signal of a bit sequence, then the problem is solved.

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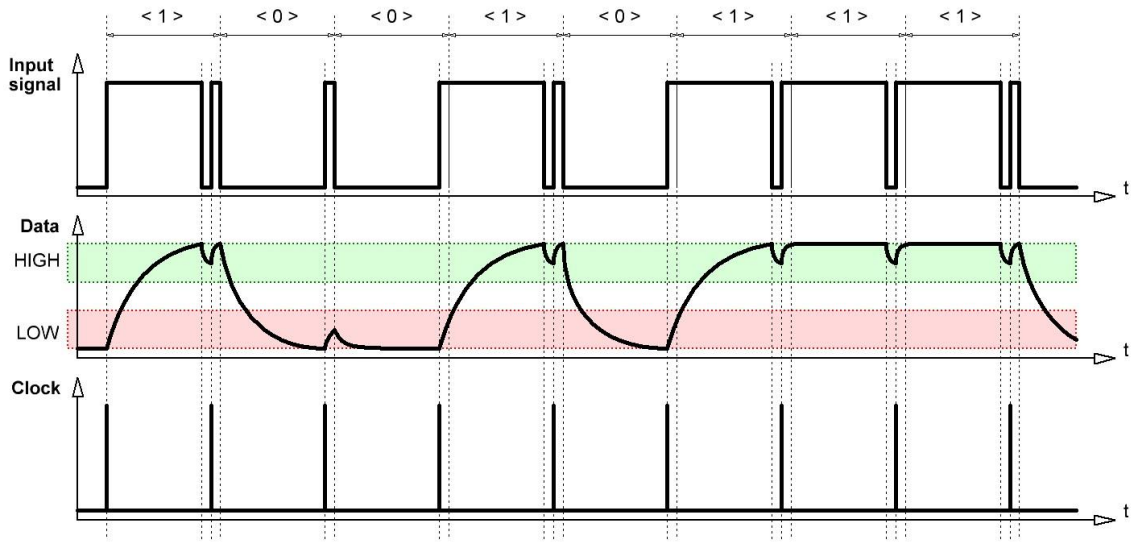

Figure 2: Separation of Signals by the Integrating RC – Element

Figure 2 shows an example of a byte "10010111" (Input signal) generated for transmission. One can readily see that in order to transmit logic data “one / zero”, it is necessary to generate a corresponding “high / low” sufficiently wide pulse, with a short “Clock” pulse at the end (Figure 3).

At this point, a careful reader may ask the question: why use an external RC element to separate the “Data” and “Clock” signals when this can be done directly in GreenPAK using the classical delay element? Looking ahead, we can say that the use of an external RC element allowed us to significantly reduce the current consumed by the receiver, as we no longer required an internal oscillator for the delay element to operate.

The “Data” signal voltage received after passing the RC element must be within a certain range of logic one voltage (green area in figure 2). The “Clock” signal voltage should not pass through the RC element and should not extend beyond the range of logic zero voltage (red area in Figure 2). There is an ambiguity area between them, where the existence of erroneous states is entirely possible. Therefore, the capacitor and resistor values must be selected so that all “charge / discharge” transient voltage values do not fall into this area. How to do this is shown below.

Let us consider the integrating RC element (Figure 1) as a series connection of resistor R and capacitor C. The following formula is used for such a circuit:

Equation 2:

$$V_{in} = V_R + V_C$$

Given that $V_R = IR = RC\frac{dV_C}{dt}$, we can write the following differential equation with respect to the capacitor voltage, which is the output voltage of our integrating element $V_C = V_{out}$:

Equation 3:

$$V_{in} = \tau\frac{dV_C}{dt} + V_C = \tau\frac{dV_{out}}{dt} + V_{out}$$

The solution of this differential equation is well known:

Equation 4:

$$V_{out} = V_{in}\left(1 - e^{-\frac{t}{\tau}}\right)$$

where τ – time constant (see eq. 1). Let us analyze this solution. At the initial time t = 0 when the input pulse is fed into the integrating element, the output voltage is $V_{out} = 0$, after which V_{out} starts to

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increase at a speed inversely proportional to the value of τ and reaches the following values (Table 1):

Table 1

Time	Result
t = 0	$V_{out} = 0$
t = τ /5	$V_{out} = V_{in}\left(1 - e^{-\frac{\tau/5}{\tau}}\right) = V_{in}\left(1 - e^{-\frac{1}{5}}\right) = V_{in}\left(1 - \frac{1}{\sqrt[5]{e}}\right) = V_{in}\left(1 - \frac{1}{\sqrt[5]{2.71828}}\right) \approx 0.181269 \cdot V_{in}$
t = τ /2	$V_{out} = V_{in}\left(1 - e^{-\frac{\tau/2}{\tau}}\right) = V_{in}\left(1 - e^{-\frac{1}{2}}\right) = V_{in}\left(1 - \frac{1}{\sqrt{e}}\right) = V_{in}\left(1 - \frac{1}{\sqrt{2.71828}}\right) \approx 0.393469 \cdot V_{in}$
t = τ	$V_{out} = V_{in}\left(1 - e^{-\frac{\tau}{\tau}}\right) = V_{in}(1 - e^{-1}) = V_{in}\left(1 - \frac{1}{e}\right) = V_{in}\left(1 - \frac{1}{2.71828}\right) \approx 0.63212 \cdot V_{in}$
t = 2τ	$V_{out} = V_{in}\left(1 - e^{-\frac{2\tau}{\tau}}\right) = V_{in}(1 - e^{-2}) = V_{in}\left(1 - \frac{1}{e^2}\right) = V_{in}\left(1 - \frac{1}{2.71828^2}\right) \approx 0.8646647 \cdot V_{in}$
t = 3τ	$V_{out} = V_{in}\left(1 - e^{-\frac{3\tau}{\tau}}\right) = V_{in}(1 - e^{-3}) = V_{in}\left(1 - \frac{1}{e^3}\right) = V_{in}\left(1 - \frac{1}{2.71828^3}\right) \approx 0.95021 \cdot V_{in}$
t = 4τ	$V_{out} = V_{in}\left(1 - e^{-\frac{4\tau}{\tau}}\right) = V_{in}(1 - e^{-4}) = V_{in}\left(1 - \frac{1}{e^4}\right) = V_{in}\left(1 - \frac{1}{2.71828^4}\right) \approx 0.981684 \cdot V_{in}$

As described below, the time characteristics of the bit sequence transmission signals in our transmitter design is as shown in Figure 3. The RC elements with the following values were used in construction of our receiver: R = 120 Ω, C = 10 nF, τ = 1.2 μs (Figure 12, Figure 13). Thus, it is possible to calculate the resulting voltage obtained when the pulses with such durations pass through the RC element. The “Data” pulse with a duration of T1 = 5 μs will fit the case of t = 4τ (more precisely, t = 4,17τ) (Table 1). At a voltage of VDD = 3.3 V the output voltage after the RC element will be $V_{out} = 0.981684 \cdot 3.3\,V \approx 3.23\,V$, that is, the logic HIGH level, which is what we need. However, the short pulse T2 = 240 ns must be filtered out by the RC element. The case of t = τ /5 will be valid for the “Clock” pulse with a duration of T2 = 240 ns (Table 1). At a voltage of VDD = 3.3 V the output voltage after the RC element will be $V_{out} = 0.181269 \cdot 3.3\,V \approx 0.59\,V$, so the “Clock” pulse will not pass through the RC element significantly. For checking purposes, let us compare the resulting signal voltage levels with the characteristic logic “zero / one” voltage levels of the respective GreenPAKs. This comparison is made for the case when the supply voltage is VDD = 3.3 V (Table 2).

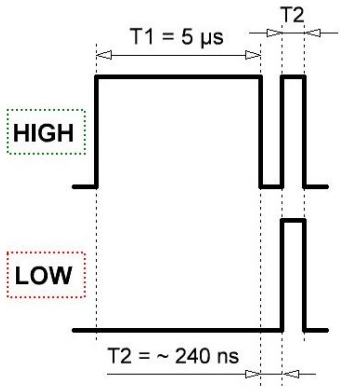

Figure 3: Form of "HIGH/LOW" Signals

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Table 2

Voltage ranges	GreenPAK3 SLG46170	GreenPAK5 SLG46533	"Data" signal voltage after RC circuit	"Clock" signal voltage after RC circuit
HIGH level	3.30 V	3.30 V	3.23 V	
	1.59 V	1.64 V		
zone of ambiguity				
LOW level	1.39 V	1.44 V		0.59 V
	0.0 V	0.0 V		

The resulting logic level voltages of "Data" and "Clock" signals are guaranteed to correspond to the required logic "zero / one" voltage values and do not fall into the ambiguity area. Summarizing all the above-mentioned information, there are two main criteria for selecting an integrating RC element to separate the "Data" and "Clock" signals:

- The signal duration T1 at the selected signal transmission frequency should be at least 3 times (in our case 4.17 times) greater than the time constant of the RC element τ :

Equation 5:

$$T1 = 3\tau$$

- The duration of the short "Clock" pulse T2 at the end of the transmission signal should be at least 4 times (in our case 5 times) shorter than the time constant of the RC element τ :

Equation 6:

$$T2 = \tau / 4$$

5 Designs Analysis

The design of "Transmitter_170" (Figure 4) consists of two main components:

- parallel-to-serial converter based on 2-bit LUT1, 3-bit LUT0 ÷ 3-bit LUT5, 3-bit LUT9, DFF0 ÷ DFF6, Pipe Delay;
- generator of the necessary bit sequence transmission signal based on CNT1, CNT4, DLY2, DLY5, 2-bit LUT2, 2-bit LUT3, 3-bit LUT6, 4-bit LUT0, FILTER0, P DLY.

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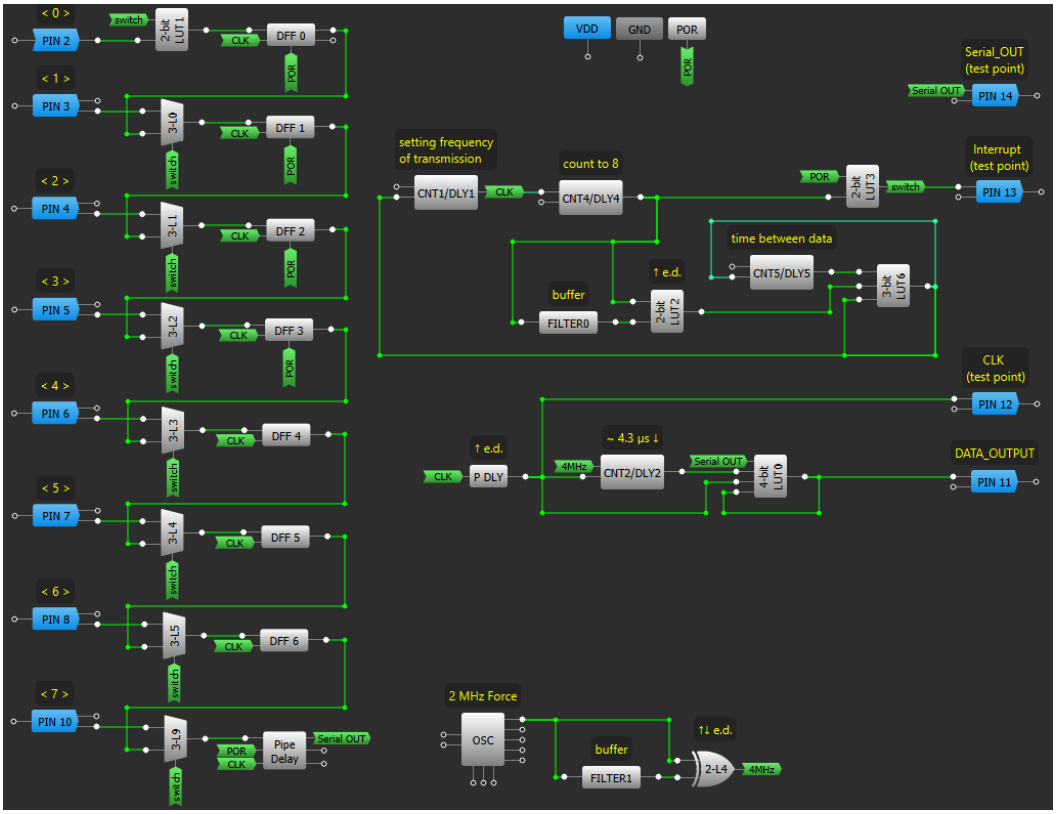

Figure 4: "Transmitter_170" Design

The CNT1 counter defines the transmission signal time (as already mentioned, it was set at ~ 5 µs). The CNT4 counter forms a packet of eight such time periods and controls the 2-bit LUT1, 3-bit LUT0 ÷ 3-bit LUT5, 3-bit LUT9 multiplexers using the 2-bit LUT3 inverter. When the internal "switch" signal coming from the output of the 2-bit LUT3 inverter is low (Figure 5, "Interrupt" signal), the recording of information from the input PIN #2, #8, #10 through the multiplexers to the corresponding triggers is performed. And then, when the "switch" ("Interrupt" signal) signal goes high, there is a shift of data on the triggers and a serial code is formed (Figure 5, "Serial_OUT" signal). The delay element DLY5 together with the 3-bit LUT6 elements and the rising edge detector based on FILTER0 and 2-bit LUT2 allow changing the time duration t2 (Figure 5, b) between the generated data packets, that is, setting the duration of parallel data output. When the "switch" ("Interrupt" signal) signal is low, a parallel code is generated in the corresponding design of the receiving converter. In our designs, the time of the generated data packet t1 and the generation time t2 are roughly the same.

The generated serial code coming from the output of the last Pipe Delay trigger is fed into the 4-bit LUT0, element, where, using the delay element DLY2 and the rising edge detector P DLY, the desired specific form of the output signal is formed (Figure 5, "DATA_OUTPUT" signal). The rising and falling edge detector consisting of FILTER1 and 2-bit LUT4 is designed to double the oscillator clock frequency for the delay element DLY2 in order to increase the resolution of delay time settings.

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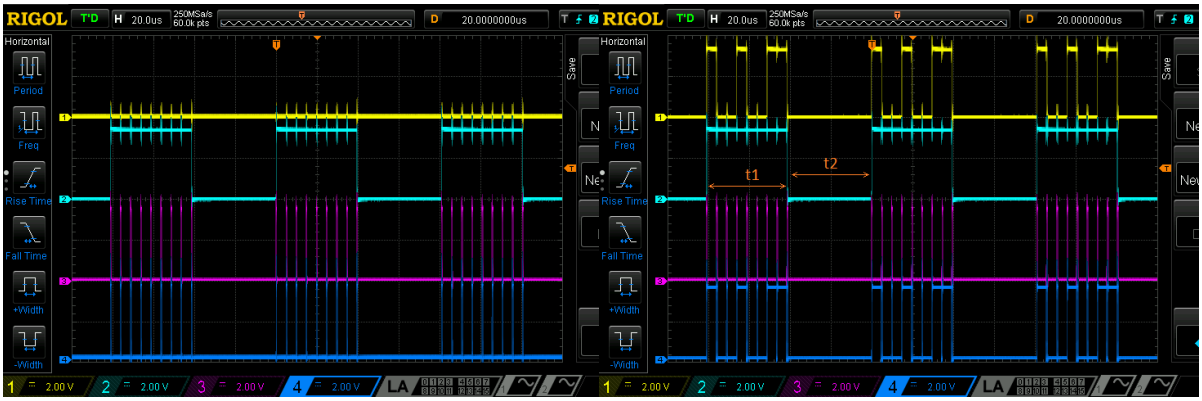
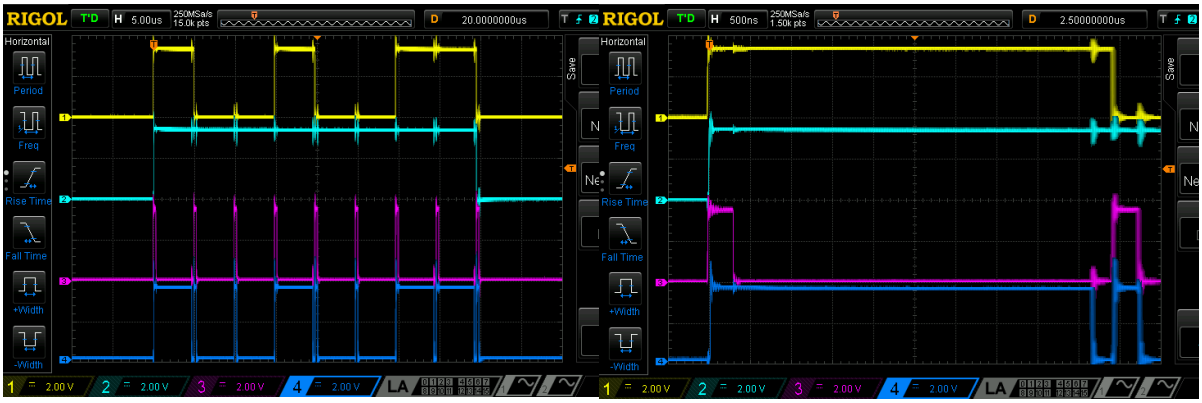


a (Input Signal from Buttons is 00000000) **b (Input Signal from Buttons is 10010011)**



c (Input Signal from Buttons is 10010011) **d (Zoomed One Period, HIGH Signal)**

Channel 1 (yellow/top line)	–	PIN#14 (Serial_OUT)	/test point/
Channel 2 (light blue/2nd line)	–	PIN#13 (Interrupt)	/test point/
Channel 3 (magenta/3rd line)	–	PIN#12 (CLK)	/test point/
Channel 4 (blue/bottom line)	–	PIN#11 (DATA_OUTPUT)	

Figure 5: Scope Shots of "Transmitter_170" Design

The design of “Receiver_170” (Figure 6) performs the inverse function of converting the serial code to parallel. For this operation, the design uses:

- a chain of eight triggers based on Pipe Delay (three triggers), DFF0 ÷ DFF3 and DFF5;
- eight latches based on 3-bit LUT0 ÷ 3-bit LUT7 for sending the parallel code to the output PINs;
- circuit of clocking the triggers' chain on the rising edge detector P DLY;
- the latches control circuit (3-bit LUT0 ÷ 3-bit LUT7 elements) on CNT2 counter and FILTER0 inverter.

After the signals are separated by an external RC element (Figure 12) the “Data” signal coming from the input PIN#2 (Figure 7) is fed into the first trigger of the trigger chain. Then, we select only the rising edge of the “Clock” signal PIN#5 using the P DLY detector and form a clock signal for the trigger chain and counter CNT2. When the internal “CNT2” signal is low (Figure 7, “CNT2” signal) the serial code is decoded into the parallel code on the trigger chain, where triggers are in operation due to the high “resDFF” signal coming from the output of the FILTER0 inverter.

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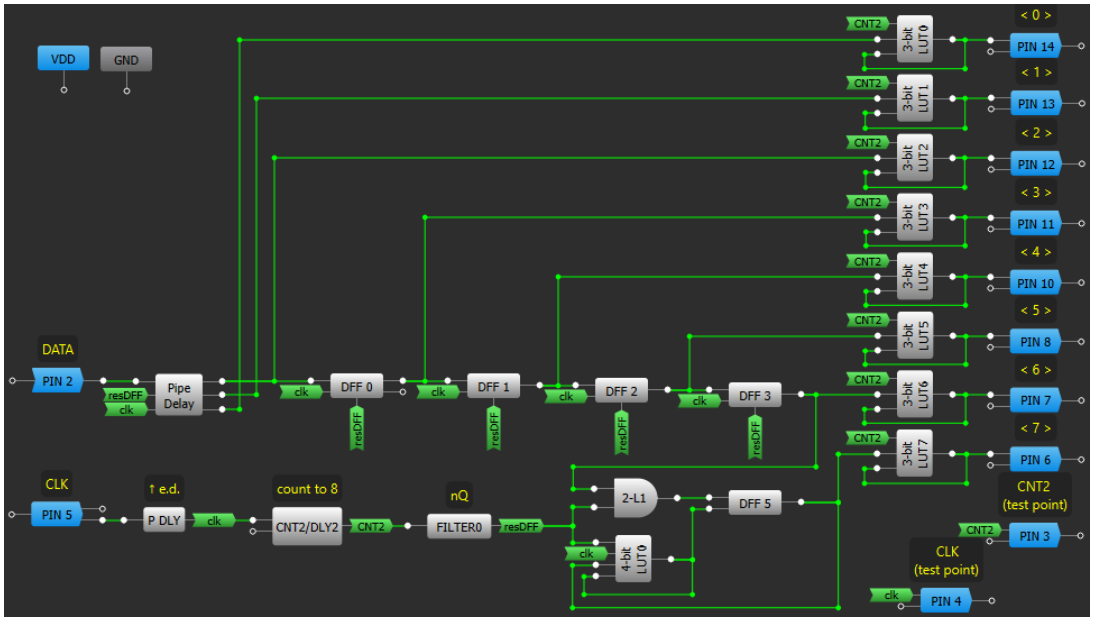
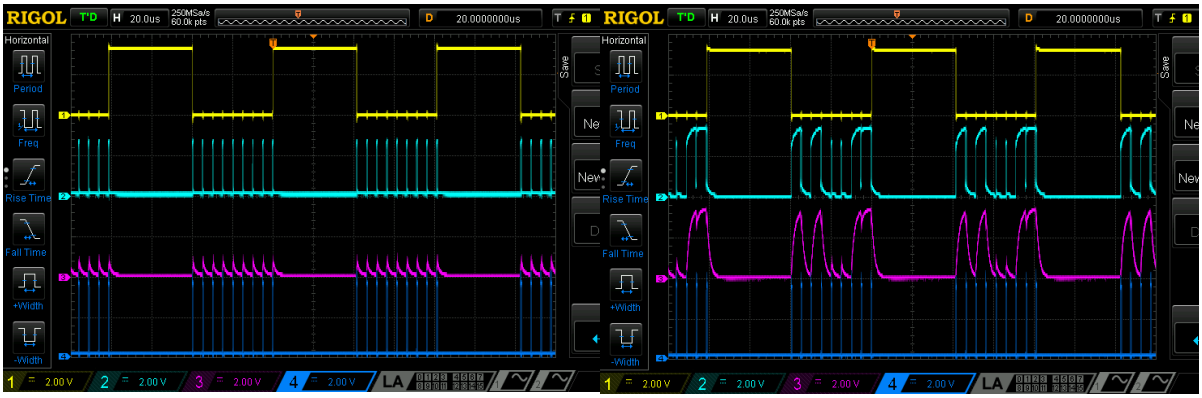


Figure 6: "Receiver_170" Design

The signal indicating the current state of each trigger is fed to the respective latch and stored when the “CNT2” signal changes from low to high. At the same time, the triggers of the decoding chain are reset to the initial state, as the “resDFF” signal changes from high to low. The latch stored signal is fed to the corresponding output PIN during the time when the “CNT2” signal is high, and this timing corresponds to the time t2 between the generated data packets in the “Transmitter_170” design.

The DFF5 trigger does not have an nRESET output. Therefore, it has an additional reset logic circuit based on 4-bit LUT0 and 2-bit LUT1 elements as described in AN-1029 [6].



a (Input Signal from Buttons is 00000000) **b (Input Signal from Buttons is 10100011)**

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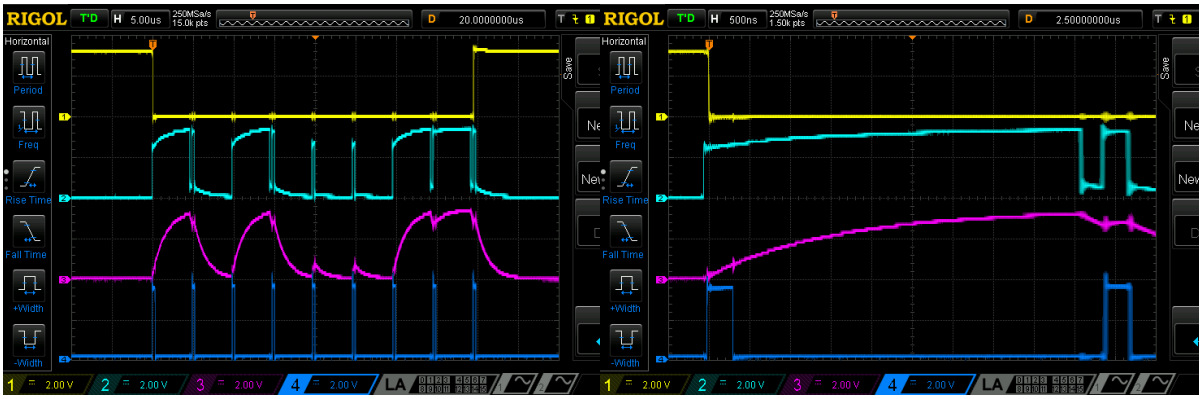

c (Input Signal from Buttons is 10100011) **d (Zoomed One Period, HIGH Signal)**

Channel 1 (yellow/top line)	–	PIN#3 (CNT2) /test point/
Channel 2 (light blue/2nd line)	–	external signal, before RC – circuit, to PIN#5
Channel 3 (magenta/3rd line)	–	external signal, after RC – circuit, to PIN#2
Channel 4 (blue/bottom line)	–	PIN#4 (CLK) /test point/

Figure 7: Scope Shots of "Receiver_170" Design

Looking carefully at the initial conditions when starting up the “Transmitter_170” and “Receiver_170”, one can notice one drawback. If the receiver starts its operation later than the transmitter, then it may happen that conversion of serial code to parallel does not start from the beginning of the data packet, but from the middle, for example. This, in turn, will cause a shift in the data output process. Thus, in order to ensure correct operation of the transmitter-receiver, it is necessary for the receiver to start operating simultaneously with the transmitter, in other words, they must have a common power source (Figure 12). One way to eliminate this drawback is to transmit a service, auxiliary signal at the beginning of each data packet to reset all triggers in the receiver design before starting the process of converting serial data. This will ensure that the process of data conversion starts at the beginning of the package. This way we will get a reliable data transmission system, where the transmitter and receiver can have their own power sources, can start operating at any time, independently of each other. To test this, the design was modified to “Transmitter_533” and “Receiver_533” (Figure 13).

The design of “Transmitter_533” (Figure 8) also consists of two main components:

- parallel-to-serial converter based on 2-bit LUT3, 3-bit LUT14 ÷ 3-bit LUT17, 3-bit LUT5 ÷ 3-bit LUT7, DFF2, DFF0, DFF5 ÷ DFF9, Pipe Delay;
- generator, that generating the necessary bit sequence transmission signal based on CNT5, CNT6, DLY0, DLY1, DFF4, 3-bit LUT0, 3-bit LUT13, EDGE DET0, P DLY, 4-bit LUT2, and 2-bit LUT1.

The operational principle of this design is no different from the previous one. Similarly, the CNT5 counter defines the transmission signal time (5 µs). Unlike the previous design, the CNT6 counter forms a packet of ten such time periods. That is, apart from eight periods designed to transmit data, there are two additional time periods S1, S0 used to generate the required service signals (Figure 9, c).

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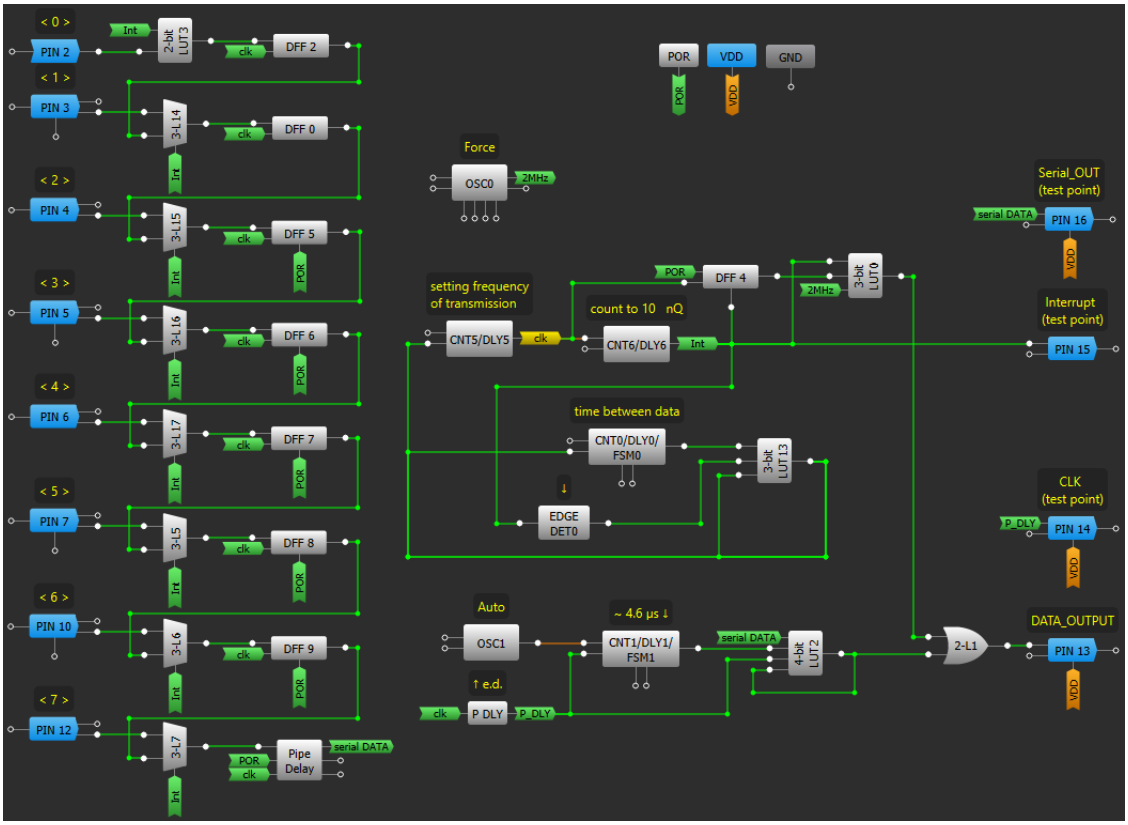
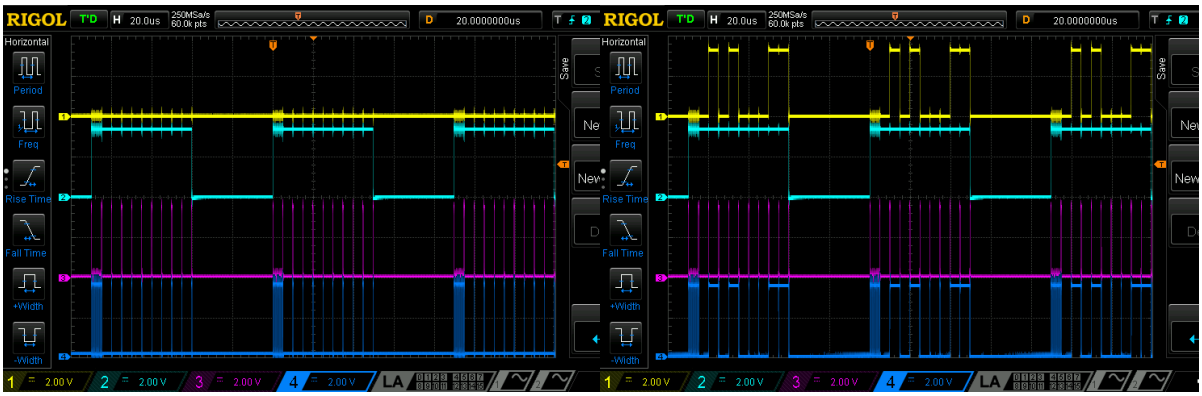


Figure 8: "Transmitter_533" Design

There may be many ways to create a special service signal, and then detect it in the receiver. We chose the first one that came to mind. Using DFF4 and 3-bit LUT0 the S1 time period of the service signal is filled with an oscillator frequency (2 MHz) and mixed with the main transmission signal using 2-bit LUT1. The S0 period is left without any changes (Figure 9, d). The reasons for this will be explained in the description of the receiver design.

Like in the previous transmitter design, the delay element DLY0 together with the 3-bit LUT13 elements and the falling edge detector EDGE DET0 allow changing the time duration between the generated data packets. The desired specific form of the output signal (Figure 3) is formed, like in the previous case, on the basis of DLY1, 4-bit LUT2 and P DLY. Since the data package consists of ten time periods, it is necessary to add two triggers to the chain to correctly generate the serial code. This is done with a Pipe Delay, where OUT0 is set at = 3.



a (Input Signal from Buttons is 00000000) **b (Input Signal from Buttons is 10100011)**

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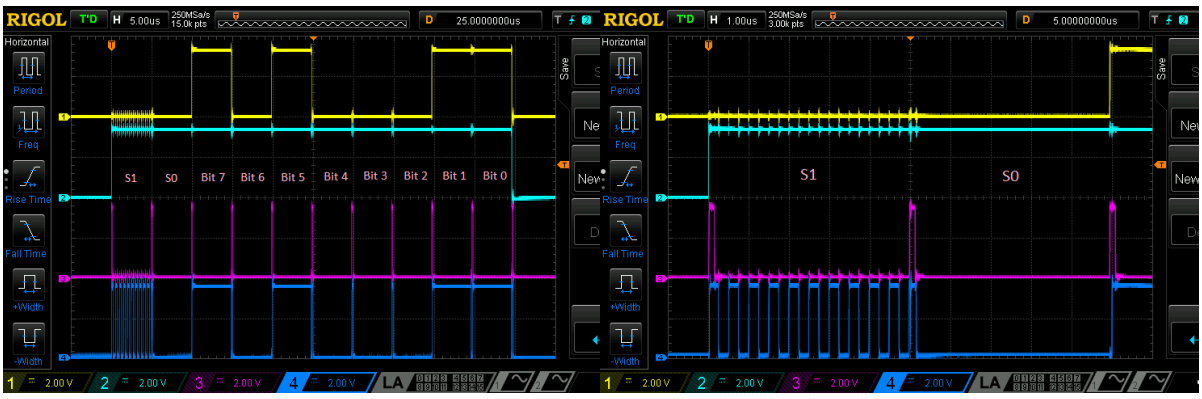

c (Input Signal from Buttons is 10100011) **d (Zoomed First Two Periods of Service Signal)**

Channel 1 (yellow/top line)	–	PIN#16 (Serial_OUT)	/test point/
Channel 2 (light blue/2nd line)	–	PIN#15 (Interrupt)	/test point/
Channel 3 (magenta/3rd line)	–	PIN#14 (CLK)	/test point/
Channel 4 (blue/bottom line)	–	PIN#13 (DATA_OUTPUT)	

Figure 9: Scope Shots of "Transmitter_533" Design

So, besides the data byte, there are two additional bits S1 and S0 transmitted in the design of “Transmitter_533”. The S1 bit is filled with a periodic signal with an oscillator frequency of 2 MHz.

The design of “Receiver_533” (Figure 10), like the previous one, performs the inverse function of decoding the serial code into the parallel one, and besides, detects the service signal (generated by the transmitter) and resets all triggers before starting the process of converting serial data.

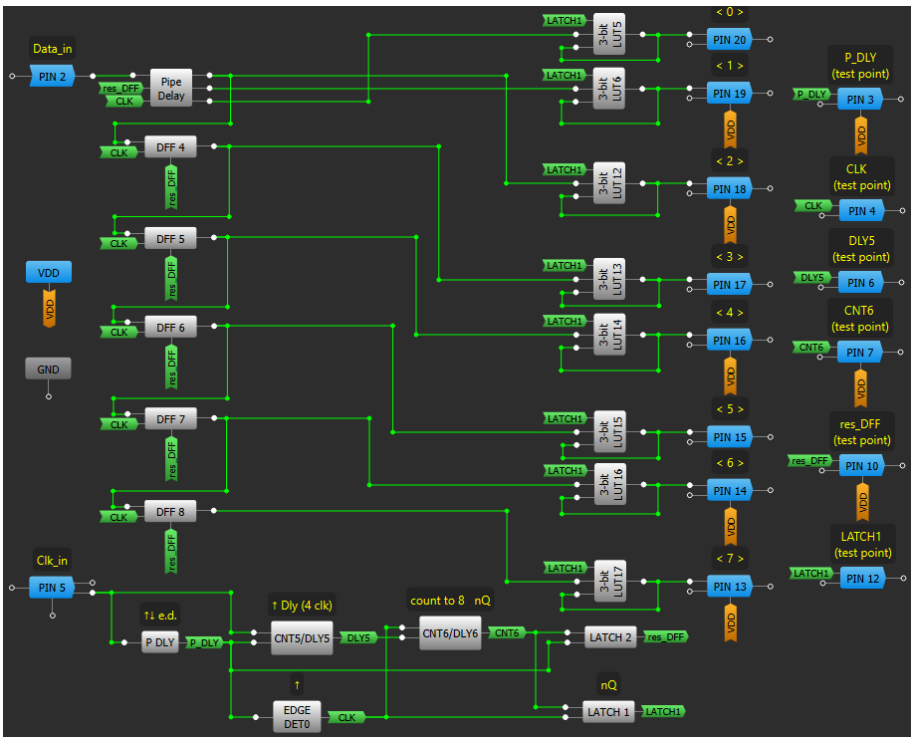

Figure 10: "Receiver_533" Design

To perform this function, the DLY5 delay element is used, where PIN #5 serves as a clock signal source, that is, the “Clock” signal before the RC element. The response of the detector P DLY of both edges to the periodic signal (at 2 MHz frequency) filling the additional S1 bit will be similar to the filter

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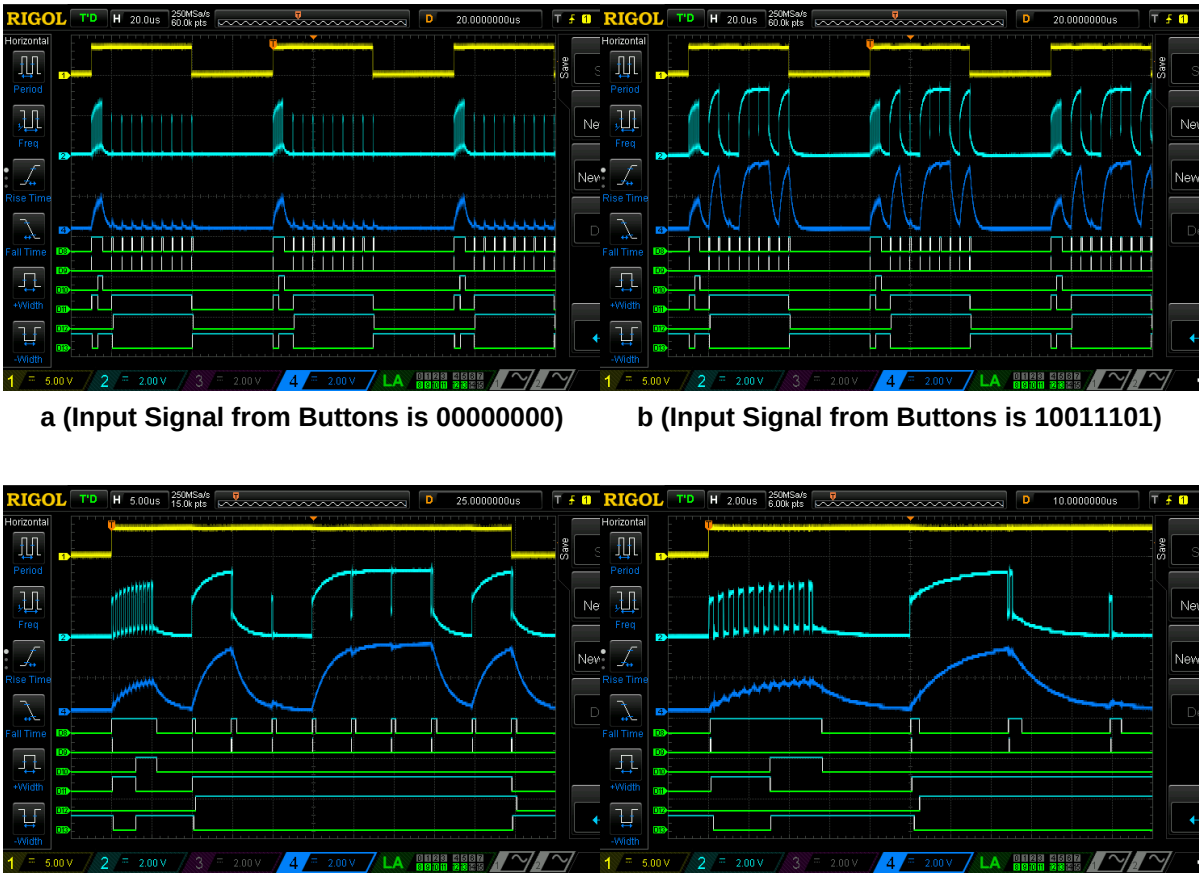
response, i.e. it is possible to generate a launch signal for DLY5 (Figure 11, “P_DLY” signal). DLY5 is a delay element on the rising edge, that is why one can readily see that DLY5 will work only when the additional S1 bit arrives (Figure 11, “DLY5” signal). In its turn, the DLY5 delay element will generate a reset signal for the CNT6 counter always before starting parallel-to-serial conversion. In this way, the CNT6 counter and two latches LATCH1, LATCH2 will generate the necessary signals to reset triggers (Figure 11, “res_DFF” signal) in the decoding chain, and the signal for latching data in the output latches 3-bit LUT5, 3-bit LUT6, 3-bit LUT12 ÷ 3-bit LUT16 during the parallel data output (Figure 11, “LATCH1” signal).



a (Input Signal from Buttons is 00000000) **b (Input Signal from Buttons is 10011101)**

c (Input Signal from Buttons is 10011101) **d (Zoomed First Two Periods of Service Signal)**

Channel 1 (yellow/top line)	–	PIN#15 (Interrupt) /test point/
Channel 2 (light blue/2nd line)	–	external signal, before RC – circuit, to PIN#5
Channel 4 (blue line/3rd line)	–	external signal, after RC – circuit, to PIN#2
D8	–	PIN#3 (P_DLY) /test point/
D9	–	PIN#4 (CLK) /test point/
D10	–	PIN#6 (DLY5) /test point/
D11	–	PIN#7 (CNT6) /test point/
D12	–	PIN#10 (res_DFF) /test point/
D13	–	PIN#12 (LATCH1) /test point/

Figure 11: Scope Shots of "Receiver_533" Design

Although the signal with a frequency of 2 MHz filling the additional S1 bit meets the requirement for "not passing the RC element" (see eq. 6), but, due to its multiple repetitions during 5 µs (duration of one bit chosen by us), it manages to charge the capacitor to a voltage level that can be identified as

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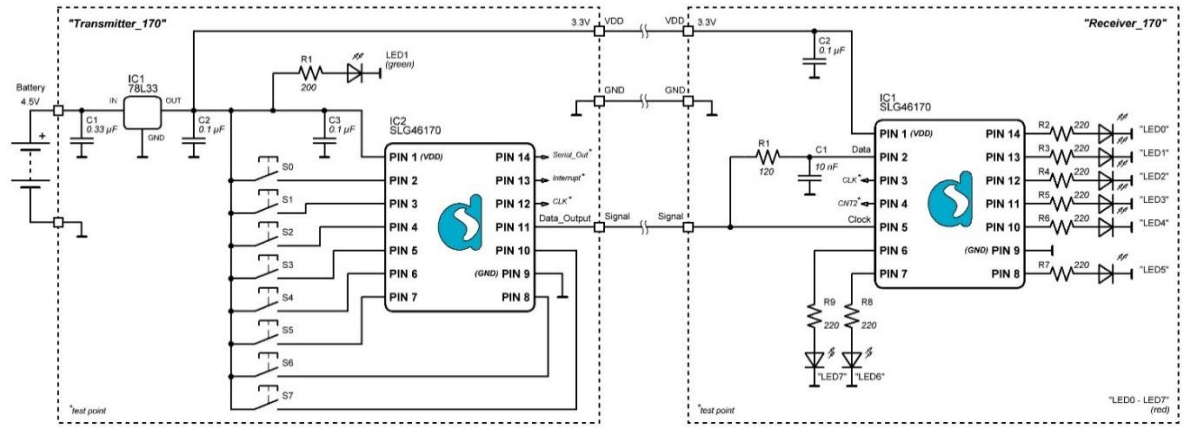
a logic one. Then, to allow the capacitor to discharge to a guaranteed logic zero level and not be able to affect Bit 7 of the data signal, we use the second additional S0 bit. Also, to improve the reliability of the system, the clock signal for the trigger chain and counter CNT6 is formed by the rising edge detector EDGE DET0, where the signal is taken after the P DLY element. This, in turn, will prevent generation of a parasitic clock signal “CLK” during decoding of service S1 bit. (Figure 11, “CLK” signal).

The rest of the elements perform the same functions as in the previous design.

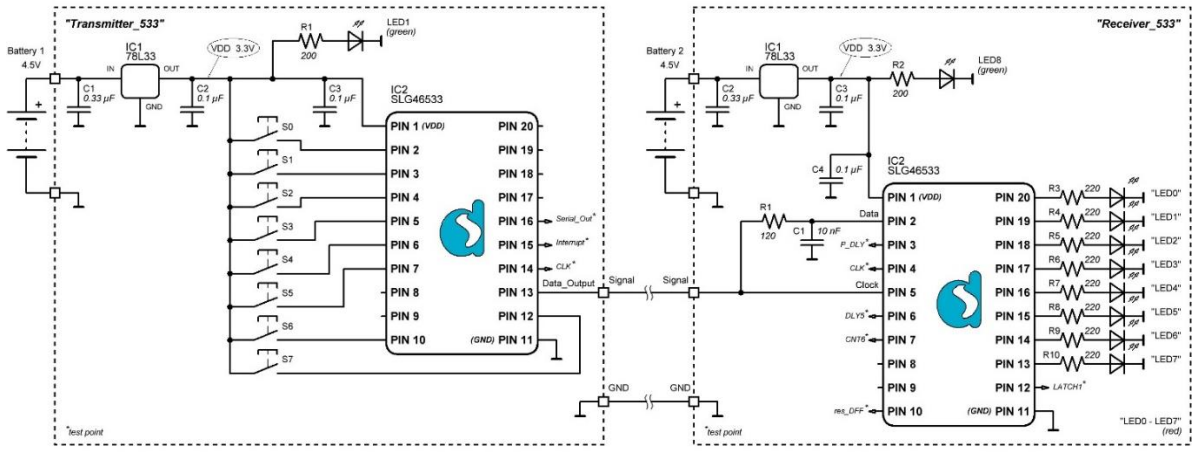
6 Circuit Analysis

As already mentioned, to demonstrate the efficiency of the presented data transmission principle, we created a pair of transmitter-receiver devices (Figure 14). The figures below present the basic circuit diagrams of these devices.



a “Transmitter 170” Device **b “Receiver 170” Device**

Figure 12: Test Circuit of “Transmitter_170 – Receiver_170" Pair



a “Transmitter_533” Device **b “Receiver_533” Device**

Figure 13: Test Circuit of “Transmitter_533 – Receiver_533" Pair

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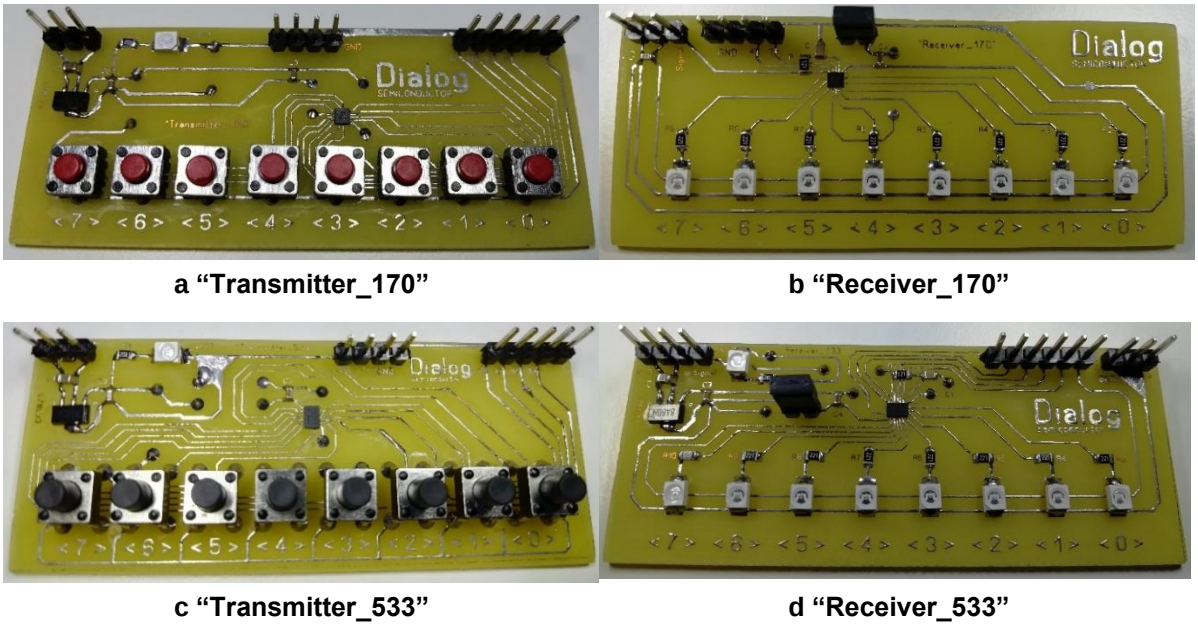

a “Transmitter_170” **b “Receiver_170”**

c “Transmitter_533” **d “Receiver_533”**

Figure 14: Test Board Photos

As mentioned above, the “Transmitter_170 – Receiver_170” pair (Figure 12) share a common 3.3V power supply from the 78L33 regulator. There are eight buttons S0 - S7 used in the transmitter circuit to generate the desired transmission signal. Accordingly, the eight LED0 - LED7 LEDs in the receiver circuit serve to visualize the received and decoded signal.

The transmitter and receiver in the “Transmitter_533 – Receiver_533” pair (Figure 13) have independent power supply nodes, and as described above, represent an independent data reception – transmission system. Similar to the previous circuit, the buttons S0 - S7 can be used to set the desired transmission signal and the result can be monitored by the LED0 - LED7 LEDs in the receiver circuit.

We have measured the current consumed by the IC's during the operation of the presented pairs of transmitter – receiver: IC1 circuit of “Receiver_170” and IC2 circuit of “Receiver_533”, together with their R1C1 elements, without taking into account the current consumed by LEDs. As it turned out, the measured current values also depend on the number of logical ones transmitted in the byte of the serial signal (this is due to the charge current of the capacitor of RC element). For comparison, the measurement results are summarized in Table 3.

Table 3

Data Byte	Current consumption	
	“Receiver_170”	“Receiver_533”
0 0 0 0 0 0 0 0	7.9 µA	17.0 µA
0 0 0 0 0 0 0 1	11.2 µA	20.0 µA
0 0 0 0 0 0 1 1	12.6 µA	22.2 µA
0 0 0 0 0 1 1 1	14.0 µA	23.3 µA
– // –	– // –	– // –
1 1 1 1 1 1 1 1	19.8 µA	27.6 µA
If we will use internal OSC (2MHz)	~ 80 µA	~ 60 µA

The measured current values indicate that the current consumed by the IC of “Receiver_533” circuit is slightly higher than the current of the “Receiver_170” circuit. This is due to the fact that the

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transmission signal in the “Receiver_533” circuit is longer by two bits due to the use of additional auxiliary service bits S1, S0.

Therefore, it can be summed up that the current consumed by the IC with RC element is much less than the current consumed by the IC with the OSC 2 MHz oscillator on.

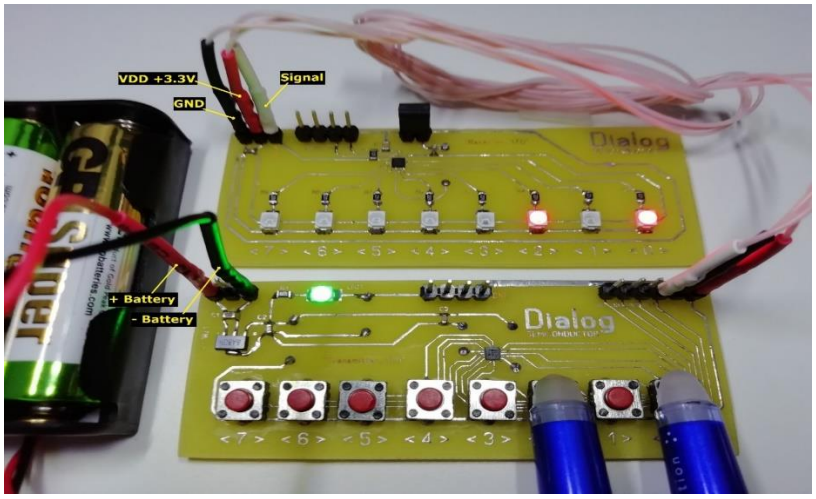

Figure 15: Photo of Working “Transmitter_170 – Receiver_170” System

(Input Signal from Buttons is 00000101)

Figure 15 and Figure 16 demonstrate the operating data transmission-reception system based on the operational principle presented above.

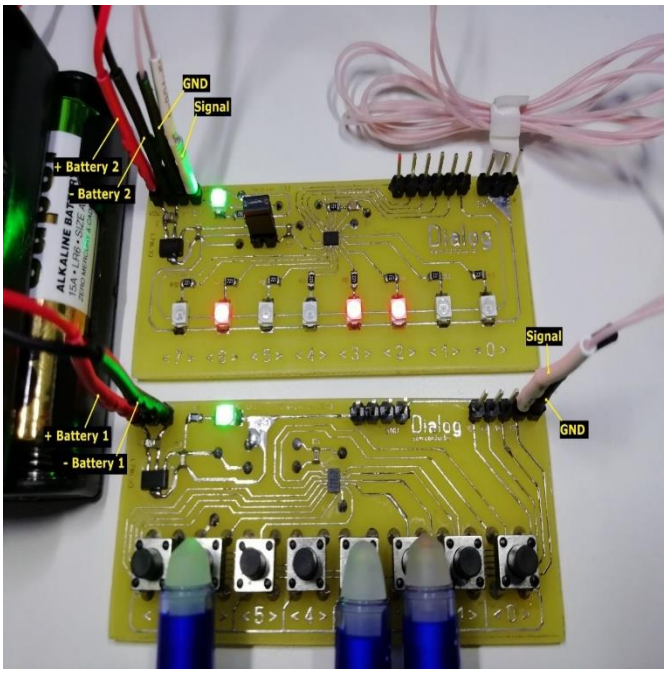

Figure 16: Photo of Working “Transmitter_533 – Receiver_533” System

(Input Signal from Buttons is 01001100)

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7 Conclusions

The proposed alternative method of transmitting serial data over a single-wire line using the GreenPAK products is quite efficient and competitive. This is fully confirmed by two data transmission-reception systems based on this principle, and comprehensive tests of their operation.

The GreenPAK products are an ideal solution for the development of this kind of system due to the large number of functional elements necessary for implementation of a variety of circuit design solutions. And this, in turn, allows a significant reduction in the number of external circuit elements. Additional advantages of GreenPAK products are quick design time and configurability, low power consumption, small board area, and low cost.

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Revision History

Revision	Date	Description
1.0	03-Jun-2020	Initial version

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