Enhancing LDO PSRR and Noise Performance Measurements Using Capacitors with Low Parasitic Parameters

SLG51003V

This application note introduces the concept of Power Supply Rejection Ratio (PSRR) and illustrates how to measure and correctly evaluate the PSRR of low voltage dropout regulators, factoring in the influence of the parasitic parameters of the capacitors used.

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Terms and Definitions

PSRR	Power Supply Rejection Ratio
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
PMIC	Power Management Integrated Circuit
LDO	Low Dropout Output

References

For related documents and software, please visit:

Power GreenPAK™ | Renesas

Renesas Electronics provides a complete library of application notes [1] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Application Notes, GreenPAK Application Notes webpage, Renesas Electronics
[2] SLG51000C Datasheet, SLG51000C Datasheet, Renesas Electronics
[3] SLG51001C Datasheet, SLG51001C Datasheet, Renesas Electronics
[4] SLG51002C Datasheet, SLG51002C Datasheet, Renesas Electronics
[5] SLG51003V Datasheet, SLG51003V Datasheet, Renesas Electronics

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1. Introduction

Low-dropout (LDO) voltage regulators are essential components in electronic systems that provide a stable output voltage by regulating the input voltage. However, LDO performance can be affected by power supply noise and fluctuations. Power supply rejection ratio (PSRR) is a measure of an LDO's ability to reject these power supply variations and maintain a stable output voltage. This introduction provides an overview of this technical application note, which focuses on enhancing the power supply rejection ratio (PSRR) and the noise performance of LDOs via the use of capacitors with low parasitic parameters.

2. Description

2.1 Introduction to Low-Dropout Voltage Regulators (LDOs) and their critical role in maintaining a stable output voltage

This technical application note explores the challenges of using LDOs to maintain a stable output voltage and provides insights into optimizing LDO performance. We delve into the intricacies of PSRR, noise in LDOs, and the critical conditions to acquire accurate PSRR measurements. Furthermore, we investigate the requirements for using output capacitors with low parasitic parameters to enhance LDO stability and efficiency. The use of capacitors with low Equivalent Series Inductance (ESL) and low Equivalent Series Resistance (ESR) is dissected in detail.

In the quest for high efficiency, we explore strategies to minimize voltage drop across the LDO (V_{DROP}), and consider power sequencing techniques to reduce working time, especially in applications with limited power availability.

Through practical considerations, real-world examples, and case studies, we aim to provide actionable insights for engineers and designers seeking to optimize LDO performance. The following sections will describe these topics, offering a comprehensive guide to understanding and addressing the intricacies of LDOs in electronic systems.

LDOs are particularly valued in applications where power efficiency and space are critical, such as in battery-powered devices, portable electronics, and sensitive analog circuits. Their simplicity, low noise, and ability to regulate voltage close to the input level make them indispensable in situations where a stable and clean voltage supply is needed.

2.2 Challenges in LDO design

Designing an efficient LDO regulator comes with several challenges, particularly regarding Power Supply Rejection Ratio (PSRR) as well as noise.

Power Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO can suppress variations (or noise) from the input power supply. High PSRR is crucial for ensuring that fluctuations in the input voltage do not affect the stability of the output voltage. However, achieving high PSRR (especially at high frequencies) can be difficult and often requires careful design of the feedback loop, error amplifier, and pass element.

Noise

Noise generated within the LDO itself can also degrade the performance of sensitive analog or RF circuits. Minimizing output noise while maintaining regulation accuracy and efficiency is a common challenge, particularly in low-power or low-dropout scenarios.

These two factors make LDO design a balancing act between stability, efficiency, noise performance, and the specific needs of the application.

3. LDO PSRR and noise explained

3.1 Understanding PSRR (Power Supply Rejection Ratio)

As previously mentioned, Power Supply Rejection Ratio (PSRR) is a critical metric that gauges how well an LDO can maintain a stable output voltage in the presence of varying input power supply conditions. High PSRR is particularly essential in applications where the input power supply is subject to fluctuations, ensuring the reliability of the supplied voltage. Figure 1 below shows the principle behind measuring PSRR.

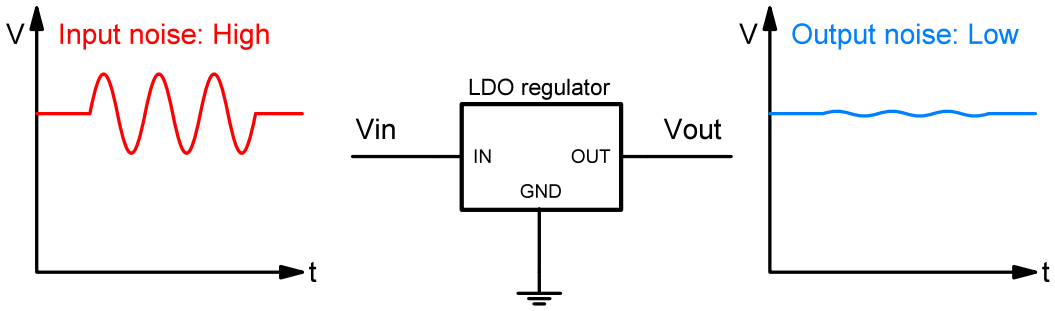

Figure 1: Measuring PSRR

PSRR is calculated using the following equation:

$$PSRR = 20\ log \frac{V_{out}}{V_{in}}$$

where V_{in} and V_{out} are the AC ripple of the input and output voltage, respectively.

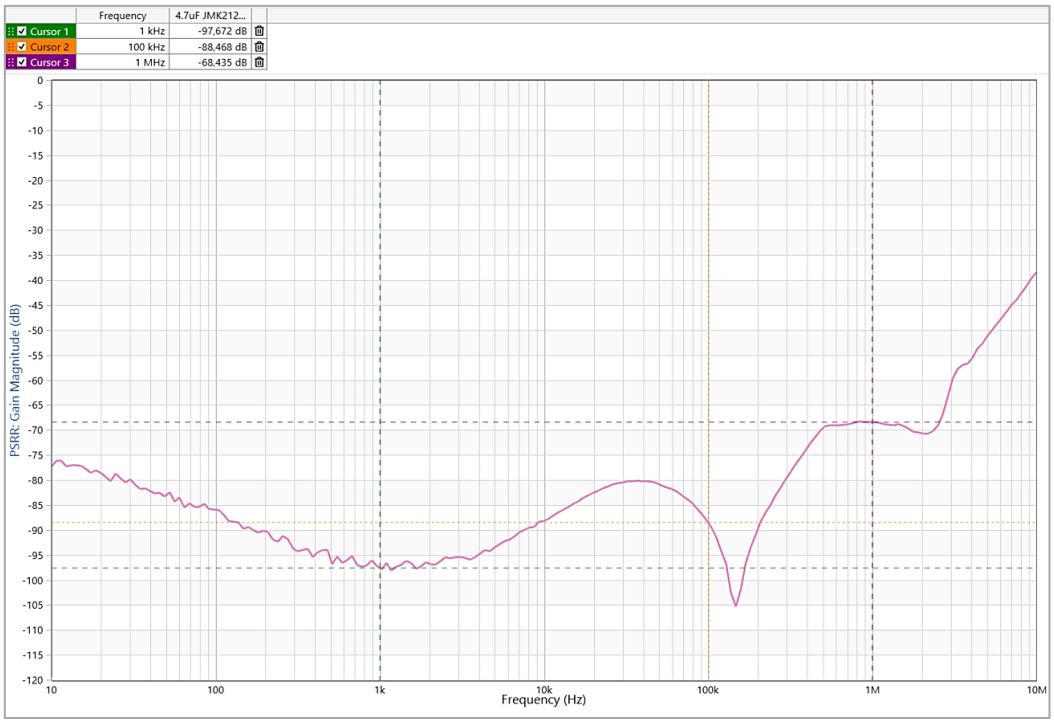

Figure 2: LDO PSRR (dB) vs. Frequency (Hz)

3.2 Factors influencing PSRR

Several factors can influence PSRR, making accurate measurements and considerations vital for effective LDO design:

1. Input frequency range

The PSRR of an LDO typically varies across different frequencies. It tends to be higher at lower frequencies but degrades as frequency increases.

Guidelines for selection:

- Test the LDO over a wide range of frequencies, particularly those relevant to the application, such as power supply switching frequencies, harmonics, and noise sources.
- Ensure that both low and high frequencies are covered. Low frequencies are usually dominated by the LDO's error amplifier, while higher frequencies are typically influenced by parasitic elements and circuit layout.

2. Voltage variation

Variations in input voltage, particularly ripple voltage or noise superimposed on the DC input, are used to assess the PSRR.

Guidelines for voltage variation:

- Use voltage ripple amplitudes representative of real-world operating conditions.
- For LDOs in sensitive applications, small ripple voltages might suffice, while LDOs designed for high-noise environments might need larger ripple voltage to test the upper limits of rejection.

3. Load conditions.

Load conditions can dramatically influence PSRR, as LDOs perform differently under varying current.

Guidelines for load conditions:

- Measure PSRR under different load currents, ranging from low load (10 mA for example) to full load.
- LDOs often show lower PSRR under heavy load conditions due to increased output impedance and limitations of internal regulation.

Effect of load conditions on PSRR:

- At low loads, the error amplifier in the LDO operates with ample bandwidth, resulting in better PSRR performance.
- At higher loads, due to the increased output current affecting the loop stability and bandwidth of the LDO, it may reduce the LDO’s ability to reject input noise, leading to a lower PSRR.
- It is essential to test PSRR across various load conditions to capture a complete picture of an LDO’s performance.

Practical tips for PSRR measurements:

- Use a high-quality power supply and low-noise signal generator to apply the input ripple or noise.
- Ensure that the measurement setup, including cables and connectors, does not introduce additional noise that could affect the accuracy of PSRR readings.
- Consider temperature variations during testing, as thermal effects may alter PSRR performance, especially at higher load currents.

3.3 Noise in LDOs

This section delves into the identification of different noise sources and examines their impact on LDO operation. Understanding the nature of noise is fundamental to implementing strategies to mitigate its effects.

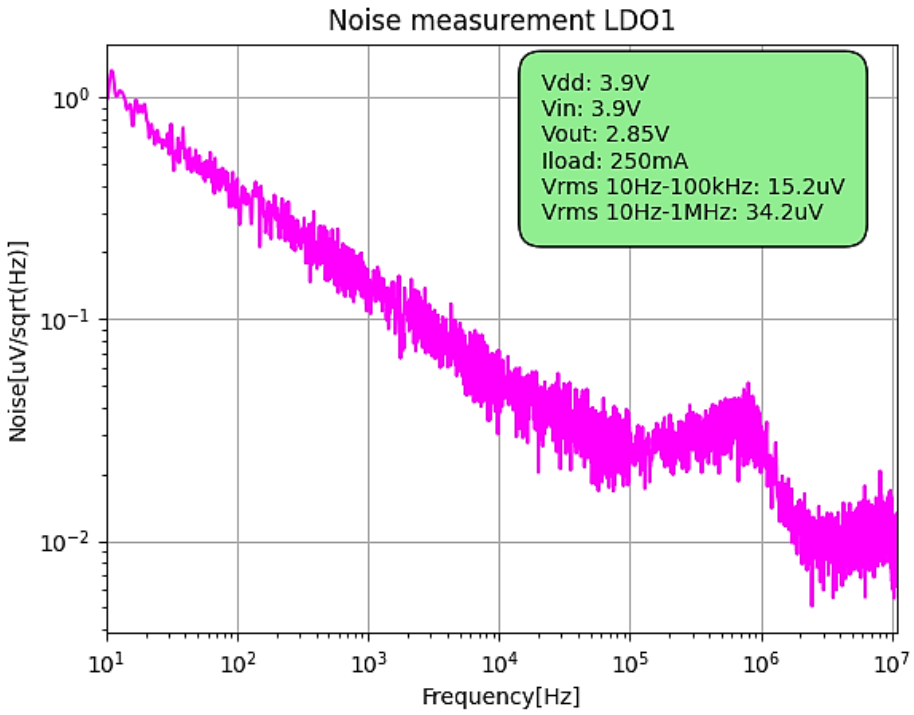

Figure 3: LDO Output Noise (µV/√Hz) vs. Frequency (Hz)

3.3.1. Identification of noise sources and a detailed examination of their impact on LDO operation

Identification of noise sources in LDOs:

- Thermal Noise: Generated by the random motion of charge carriers (usually electrons) within the LDO's semiconductor material. Thermal noise is broadband and exists across the entire frequency range.
- Flicker Noise (1/f Noise): Dominates at low frequencies (below 1 kHz) and is caused by fluctuations in the carrier density and mobility within the semiconductor material.
- Power Supply Ripple: Any AC components present on the input power supply will translate to output noise if the LDO's PSRR is insufficient.
- Load-Induced Noise: Variations in current load can induce noise at the LDO output, especially if the load changes rapidly or drastically.

Impact of noise on LDO Operation:

- Noise present in an LDO can degrade the performance of circuit capabilities, particularly in sensitive applications such as RF communication, analog signal processing, and precision sensors. It can materialize as glitches, jitter, or distortion in these circuits, leading to suboptimal or even faulty performance.

3.3.2. Differentiation between various types of noise and their effects on the output voltage

- Broadband Noise: Covers a wide frequency range and can be a result of thermal noise and other high-frequency interference.
- Low-frequency Noise: Often dominated by flicker noise, this type of noise is particularly problematic for circuits that require stability and precision over long periods.
- High-frequency Noise: Typically stems from external interference or power supply ripple. This noise can be filtered out by choosing appropriate capacitors in the LDO design.

4. Choosing the correct conditions for PSRR measurements

To accurately evaluate the Power Supply Rejection Ratio (PSRR) of Low Dropout Regulators (LDOs), it is crucial to carefully select the measurement conditions. These conditions, such as input frequency range, voltage variations, and load conditions, significantly influence the accuracy and reliability of PSRR measurements. Accurate PSRR measurements are essential for:

- Assessing LDO performance: High PSRR indicates that the LDO is effectively attenuating input noise, resulting in a cleaner, more stable output.
- Design optimization: PSRR data helps designers choose the right LDO for applications where power integrity is critical, such as in noise-sensitive analog circuits or RF systems.
- System reliability: Understanding the LDO's PSRR behavior ensures reliable performance, especially under varying operating conditions.

In real-world scenarios, electronic systems often operate in dynamic environments where the power supply conditions can vary. Accurate PSRR measurements enable engineers to assess how well an LDO can handle these variations, ensuring the stability and reliability of the entire system.

5. Requirements for using capacitors with low parasitic parameters

Capacitors are fundamental components in electronics, playing a critical role in stabilizing circuits and filtering noise. When choosing capacitors, low parasitic parameters such as Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR) are essential for high-performance applications, including Low Dropout Regulators (LDOs). This chapter focuses on capacitors with low ESL and ESR, explaining their significance, selection criteria, and practical considerations for implementation.

5.1 Low ESL capacitors

5.1.1. Significance of low Equivalent Series Inductance (ESL)

ESL corresponds to the inductive behavior of a capacitor, which can degrade performance in high-frequency applications. Capacitors with low ESL provide enhanced noise filtering and stability, especially in circuits such as LDOs where noise rejection is critical. It reduces the phase shift in the feedback loop and suppresses high-frequency noise leading to improved stability and performance. It also prevents oscillations and maintains smooth voltage regulation under varying load conditions, which is vital for sensitive electronics.

5.1.2. Criteria for selecting capacitors with low ESL

Low ESL capacitors minimize the formation of resonances within the circuit, which can lead to spikes in voltage noise. By reducing the capacitor inductance, high-frequency noise is filtered out. Additionally, low ESL capacitors stabilize the feedback loop in LDOs, improving phase margin and ensuring reliable operation across a wide range of loads. Capacitors with low ESL are generally characterized by their construction and material composition. Ceramic capacitors, particularly Multilayer Ceramic Capacitors (MLCCs), commonly have low ESL properties. During capacitor selection, the following criteria should be considered:

- Type: MLCCs typically offer the lowest ESL.
- Capacitance value: Higher capacitance values in small package sizes often indicate lower ESL.
- Package size: Shorter lead lengths of smaller packages (e.g., 0402, 0603) tend to have lower inductance.
- Mounting technology: Surface-mount capacitors have lower inductance compared to through-hole types.
- X5R or X7R dielectric types of capacitors are suitable for higher capacitance applications.

Guidelines for selection should focus on balancing capacitance, voltage rating, and ESL to match the specific frequency and stability requirements of the circuit.

5.1.3. Practical considerations for implementation

- PCB Placement: Capacitors with low ESL should be placed as close as possible to the load components or power input to minimize the inductive path. This also helps to achieve better noise filtering and stability.
- Proximity to Load: The closer the capacitor is to the load, the more effective it will be in reducing noise and stabilizing the voltage.
- Manufacturer Guidelines: Always adhere to the manufacturer's recommendations regarding placement, handling, and operating conditions to ensure optimal performance.
- Via Design: If vias are required for connection, minimizing their number and ensuring proper design can help maintain low inductance.

5.2 Low ESR capacitors

5.2.1. Significance of low Equivalent Series Resistance (ESR)

Equivalent Series Resistance (ESR) is the resistive element within a capacitor that causes power dissipation. Low ESR is critical in power-sensitive applications, such as LDOs, as it minimizes energy loss and improves efficiency. Capacitors with low ESR are more effective at stabilizing the output voltage and reducing ripple, especially under dynamic load conditions. They also enhance the transient response, allowing the regulator to quickly compensate for sudden changes in load demand.

5.2.2. Criteria for selecting capacitors with low ESR

When selecting capacitors with low ESR, the following factors should be considered:

- Capacitor type: ceramic capacitors, especially MLCCs, are known for their inherently low ESR, making them ideal for high-frequency and low-noise applications. Tantalum and polymer capacitors also offer low ESR, particularly at higher capacitance values.
- Temperature stability: capacitors with stable ESR over a wide temperature range are preferable for applications that experience fluctuating operating temperatures.
- Frequency range: the ESR of a capacitor can vary with frequency. Choosing a capacitor that maintains low ESR across the required frequency spectrum is crucial for consistent performance.

6. Practical application and case studies in real-life capacitor usage with high performance SLG51003 Power GreenPAK IC

6.1 Measuring the impact of various capacitors on PSRR performance

In practical applications, the Power Supply Rejection Ratio (PSRR) is a key parameter to analyse the performance of capacitors in conjunction with high-performance PMICs. The effectiveness of using specific capacitors to achieve high PSRR performance are shown the following Tables and Figures using real experimental measurements with the High Performance LDO of SLG51003 Power GreenPAK IC.

Table 1: List of capacitors used for measurement comparison

Capacitance [µF]	Manufacturer Product Number	Voltage [V]	Package	Features
2.2	LMK212B7225MGHT	10V	0805	Ultra Low ESR
2.2	GRM216R61A225KE24D	10V	0805	General Purpose
2.2	GRM21BR71E225KE11	25V	0805	General Purpose
4.7	JMK212ABJ475MGHT	6.3V	0805	Ultra Low ESR
4.7	GRM21BR71C475KE51L	16V	0805	General Purpose
4.7	C2012X5R1C475M060AC	16V	0805	Low ESL
10	LMK212AC6106MD-T	10V	0805	Ultra Low ESR
10	GRM21BR71A106KA73K	10V	0805	General Purpose
10	C2012X5R1C106K085AC	16V	0805	Low ESL

Table 2: Test instruments and equipment

Equipment	Manufacturer	Model	Quantity
Power Supply	Rohde-Schwarz	HMP4040	1
Source Meter	Keithley	2460/2461	1
Digital Multimeter	Keysight	34465A	1
Oscilloscope	Pico Technology	Pico Scope 5444D MSO	1
Network Analyzer	Omicron Lab	Bode 100	1
Line Injector	Omicron Lab	Picotest J2120A	1
HF Cable(coaxial)	Amphenol RF	Cable Assembly Coaxial BNC to SMB RG-174 12.00" (304.80mm)	2
HF Cable(coaxial)	-	Cable Assembly Coaxial BNC to BNC	1

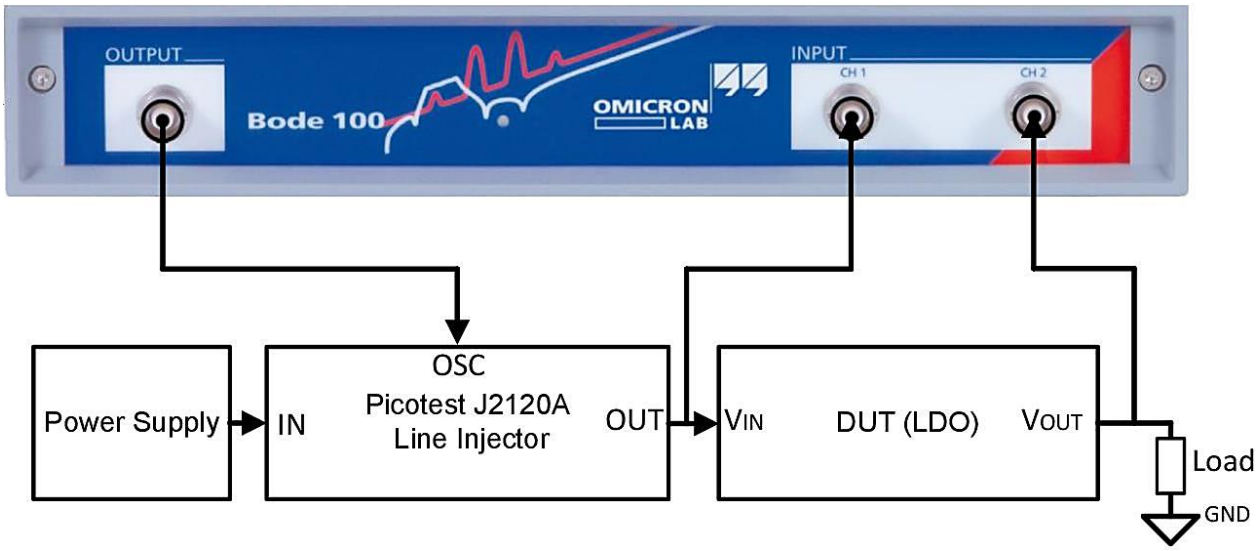

Figure 4: PSRR measurement bench setup diagram

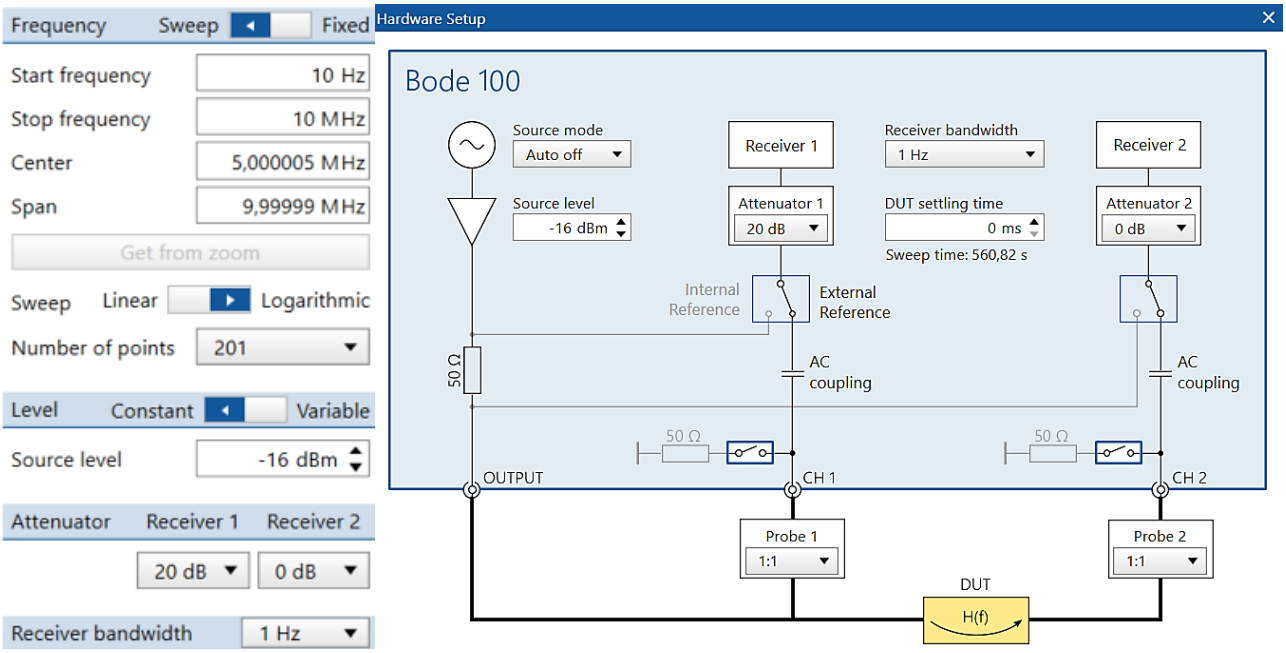

Figure 5: Bode analyzer suite configuration

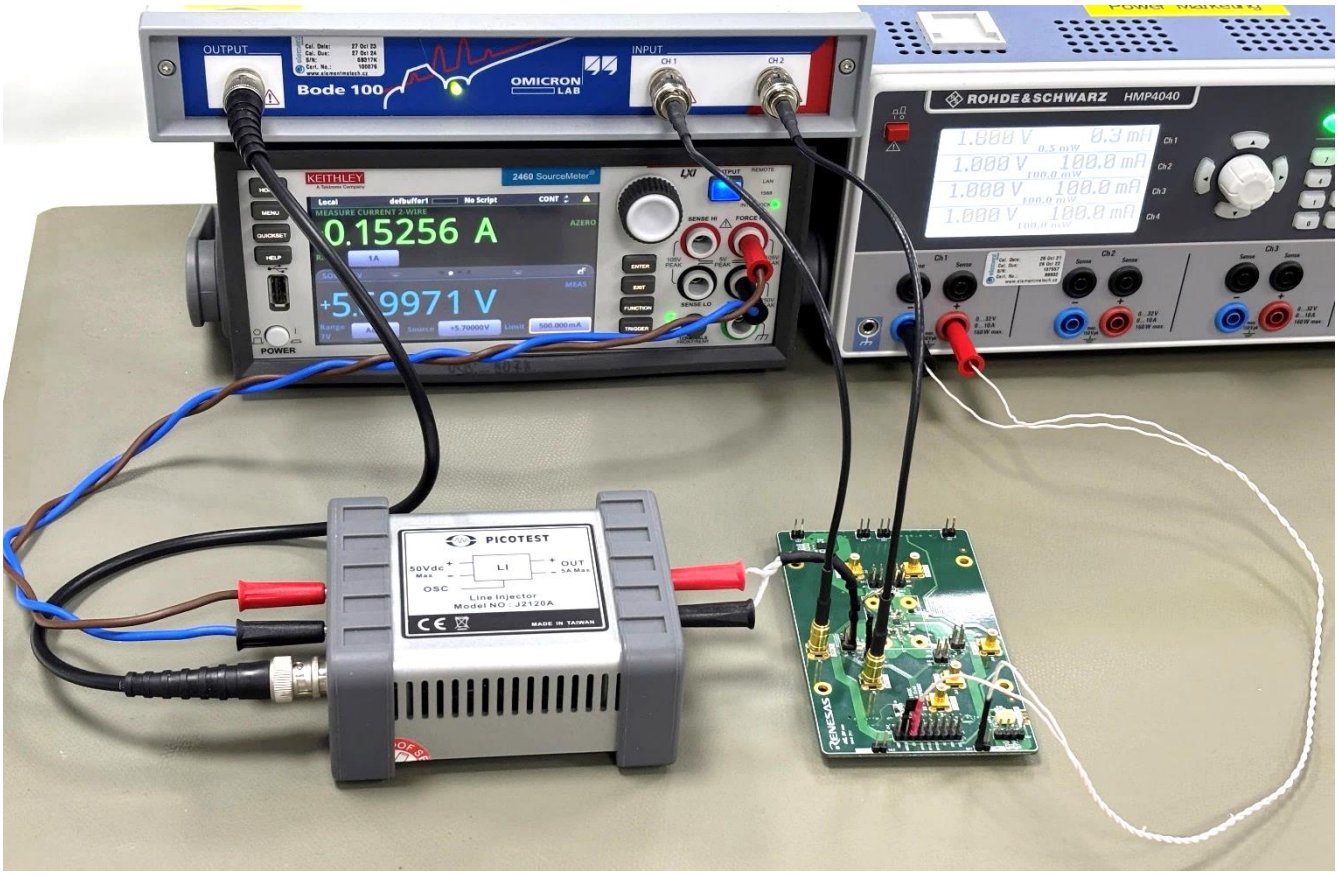

Figure 6: General setup including the SLG51003 Power GreenPAK IC

The PSRR results are shown in Figure 7 and Table 3.

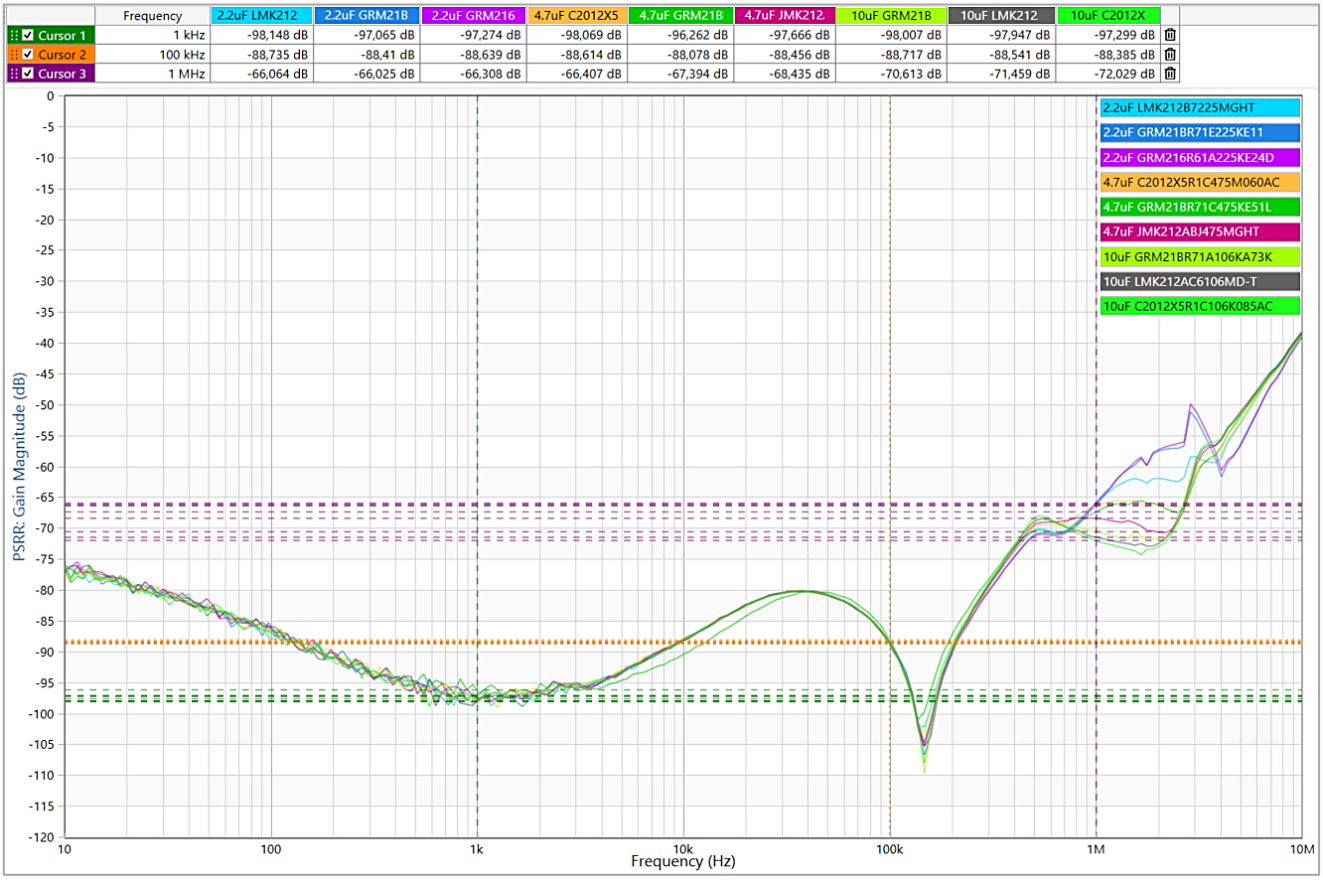

Figure 7: SLG51003 PSRR plot with selected capacitors for bench measurements

Table 3: SLG51003 PSRR bench measurements results with selected capacitors

Conditions					Results			Unit
C_{OUT} [µF]	I_{LOAD} [mA]	V_{DD} [V]	V_{IN} [V]	V_{OUT} [V]	1 kHz	100 kHz	1 MHz	
2.2 LMK212B7225MGHT	150	3.2	3.2	2.85	-98.148	-88.735	-66.064	dB
2.2 GRM216R61A225KE24D					-97.065	-88.41	-66.025	dB
2.2 GRM21BR71E225KE11					-97.274	-88.639	-66.308	dB
4.7 JMK212ABJ475MGHT					-98.069	-88.614	-66.407	dB
4.7 GRM21BR71C475KE51L					-96.262	-88.078	-67.394	dB
4.7 C2012X5R1C475M060AC					-97.666	-88.456	-68.435	dB
10 LMK212AC6106MD-T					-98.007	-88.717	-70.613	dB
10GRM21BR71A106KA73K					-97.947	-88.541	-71.459	dB
10 C2012X5R1C106K085AC					-97.299	-88.385	-72.029	dB

Analyzing data obtained in Table 3 indicates that the HP LDO of the SLG51003 retains a lower PSRR value with lower capacitance but still maintaining relevant performance. The higher capacitance provides significant performance improvement for PSRR results in the High Frequency range. Considerable impact on measurement results may affect effective capacitance after derating.

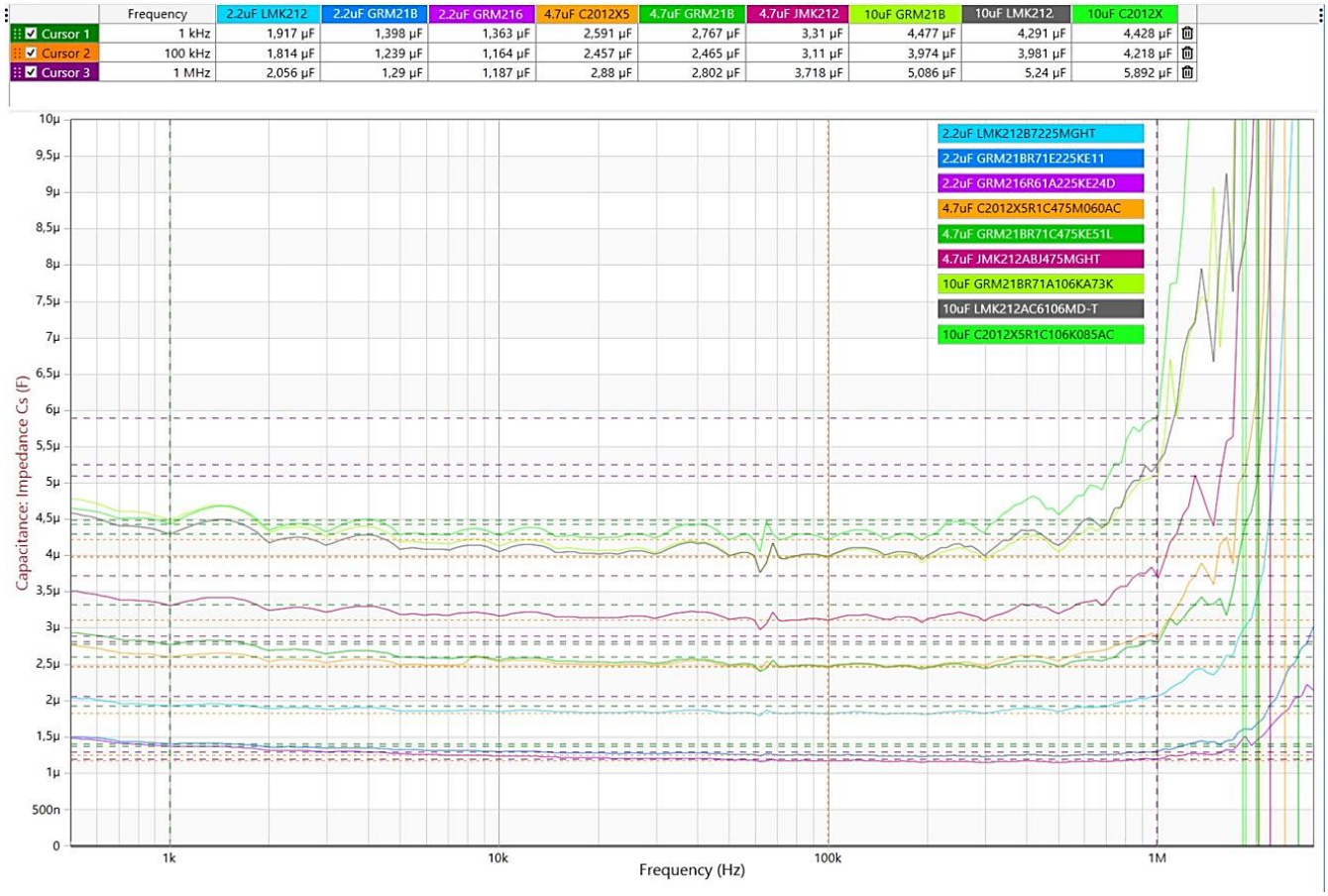

Figure 8: Derated measured capacitance with 2.85 V DC voltage offset

Figure 8 shows the real measured capacitance with a 2.85 V DC voltage offset applied. As can be seen, the real value is much lower than specified. Therefore, it is customary to use the concept of effective capacitance.

6.2 Constant output load variations and PSRR value

Another factor that impacts on the PSRR performance is the value of the output load. Even if using a lower current in some cases can improve the PSRR performance, this value cannot be considered, given that most LDOs have been optimized to work within the typical recommendations of the output load.

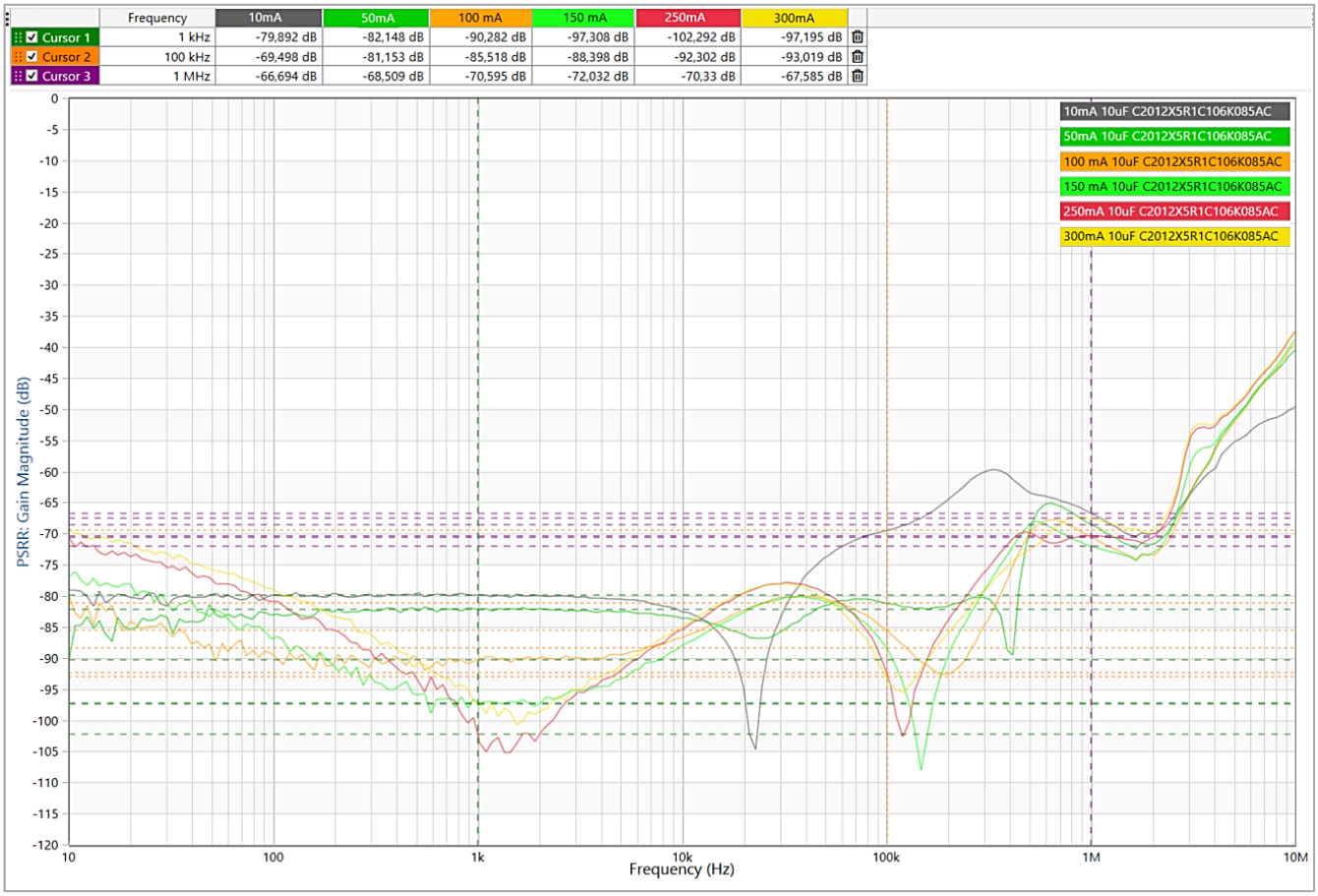

Figure 9: PSRR plot constant load dependance on HP LDO with a 10µF C2012X5R1C106K085AC output capacitor

Table 4: SLG51003 PSRR bench measurement results with a 10 µF C2012X5R1C106K085AC capacitor and different output loads

Conditions					Results			Unit
C_{OUT} [µF]	I_{LOAD} [mA]	V_{DD} [V]	V_{IN} [V]	V_{OUT} [V]	1 kHz	100 kHz	1 MHz	
10 C2012X5R1C106K085AC	10	3.2	3.2	2.85	-79.892	-69.5	-66.69	dB
	50				-82.147	-81.152	-68.504	dB
	100				-90.286	-85.511	-70.591	dB
	150				-97.299	-88.385	-72.029	dB
	250				-102.26	-92.278	-70.33	dB
	300				-97.193	-93.005	-67.584	dB

Analyzing Table 4, SLG51003 shows better optimization for a higher output load. This provides a significant benefit for powering in a system that requires high performance with high output current on the LDO and at the same time have acceptable high performance for lower load.

7. Conclusion

In applications which require a high performance LDO to supply power, the output capacitor used can degrade or significantly improve the performance. The SLG51003V multi-output, multiple LDO PMIC offers high PSRR (98.5 dB at 1 kHz and 68 dB at 1 MHz for LDO_HP) and Low Noise (16 µV LDO_HP) which are guaranteed when operating within datasheet conditions.

The provided measurement data covers cases outside of datasheet specifications where the SLG51003V demonstrates high performance when operating under low capacitance and offers significant improvements with higher capacitance after derating.

The SLG51003's main application is as an Advanced Sensor Power Supply. It enhances system performance, improves image quality, and ensures that final products stand out in competitive markets where reliability and precision are critical. In addition, it provides all of the Power GreenPAK additional benefits, such as high configurability, statuses and reports, programmable scenarios and sequencing, GPIOs, and I^2C interface support.

8. Revision History

Revision	Date	Description
1.00	Oct 17, 2024	Initial version