

How to measure PSRR for SLG5100X PMICs

This document describes how to measure the LDOs Power Supply Rejection Ratio (PSRR) for SLG51000X Power GreenPAK PMICs in the 10 Hz to 10 MHz frequency range using bench equipment.

Contents

Terms and Definitions	1
References.....	2
1. Introduction.....	2
2. What is PSRR?.....	2
3. Equipment and Setup.....	3
4. Settings for PSRR Bench Measurements Setup	5
5. Conclusions	12
6. Revision History	13

Figures

Figure 1: Measurement Principle.....	3
Figure 2: J2120A Resistance and Voltage Drop Versus Output Current	4
Figure 3: PSRR Bench Measurement Block Diagram.....	5
Figure 4: Start Menu	6
Figure 5: Setting Trace 1	6
Figure 6: Hardware Setup in Gain/Phase Measurement Mode and Measurement Configuration.....	7
Figure 7: "Full Range Calibration" Button.....	7
Figure 8: Full Range Calibration Window	8
Figure 9: Calibration Setup	8
Figure 10: Performed Calibration Window.....	9
Figure 11: Simplified Example That Shows Headroom Impact on the Ripple Magnitude.....	10
Figure 12: Example of Applied Ripple and Its Magnitude with DC Offset for LDO's Input.....	10
Figure 13: Working with Cursors	11
Figure 14: Example of Captured PSRR Graph for SLG51003 LDO.....	11
Figure 15: SLG51003 PSRR Bench Measurement Setup	12

Terms and Definitions

PSRR	Power Supply Rejection Ratio
PMIC	Power Management Integrated Circuit
LDO	Low Dropout Output

References

- [1] [SLG51000 Datasheet \(renesas.com\)](#), Revision 3.11, Renesas Electronics.
- [2] [SLG51001 Datasheet \(renesas.com\)](#), Revision 3.01, Renesas Electronics.
- [3] [SLG51002 Datasheet \(renesas.com\)](#), Revision 3.11, Renesas Electronics.
- [4] [SLG51003 Datasheet \(renesas.com\)](#), Revision 1.00, Renesas Electronics.
- [5] [AN-CM-399 Enhancing LDO PSRR and Noise Performance Measurements Using Capacitors with Low Parasitic Parameters](#), Application Note, Renesas Electronics.
- [6] [Go Configure™ Software Hub | Renesas](#)

Author: Oleh Yakymchuk, Applications Engineer, Renesas Electronics

Originally published at <https://www.edn.com/how-to-measure-psrr-of-pmics/>

1. Introduction

This manual provides comprehensive guidelines on measuring the Power Supply Rejection Ratio (PSRR) for the SLG5100X Power GreenPAK PMICs. PSRR is a critical parameter that indicates how well a circuit can reject variations in its power supply voltage, thereby ensuring stable performance. Understanding and accurately measuring PSRR helps in designing robust and reliable electronics that perform consistently under varying power conditions.

2. What is PSRR?

The Power Supply Rejection Ratio (PSRR) is a vital parameter that assesses an LDO's capability to maintain a consistent output voltage amidst variations in the input power supply. Achieving high PSRR is crucial in scenarios in which the input power supply experiences fluctuations, thereby ensuring the dependability of the output voltage. [Figure 1](#) below illustrates the general methodology for measuring PSRR.

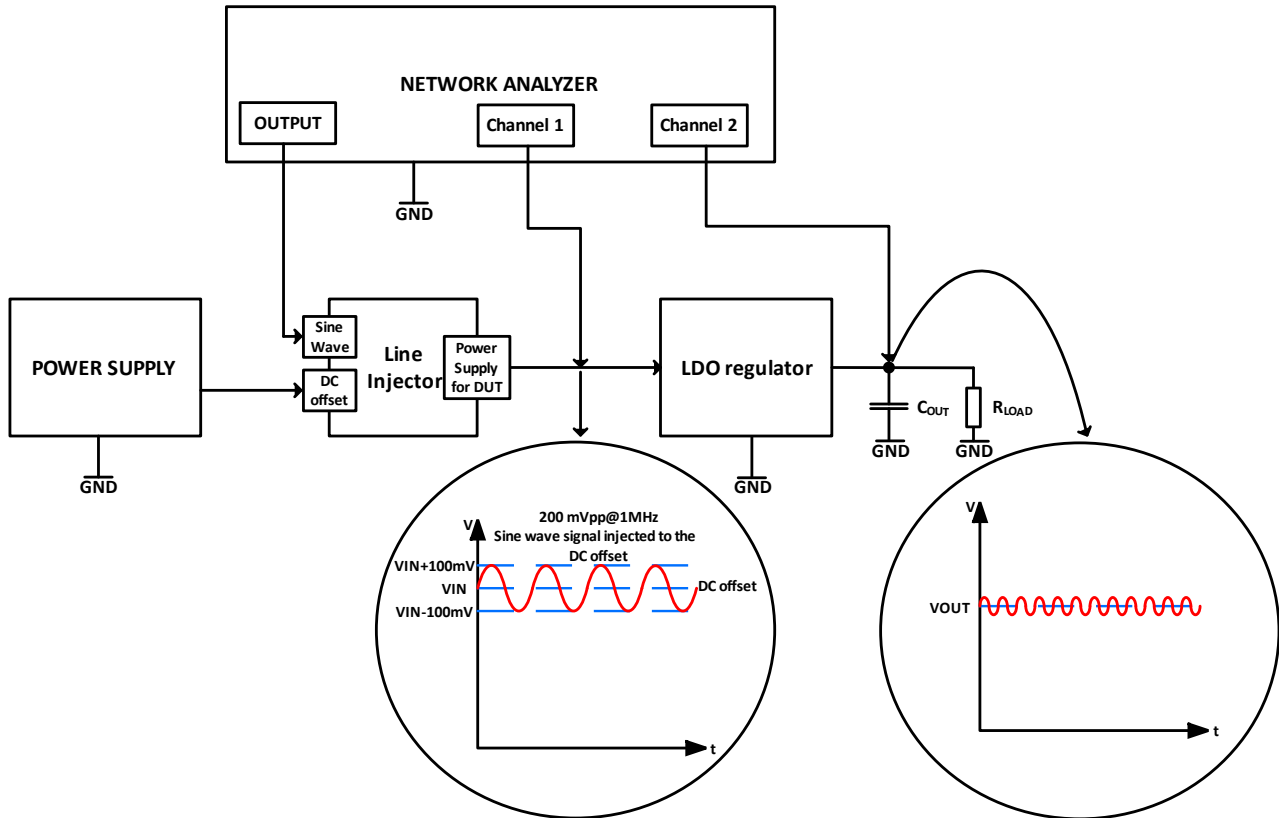


Figure 1: Measurement Principle

The mathematical expression to calculate the PSRR value is:

$$PSRR = 20 \log_{10} \frac{V_{IN}}{V_{OUT}}$$

where V_{IN} and V_{OUT} are the AC ripple of the input and output voltage, respectively.

3. Equipment and Setup

To ensure an accurate measurement of the PSRR, it is essential to set up the test environment with precision. The following design outlines the use of the listed equipment to establish a robust and reliable test configuration.

First, connect the power supply, in our case it is a Keithley 2460, to the input of the Picotest J2120A Line Injector. The power supply should be configured to generate a stable DC voltage while the AC ripple component (to simulate power supply variations) is provided by a Bode 100 network analyzer output using the J2120A line injector [Note 1].

Next, a Digital Multimeter is used to monitor both the input and output voltages of the PMIC. Ensure that proper grounding is used, and minimal interference is present in the connections to maintain measurement integrity.

Finally, a Bode 100 from Omicron Lab is used to record and analyze the measurements. This data can be used to compute the PSRR values and evaluate the PMIC's ability to maintain a stable output despite variations in the input supply.

By carefully following this setup, one can ensure accurate and reliable PSRR measurements, contributing to the development of high-performance and dependable electronic systems.

How to measure PSRR for SLG5100X PMICs

Note 1: The J2120A line injector includes an internally biased N-Channel MOSFET. This means that there is a voltage drop between the J2120A input and output. The voltage drop is non-linear and its dependency is shown on Figure 2. This means that each time the load current is adjusted the source power supply must also be adjusted to maintain a constant DC output voltage at the J2120A terminals. For example, to get 1.2 V at the input of the LDO regulator, and depending on the load current, it might be required to set the voltage on the input of the Line Injector from 2.5 V to 3.5 V. The MOSFET operates open loop so as not to become unstable when connected to the external regulator.

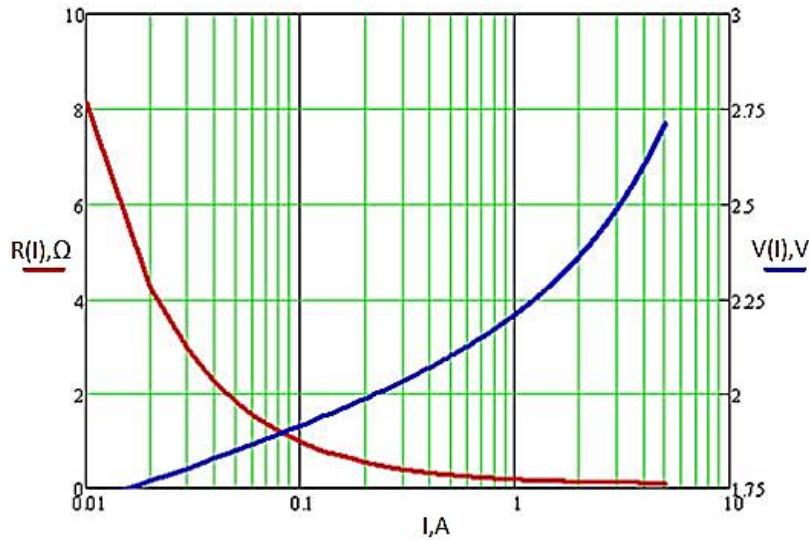


Figure 2: J2120A Resistance and Voltage Drop Versus Output Current

Table 1: Instruments

Equipment	Manufacturer	Model	Quantity
Power Supply	Rohde-Schwarz	HMP4040	1
Source Meter	Keithley	2460	1
Digital Multimeter	Keysight	34465A	1
Oscilloscope	Siglent	SDS1104X-E	1
Network Analyzer	Omicron Lab	Bode 100	1
Line Injector	Omicron Lab	Picotest J2120A	1

Table 2: LDOs Test Conditions

LDO type	Conditions				
	C _{OUT} [μF]	I _{LOAD} [mA]	V _{DD} [V]	V _{IN} [V]	V _{OUT} [V]
HP_LDO (SLG51000: LDO1, LDO2; SLG51001: LDO1; SLG51003: LDO1)	4.7	150	3.2	3.2	2.85
HV_LDO (SLG51000: LDO3, LDO4, LDO7; SLG51001: LDO2 - LDO5; SLG51002: LDO1 - LDO3; SLG51003: LDO2)	4.7	250	3.8	3.8	3.3
HC_LDO (SLG51002: LDO4, LDO5)	4.7	250	3.8	3.8	3.3
LV_LDO (SLG51000: LDO5, LDO6;	22	400 for SLG51000,	3.8	1.475	1.175

LDO type	Conditions				
	C _{OUT} [μF]	I _{LOAD} [mA]	V _{DD} [V]	V _{IN} [V]	V _{OUT} [V]
SLG51001: LDO6; SLG51002: LDO6 - LDO8; SLG51003: LDO3)		500 for SLG51001- SLG51003			

4. Settings for PSRR Bench Measurements Setup

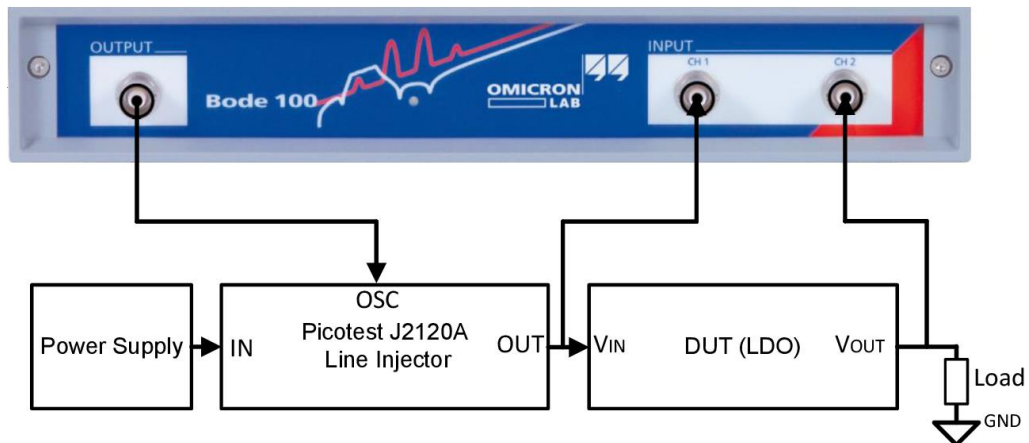


Figure 3: PSRR Bench Measurement Block Diagram

The PSRR measurement is performed with the Bode 100. The Gain/Phase measurement type should be chosen in the Bode Analyzer Suite software as shown on [Figure 4](#).

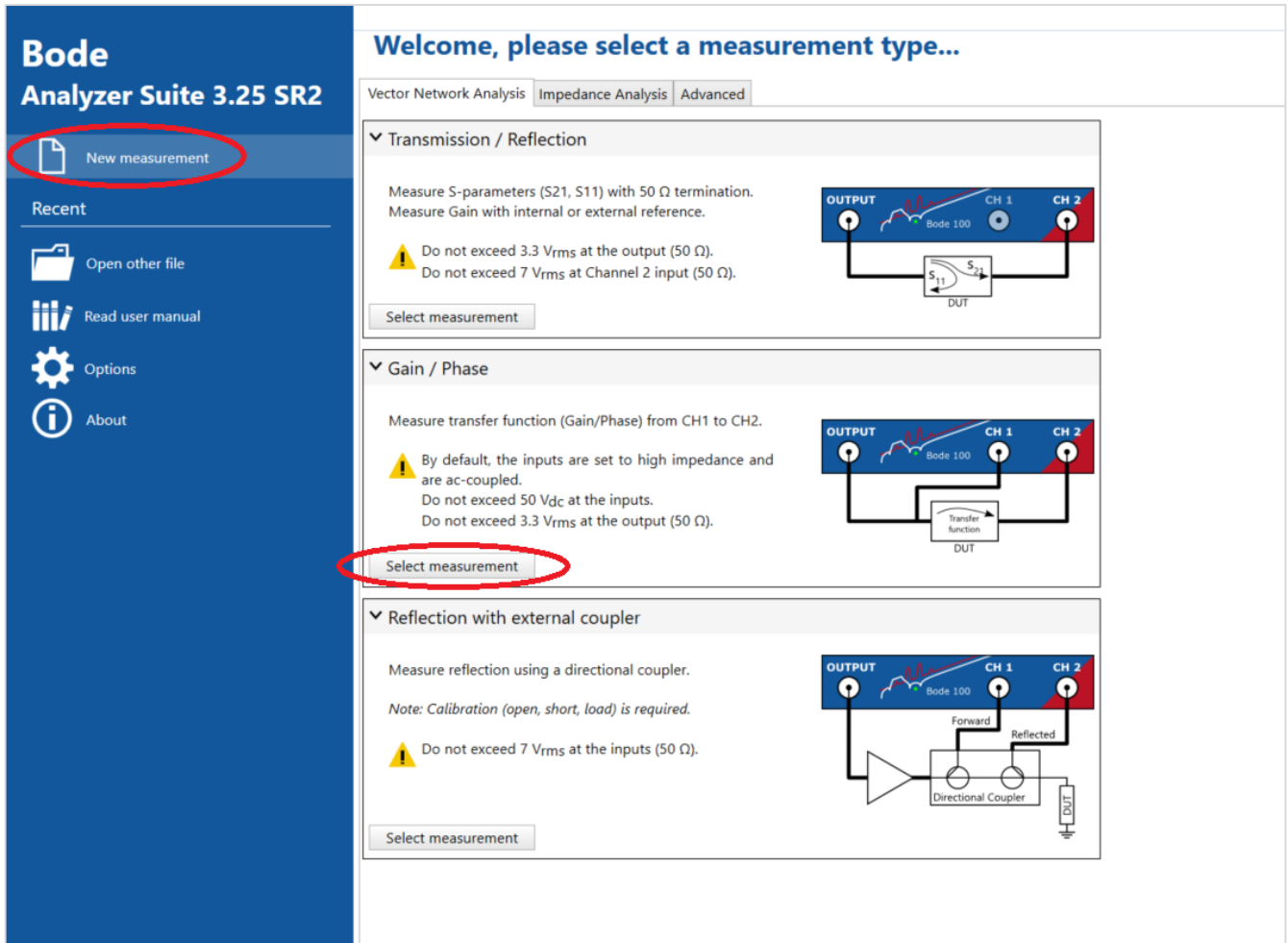


Figure 4: Start Menu

Set the Trace 1 format to Magnitude (dB).

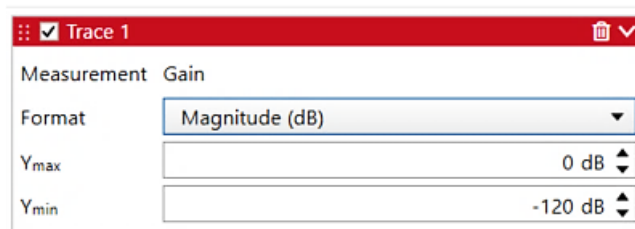


Figure 5: Setting Trace 1

To get the target PSRR measurement, choose the following settings in the "Hardware Setup":

1. **Frequency:** change the Start frequency to "10 Hz" and Stop frequency to "10 MHz".
2. **Source mode:** Choose between Auto off or Always on. In Auto off mode, the source will be automatically turned off whenever it is not used (when a measurement is stopped). In Always on mode the signal source stays on after the measurement has finished. This means that the last frequency point in a sweep measurement defines the signal source frequency and level.
3. **Source level:** Set the constant source level to "-16 dB" or higher for the output level. The unit can be changed in the options . By default, the Bode 100 uses dBm as the output level unit. 1 dBm equals 1 mW at 50 Ω load. "Vpp" can be chosen to display the output voltage in peak-to-peak voltage. Please note that the

How to measure PSRR for SLG5100X PMICs

internal source voltage is 2 times higher than the displayed value and valid when a 50 Ω load is connected to the output.

4. **Attenuator:** Set the input attenuators 20 dB for Receiver 1 (Channel 1) and 0 dB for Receiver 2 (Channel 2).
5. **Receiver bandwidth:** Select the receiver bandwidth used for the measurement. Higher receiver bandwidth increases the measurement speed. Reduce the receiver bandwidth to reduce noise and to catch narrow-band resonances.

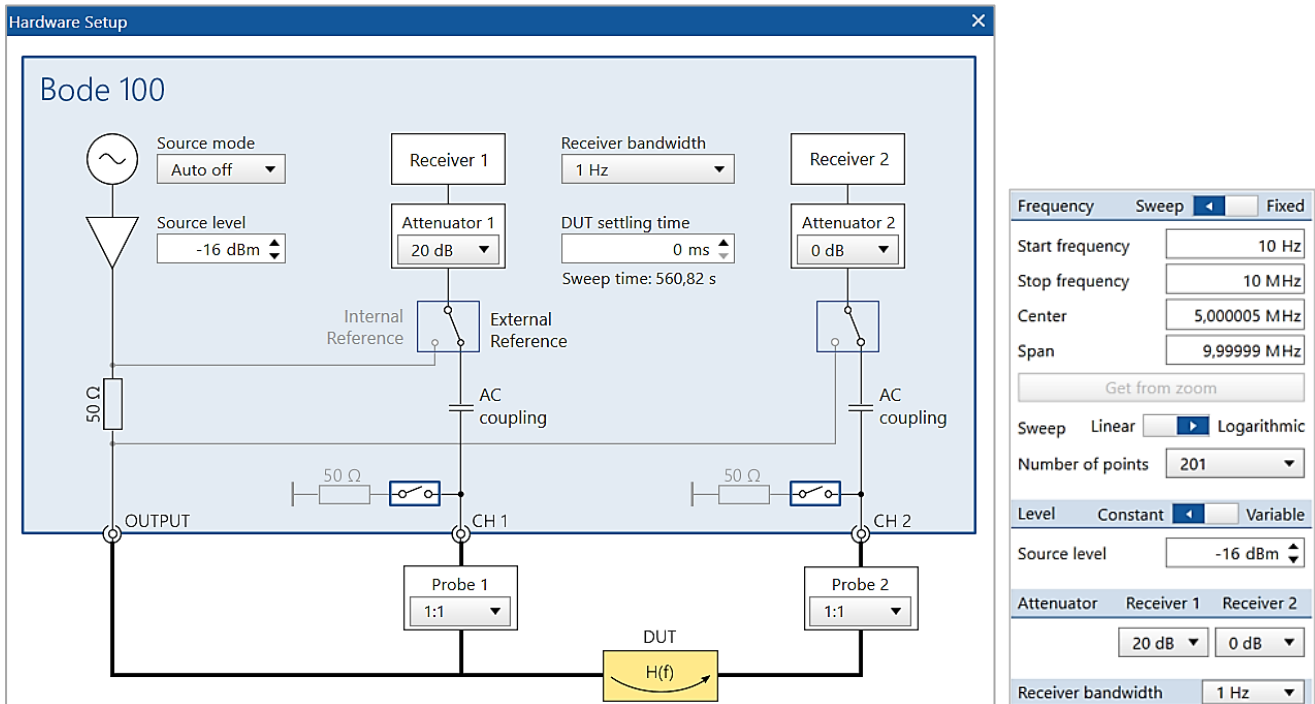


Figure 6: Hardware Setup in Gain/Phase Measurement Mode and Measurement Configuration

Before starting the measurement, the Bode 100 needs to be calibrated. This will ensure the accuracy of the measurements. Press the "Full Range calibration" button as shown on Figure 7. To achieve maximum accuracy, do not change the attenuators after external calibration is performed.

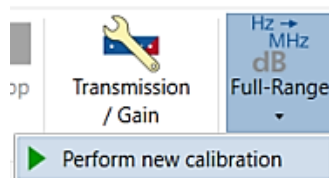


Figure 7: "Full Range Calibration" Button

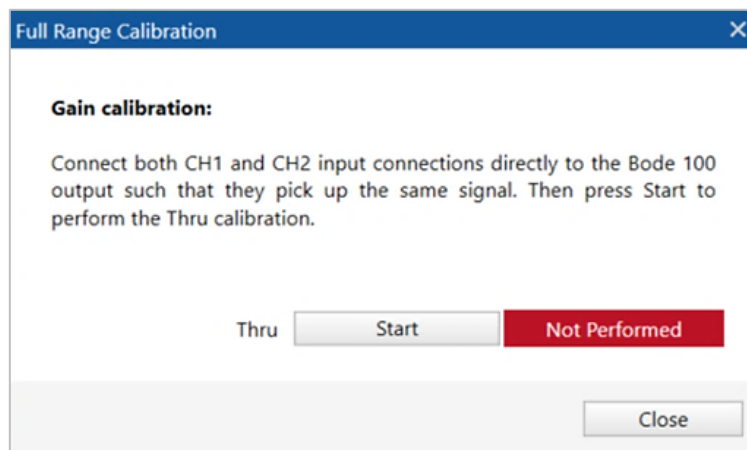


Figure 8: Full Range Calibration Window

Connect OUTPUT, CH1, and CH2 as shown below and perform the calibration by pressing the Start button.

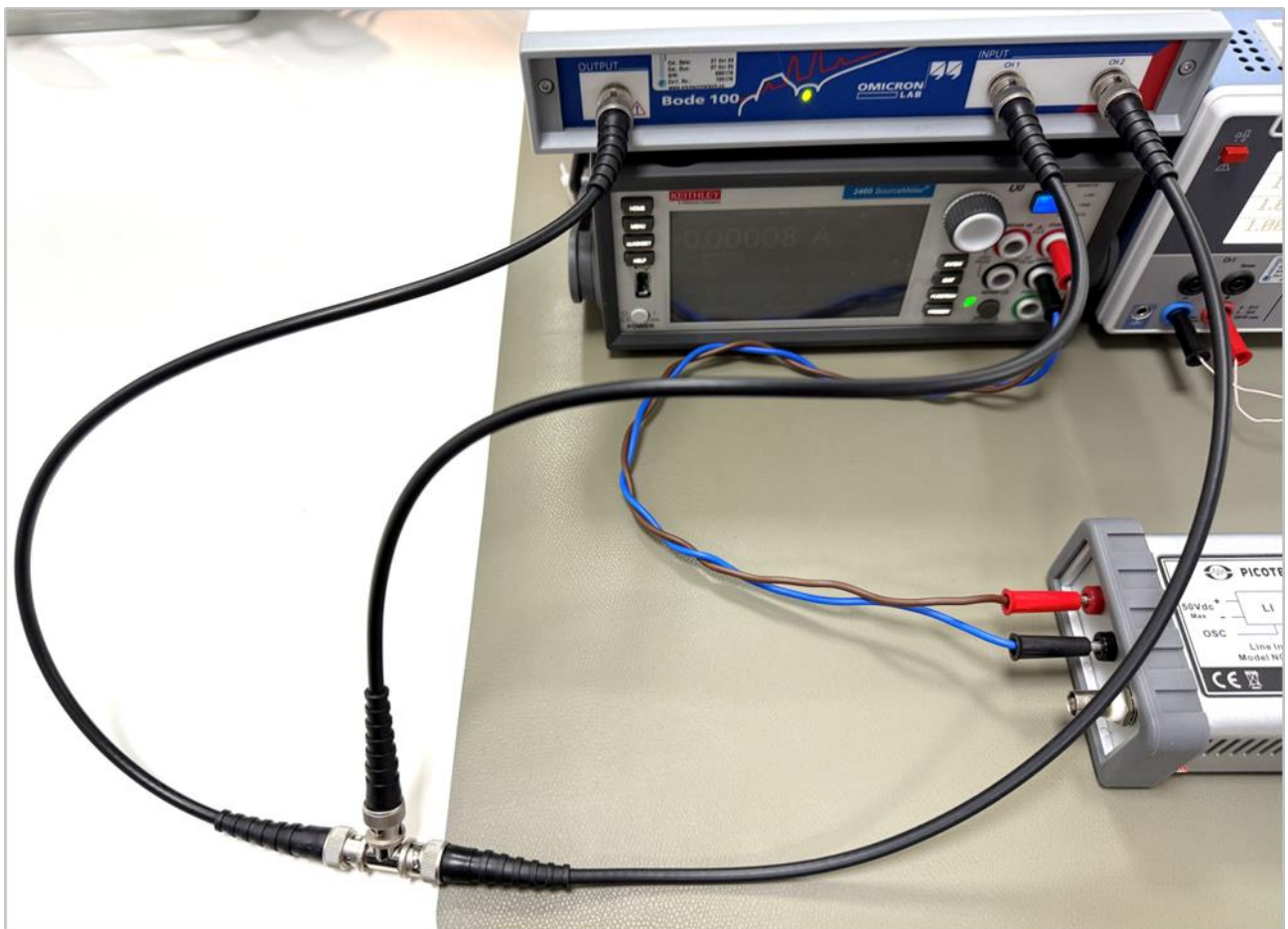


Figure 9: Calibration Setup

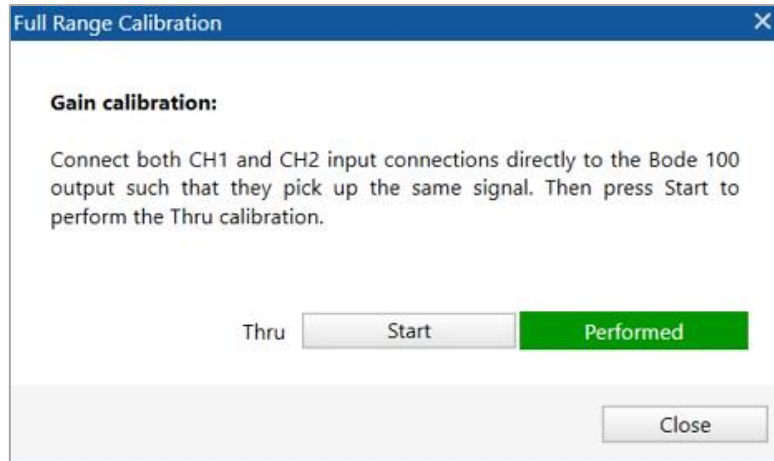


Figure 10: Performed Calibration Window

For all LDOs:

1. The input capacitor will filter out some of the signals injected into the LDO, so it is best to remove the input capacitors for the tested LDO or keep one as small as possible.
2. Configure the network analyzer: use the power supply to power the line injector and connect the output of the network analyzer to the OSC input of the line injector.
3. Power up the device under test (DUT) and configure the tested LDO's output voltage.
To prevent damage to the PMIC, the LDO's input voltage should be less than or equal than the max input voltage. It is highly recommended to power up the LDO without a resistive load, then apply the load and adjust the input voltage. Keep in mind the previous [Note 1](#) regarding line injector behavior vs. load.
4. Configure the LDO VOUT as specified in [Table 2](#).
5. Enable the LDO under test and use a voltmeter to check the output voltage.
6. To ensure that the start-up current limit does not prevent the LDO from starting correctly, connect the resistive load to the LDO once the VOUT voltage has reached its max level.
7. Adjust the voltage at the J2120A OUT terminals to their target VIN voltages.
8. Connect the first channel (CH1) of the network analyzer to the input of the LDO under test using a short coaxial cable.
9. Connect the second channel (CH2) of the network analyzer to the output of the LDO under test using a short coaxial cable.
10. Monitor the output voltage of the line injector on an oscilloscope. Perform a frequency sweep and check that the minimum input voltage and an appropriate peak to peak level for test are achieved. Make sure that the AC component is 200 mVpp or lower.

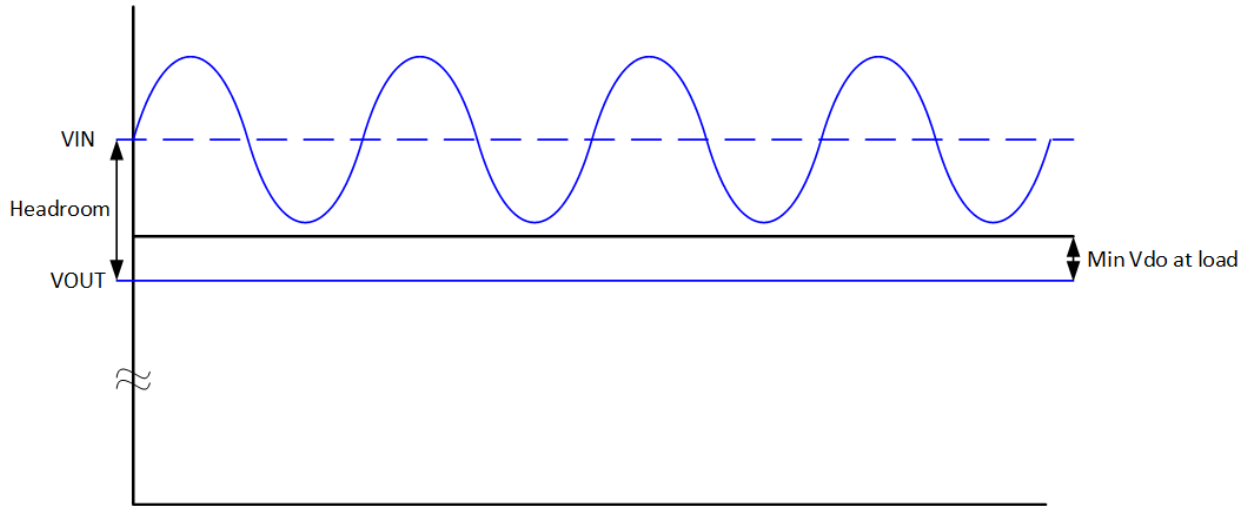


Figure 11: Simplified Example That Shows Headroom Impact on the Ripple Magnitude

Note 2: The headroom for the PSRR is not the same as the dropout voltage parameter (Vdo) specified in the datasheets (see Figure 11). Headroom in the context of PSRR refers to the additional voltage margin above the output voltage that an LDO requires to effectively reject variations in the input voltage. Essentially, it ensures that the LDO can maintain a stable output despite fluctuations in the input power supply. Dropout voltage (Vdo), on the other hand, is a specific parameter defined in the datasheets of LDOs. It is the minimum difference between the input voltage (VIN) and the output voltage (VOU) at which the LDO can still regulate the output voltage correctly under static DC conditions. When the input voltage drops below this minimum threshold, the LDO can no longer maintain the specified output voltage, leading to potential performance issues.

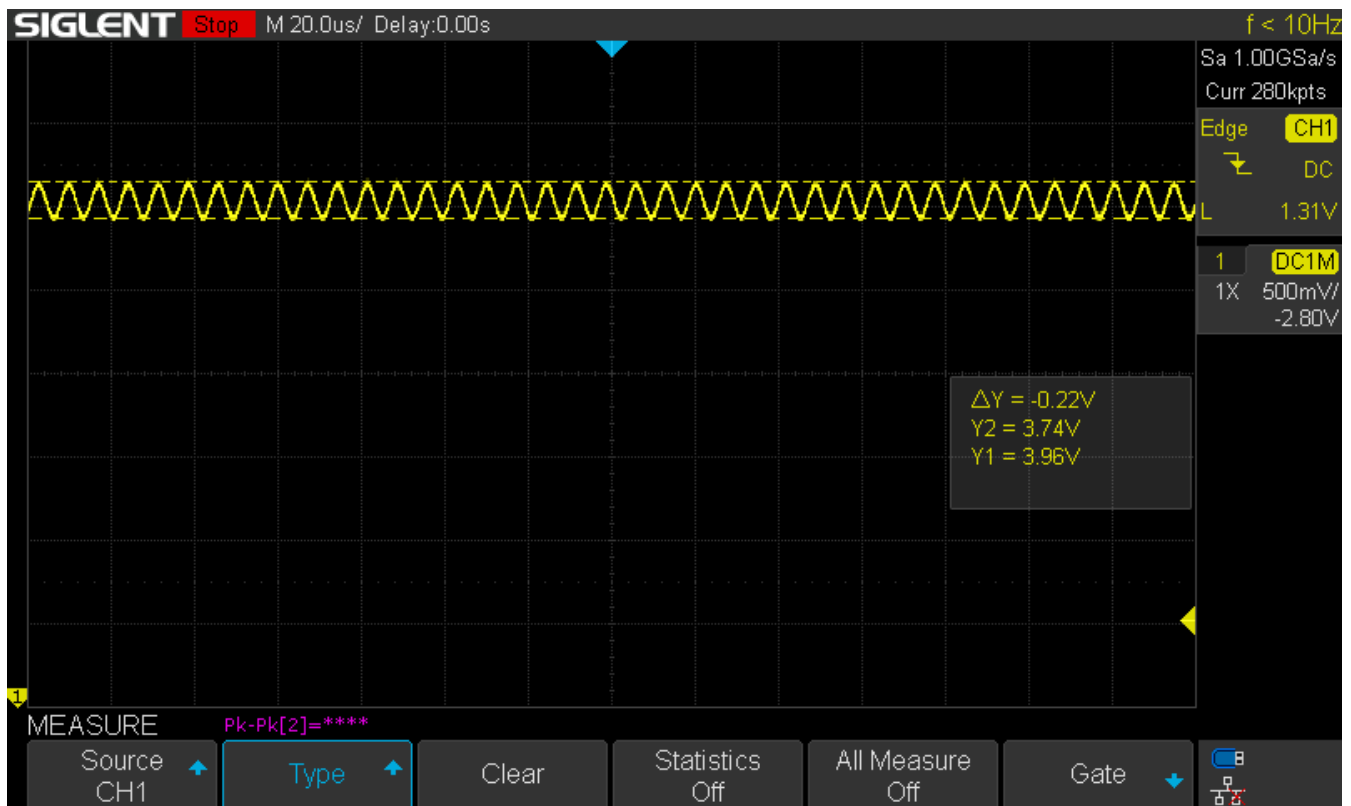


Figure 12: Example of Applied Ripple and Its Magnitude with DC Offset for LDO's Input

11. Set up the network analyzer by using cursors to measure the PSRR at each required frequency (1 kHz, 100 kHz and 1 MHz). Add more cursors if needed to measure peaks as shown on Figure 13.

How to measure PSRR for SLG5100X PMICs

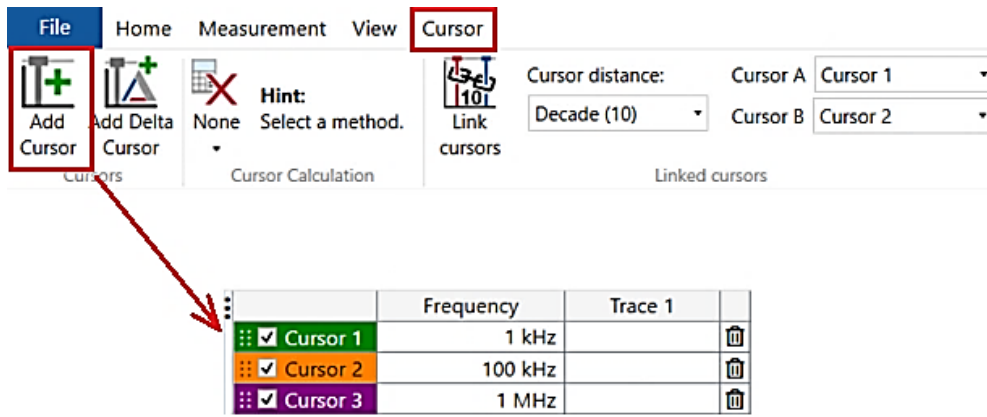


Figure 13: Working with Cursors

12. Capture images for each measured condition.

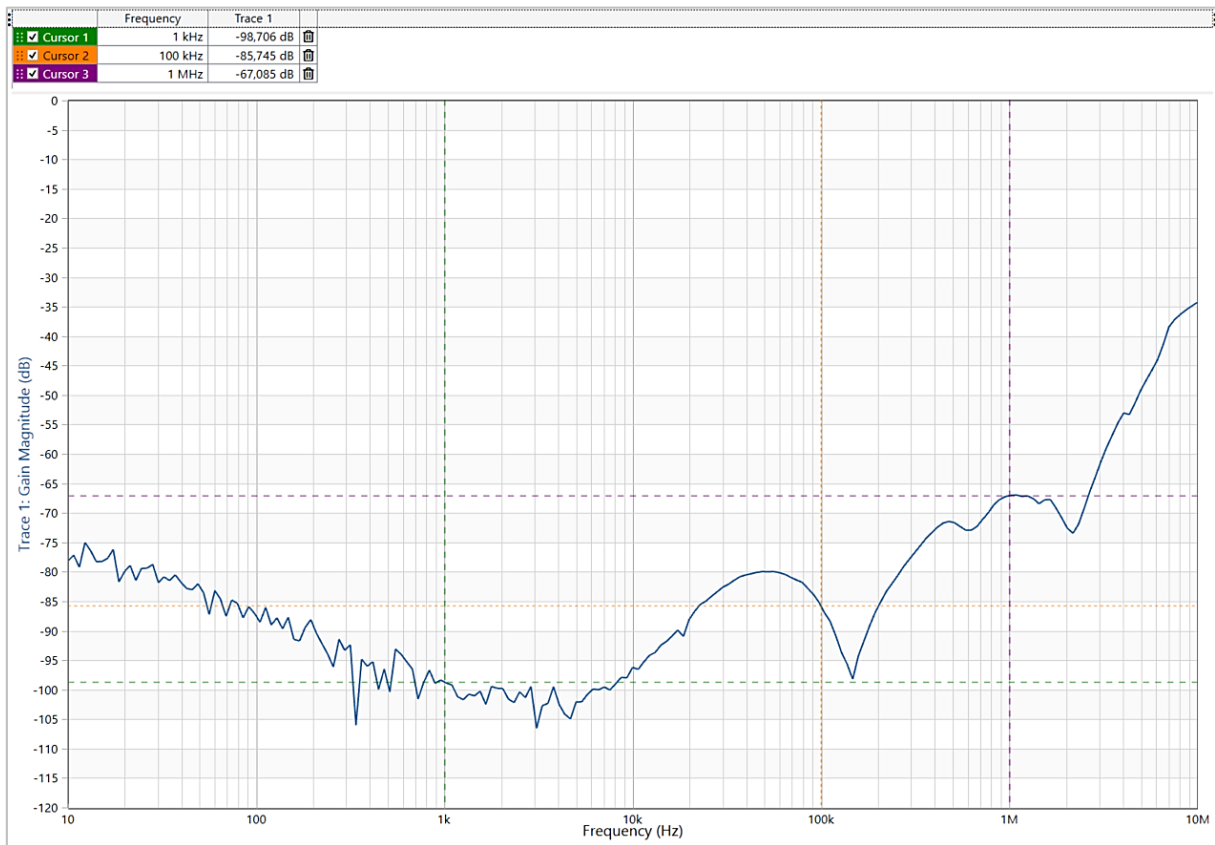


Figure 14: Example of Captured PSRR Graph for SLG51003 LDO

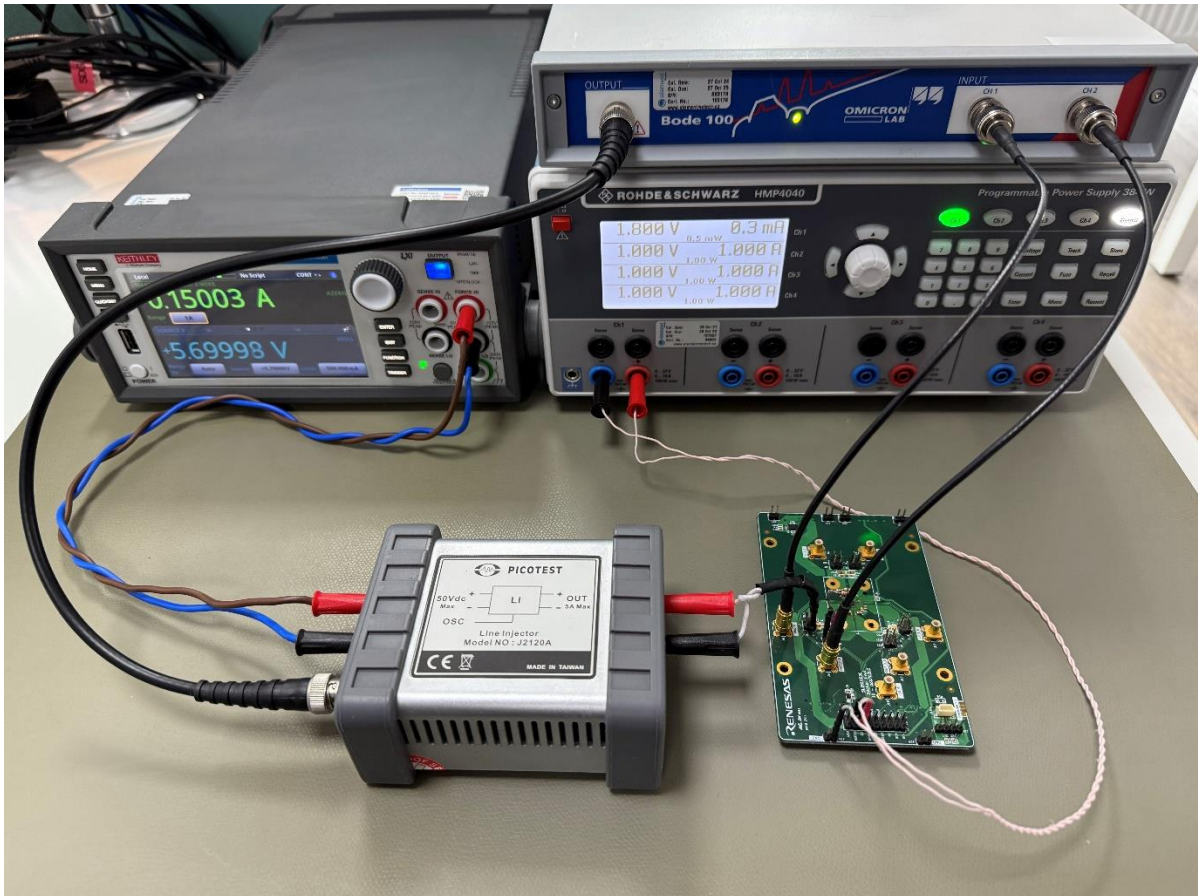


Figure 15: SLG51003 PSRR Bench Measurement Setup

5. Conclusions

The methodology detailed in this document outlines the process for measuring the Power Supply Rejection Ratio for SLG5100X PMICs using an Omicron Lab Bode 100 and a Picotest J2120A. Accurate measurement of PSRR in the 10 Hz to 10 MHz frequency range is essential for ensuring LDO performance.

The figures represent a valuable reference for setting up and interpreting measurements. Adhering to these guidelines ensures reliable PSRR measurements, contributing to the quality of power management systems

6. Revision History

Revision	Date	Description
1.00	March 28, 20245	Initial release.