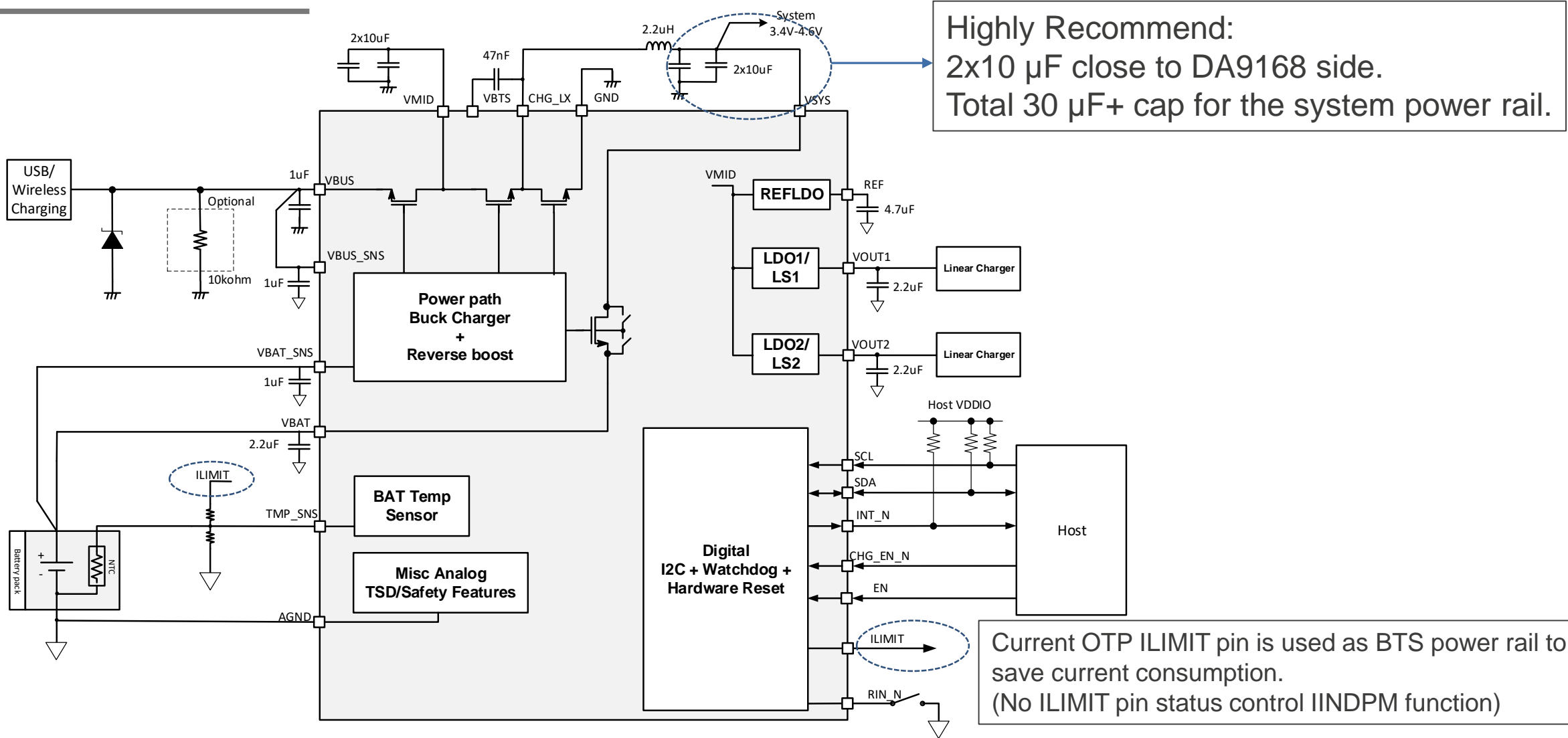


DA9168BC APPLICATION NOTE

FEB 2022

RENESAS ELECTRONICS CORPORATION

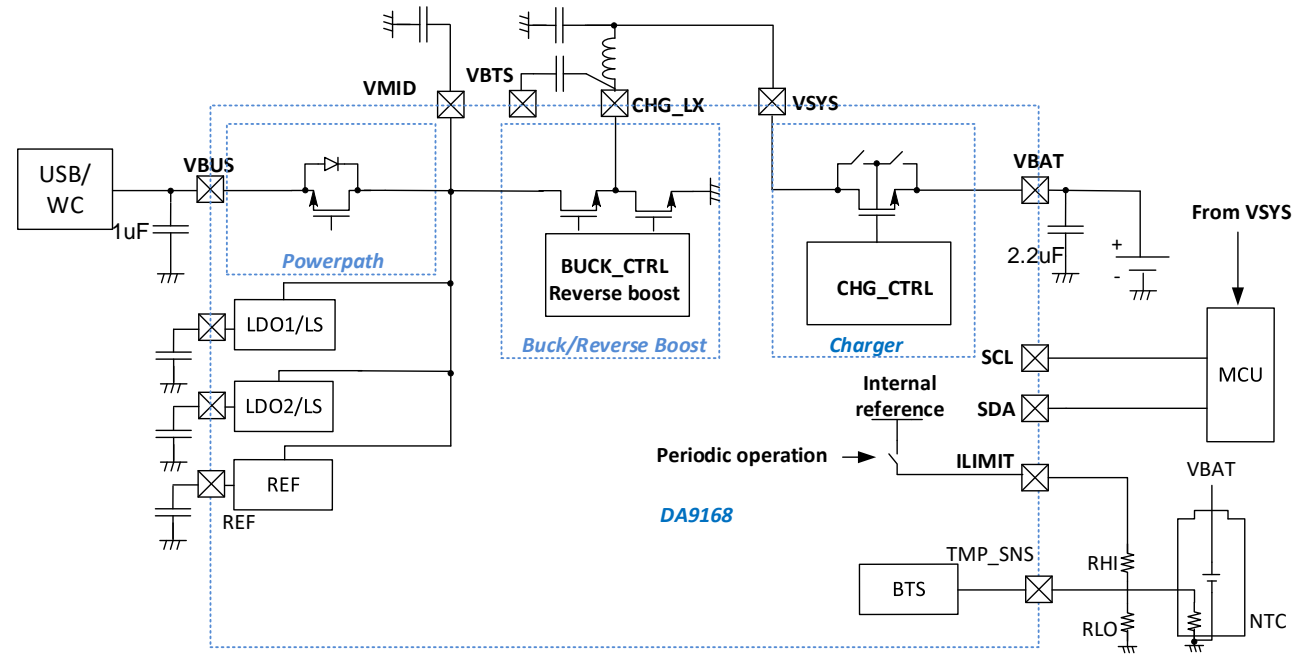
TYPICAL TWS APPLICATION WITH CURRENT OTP



DA9168 BTS WITH ILIMIT PIN

BTS WITH ILIMIT - VBUS IQ

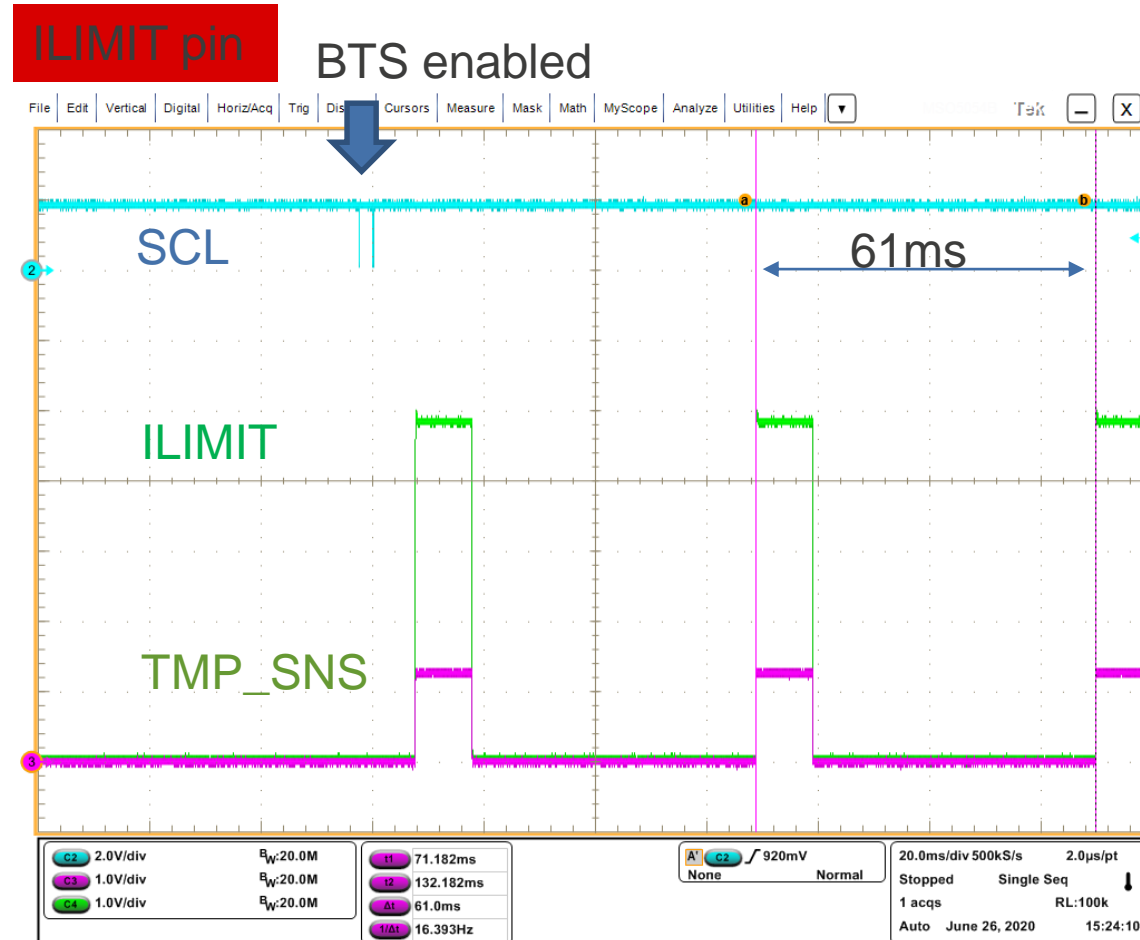
Using ILIMIT pin (instead of REF) for BTS has large I_Q savings



BTS Reference	BTS	Condition	I_Q from VBAT (μA)	Savings (μA)
REF	Disabled	Reverse boost + REFLDO	377	-
REF	Enabled	Reverse boost + REFLDO + BTS (50msec)	380	-
REF	Enabled	Reverse boost + REFLDO + BTS (2 sec)	377	-
ILIMIT	Disabled	Standby (boost disable)	10	I_Q increase from BTS just $\sim 1 \mu\text{A}$
ILIMIT	Enabled	Standby (boost disable) + BTS (50 msec)	41	
ILIMIT	Enabled	Standby (boost disable) + BTS (2 sec)	11	

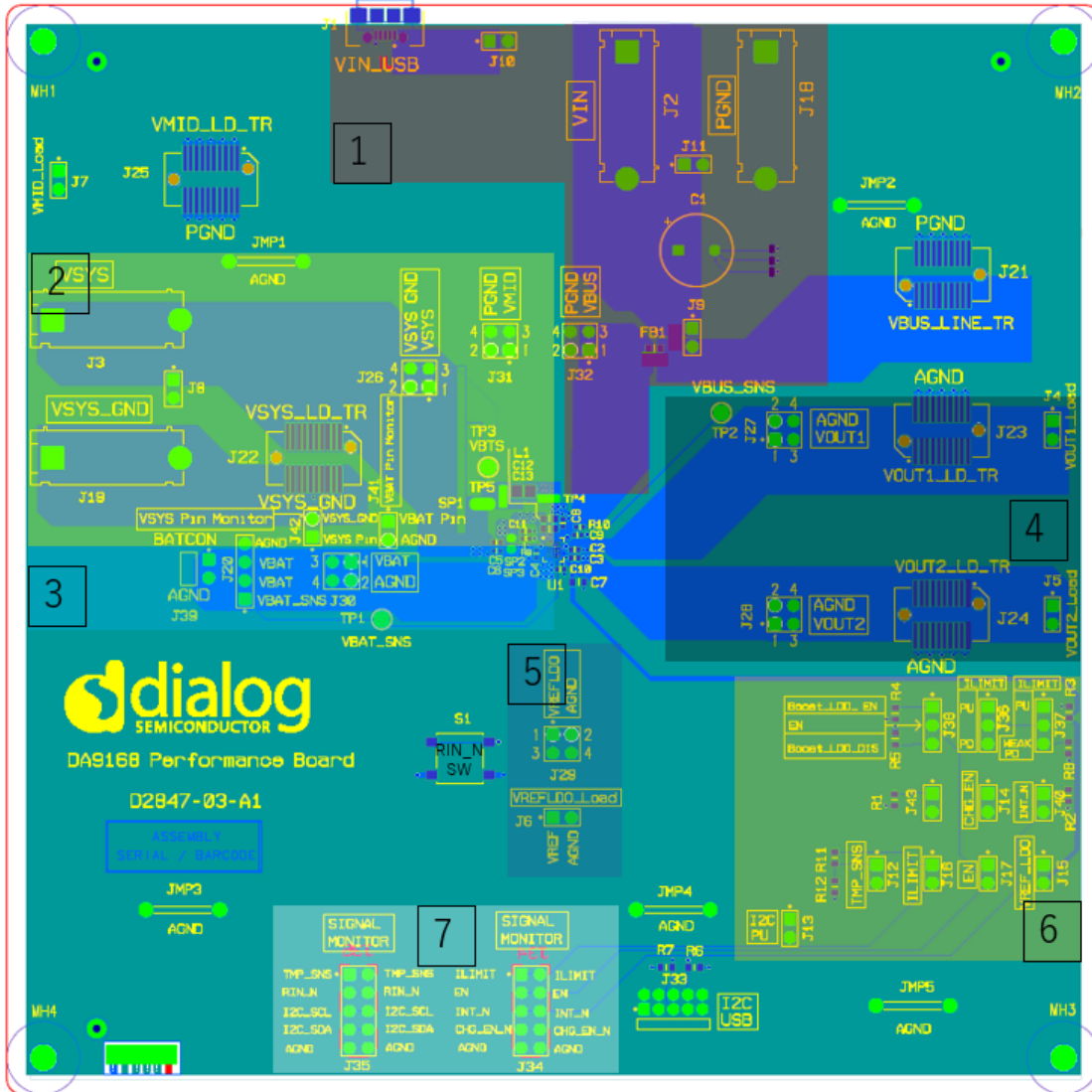
BTS WITH ILIMIT - PERIODIC OPERATION

- ✓ BTS periodic operation working as expected



DA9168 PERFORMANCE BOARD

PERFORMANCE BOARD OVERVIEW

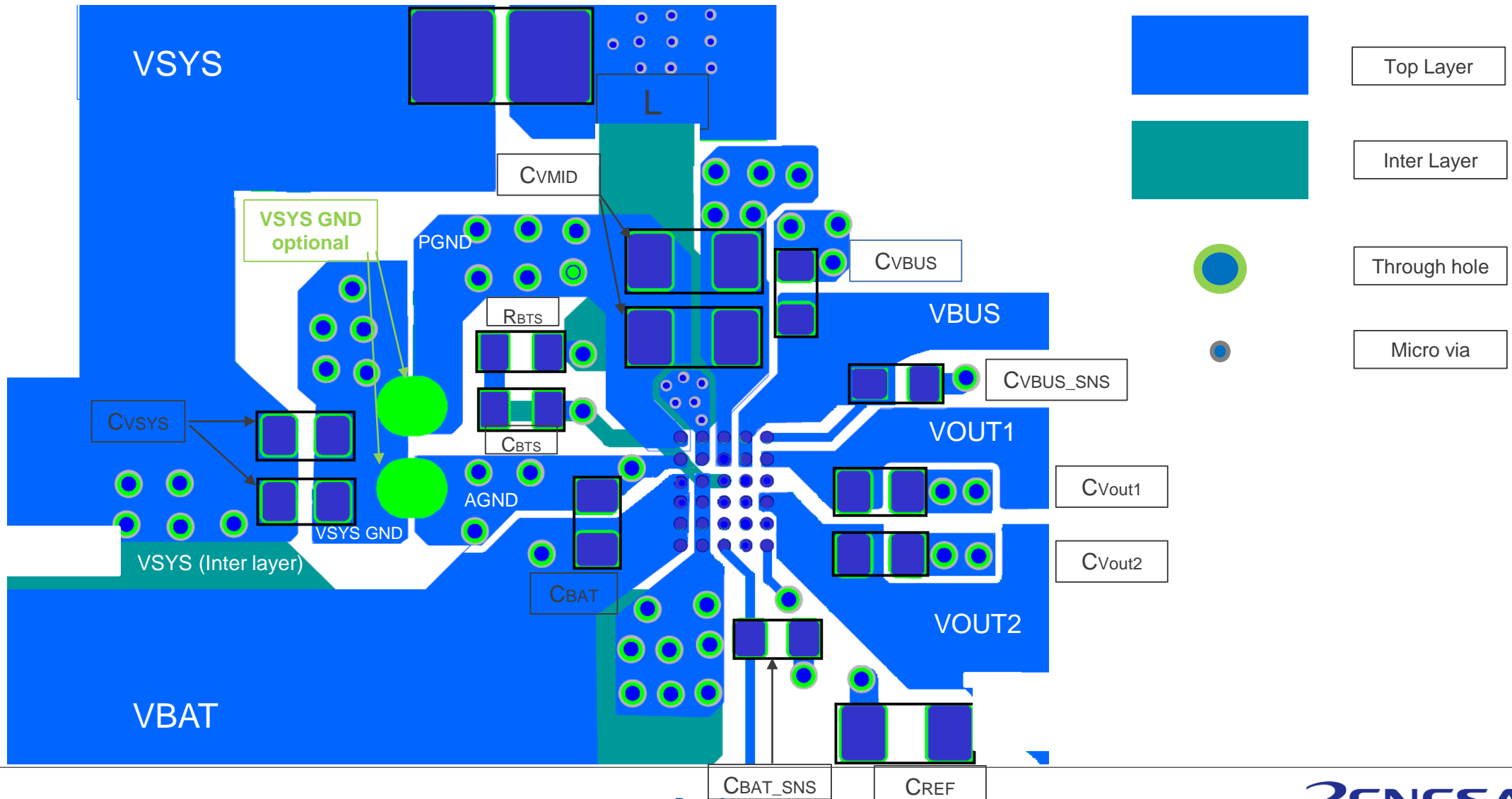


CAUTION

Apply high current to J26, J27, J28, J29, J30, J31, J32, J41 and J42 headers pin 1 and 2 may causes the voltage sensing traces burn out.

1. VBUS input section: Power supply and USB power supply connectors.
2. VSYS output section.
3. VBAT input/output section.
4. VOUT1 and VOUT2 outputs section.
5. REFLDO output section.
6. GPIOs network section.
7. GPIOs signal monitors section.

DA9168 PERFORMANCE BOARD LAYOUT CONCEPT



LAYOUT GUIDELINES

1. Minimize high frequency current path loop (VMID – CHG_LX – VSYS – GND and CHG_LX – VSYS - GND) to reduce EMI.
2. The two VMID capacitors (2x10 μ F) need to be placed as close as possible to the device DA9168.
3. The inductor input pin connected to GHG_LX pin should be as short as possible to reduce switching noise.
4. Make sure decoupling capacitors trace to the device pins as short as possible.
5. Split AGND (analog ground) and GND (power ground), and tie the analog ground and power ground with single ground connection.
6. For high current paths, ensure that the vias number and copper area is enough to support the operation current.

Note:

1. *Currently, there are two options for VSYS GND connection. Based on device evaluation results, recommend VSYS GND connect to AGND.*
2. *VBAT_SNS Capacitor can be removed if the battery connection is short enough.*

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

▪ Inductors

Manufacturers	Part #	Size (mm)	Inductance (μH)	Rdc (mΩ)		Heat Rating Current (A)		Saturation Current (A)	
				Typ	Max	Typ	Max	Typ	Max
Cyntec	HTEH20160H-1R0MSR	L = 2.0; W = 1.6 T = 0.8 (max)	1.0	29	35	4.4	4.0	4.0	3.6
Cyntec	HTEH20160H-2R2MSR	L = 2.0; W = 1.6 T = 0.8 (max)	2.2	75	90	2.6	2.3	2.9	2.7

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

▪ MLCC

Manufacturers	Part #	Size (mm)	Height (mm)	Capacitance (μF)	Rated voltage	Temp characteristics	ESR @1 MHz (Ω)	Position
Murata	GRM155R6YA105KE11	1005	0.5 ±0.1	1.0 ±10%	35 V	X5R	0.01	VBUS VBUS_SNS (*VBAT_SNS)
Murata	GRM155R61A106ME11	1005	0.5 ±0.2	10.0 ±20%	10 V	X5R	-	VSYS(2x)
Murata	GRM188R61E106MA73D	1608	0.8 ±0.2	10.0 ±20%	25 V	X5R	-	VMID (2x)
Taiyo Yuden	TMK105BJ473KV-F	1005	0.55 (Max)	0.047±10%	25 V	X5R	0.1	VBTS
Murata	GRM155R61C225KE11	1005	0.5 ±0.2	2.2 ±10%	16 V	X5R	0.008	VBAT VOUT1 VOUT2
Murata	GRM155R61C105KA12	1005	0.5 ±0.05	1.0 ±10%	16 V	X5R	0.02	VBAT_SNS
Murata	GRM185R61C475KE11	1608	0.5 ±0.05	4.7 ±10%	16 V	X5R	0.006	VREF

DA9168 GUI

For GUI Install and Setup, please refer to document:
“UM_PM_051_DA9168_Performance_Board_User_Manual”

SYSTEM STATUS REGISTERS

The screenshot shows the 'System Status' section of the DA9168BC tool. It displays four registers: PMC_STATUS_00, PMC_STATUS_01, PMC_STATUS_02, and PMC_STATUS_03. Each register has a set of status flags and their current values. A yellow box highlights the 'S_VBUS_OK' and 'S_VBUS_UV' flags in the PMC_STATUS_00 register. A blue box highlights the 'S_VBUS_UV' flag in the PMC_STATUS_01 register. A text box labeled 'Example: Rev-boost operation status' points to the 'S_VBUS_UV' flag in PMC_STATUS_01. Another text box labeled 'Read-only registers indicate device current status' points to the entire register display area. A 'Note' on the right states: 'Beside normal VBUS plug in/out condition, S_VBUS_OK and S_VBUS_UV status flags by REV_VBUS on/off'. At the bottom, there is a 'Console' window showing log messages and a 'Bitfield Info' window showing details for the 'S_VSYS_UV' bitfield.

Register	Flag	Value
PMC_STATUS_00	S_VBUS_VINDPM	VBUS not in VINDPM
	S_VBUS_IINDPM	VBUS not in IINDPM
	S_VMID_OC	VMID not in OC
	S_VBAT_OC	VBAT not in OC
	S_VBUS_OK	VBUS not in UV
	S_VMID_OK	VMID OK
	S_VSYS_OK	VSYS OK
	S_VBAT_OK	VBAT OK
	0x0000	0x07
	PMC_STATUS_01	S_VBUS_OV
S_VMID_OV		VMID not in OV
S_VSYS_OV		VSYS not in OV
S_VBAT_OV		VBAT not in OV
S_VBUS_UV		VBUS in UV
S_VMID_UV		VMID not in UV
S_VSYS_UV		VSYS not in UV
S_VBAT_UV		VBAT not in UV
0x0001		0x08
PMC_STATUS_02		S_TSD_CRIT
	S_TSD_WARN	Below
	S_WD_TIMER	Watch-dog timer not
	S_TS_HOT	Battery temp sens...
	S_TS_WARM	Battery temp sens...
	S_TS_COOL	Battery temp sens...
	S_TS_COLD	Battery temp sens...
	S_TS_OFF	Battery temp sens...
	0x0002	0x00
	PMC_STATUS_03	S_CHG_SLEEP
S_CHG_SPLMT		VBAT fet not
S_CHG_TIMER		Charge timer not
S_CHG_TRICKLE		Charger not in trickle
S_CHG_PRE		Charger not
S_CHG_CC		Charger not
S_CHG_CV		Charger not
S_CHG_DONE		Charge termination...
0x0003		0x00

Note:
Beside normal VBUS plug in/out condition,
S_VBUS_OK and S_VBUS_UV status flags by REV_VBUS on/off

SYSTEM EVENTS REGISTERS

The screenshot displays the DA9168BC register configuration tool. The main window is titled 'DA9168' and shows various functional registers under the 'SYSTEM' tab. A yellow box highlights the 'System Events' section, which includes registers for PMC_EVENT_00 through PMC_EVENT_04. Each event register has a list of bitfields with corresponding status indicators (e.g., 'VBUS not in VINDPM', 'VMID not in OC', 'VBAT not in OC', etc.) and a value field set to 0x0000. Below this, a text box states: 'Registers indicate device events, clear on read (Default)'. An arrow points from this text box to the 'PMC SYS 00' register, which is also highlighted with a yellow box. This register has bitfields for 'E_RD_CLR_DIS' (set to 'Low'), 'VSYS_MIN' (set to 3.7), and 'VINDPM' (set to 4.2). The value field for PMC SYS 00 is 0x000F. At the bottom, a console window shows a log of system events, including 'poller stopped' and 'starting poller' messages with timestamps and hex values. A 'Bitfield Info' window is open on the right, showing details for the 'E_VSYS_SHUTDOWN' bitfield in the 'PMC_EVENT_04' register, including its current value (0) and enumerated value ('VSYS not in SHUTDOWN').

Note:

Beside normal VBUS plug in/out condition, E_VBUS_OK and E_VBUS_UV events asserted by REV_VBUS on/off

INTERRUPT MASK REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

Interrupt mask bits

Register	Value
PMC_MASK_00	0x000A
PMC_MASK_01	0x000B
PMC_MASK_02	0x000C
PMC_MASK_03	0x000D
PMC_MASK_04	0x000E

System Status

System Events

Interrupt mask

M_VBUS_VINDPM Masked

M_VBUS_IINDPM Masked

M_VMID_OC Masked

M_VBAT_OC Masked

M_VBUS_OK Masked

M_VMID_OK Masked

M_VSYS_OK Masked

M_VBAT_OK Masked

M_VSYS_SHUTDOWN Masked

M_REF_OC Masked

M_LDO2_IMON1 Masked

M_LDO2_IMON2 Masked

M_LDO2_OC Masked

M_LDO1_IMON1 Masked

M_LDO1_IMON2 Masked

M_LDO1_OC Masked

M_VBUS_OV Masked

M_VMID_OV Masked

M_VSYS_OV Masked

M_VBAT_OV Masked

M_VBUS_LUV Masked

M_VMID_LUV Masked

M_VSYS_LUV Masked

M_VBAT_LUV Masked

M_TSD_CRIT Masked

M_TSD_WARN Masked

M_WD_TIMER Masked

M_TS_HOT Masked

M_TS_WARM Masked

M_TS_COOL Masked

M_TS_COLD Masked

M_TS_OFF Masked

M_CHG_SLEEP Masked

M_CHG_SPLMT Masked

M_CHG_TIMER Masked

M_CHG_TRICKLE Masked

M_CHG_PRE Masked

M_CHG_CC Masked

M_CHG_CV Masked

M_CHG_DONE Masked

INT_N signal masked for all events (Default) which means INT_N no react while these events triggered.

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

Interrupt mask bits

Register	Value
PMC_MASK_00	0x000A
PMC_MASK_01	0x000B
PMC_MASK_02	0x000C
PMC_MASK_03	0x000D
PMC_MASK_04	0x000E

System Status

System Events

Interrupt mask

M_VBUS_VINDPM Masked

M_VBUS_IINDPM Masked

M_VMID_OC Masked

M_VBAT_OC Masked

M_VBUS_OK Masked

M_VMID_OK Masked

M_VSYS_OK Masked

M_VBAT_OK Masked

M_VSYS_SHUTDOWN Masked

M_REF_OC Masked

M_LDO2_IMON1 Masked

M_LDO2_IMON2 Masked

M_LDO2_OC Masked

M_LDO1_IMON1 Masked

M_LDO1_IMON2 Masked

M_LDO1_OC Masked

M_VBUS_OV Masked

M_VMID_OV Masked

M_VSYS_OV Masked

M_VBAT_OV Masked

M_VBUS_LUV Masked

M_VMID_LUV Masked

M_VSYS_LUV Masked

M_VBAT_LUV Masked

M_TSD_CRIT Masked

M_TSD_WARN Masked

M_WD_TIMER Masked

M_TS_HOT Masked

M_TS_WARM Masked

M_TS_COOL Masked

M_TS_COLD Masked

M_TS_OFF Masked

M_CHG_SLEEP Masked

M_CHG_SPLMT Masked

M_CHG_TIMER Masked

M_CHG_TRICKLE Masked

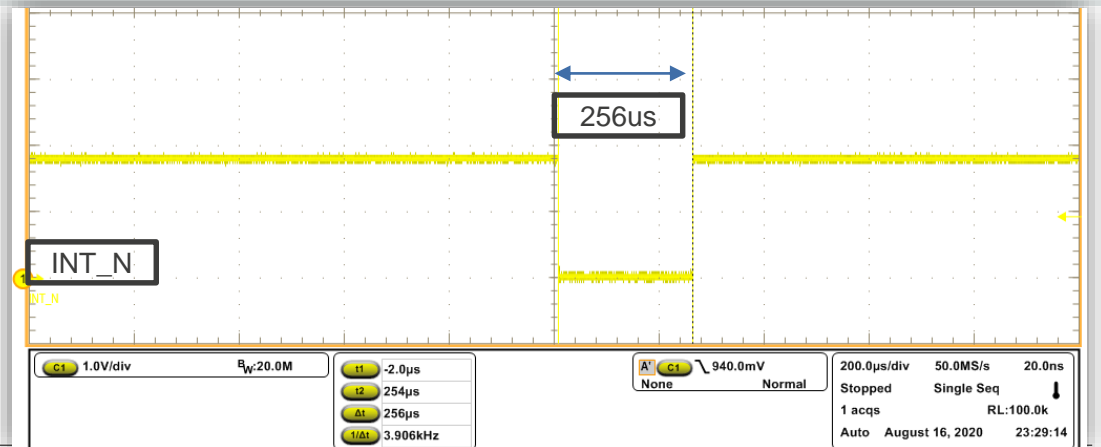
M_CHG_PRE Masked

M_CHG_CC Masked

M_CHG_CV Masked

M_CHG_DONE Not Masked

Example: M_CHG_DONE register is set as "Not masked"



SYSTEM REGISTERS

DA9168BC
File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

System

Chip ID

OTP_DEVICE_ID
DEV_ID: 215
0x0042 0xD7

OTP_VARIANT_ID
MRC: 1
VRC: 0
0x0043 0x10

OTP_CONFIG_ID
CONFIG_REV: 0
0x0044 0x00

System settings

PMC_SYS_00
E_RD_CLR_DIS: Low
VSYS_MIN: 3.7
VINDPM: 4.2
0x000F 0x38

PMC_SYS_01
VSYS_OV_SHUTDOWN_DIS: System
VSYS_UV_SHUTDOWN_DIS: System
ILIMIT_EN: No IINDPM update
IINDPM: 0.1
0x0010 0x00

PMC_SYS_02
BTS_VBAT_RATE: 50 ms
BTS_VBAT_EN: Disable
BTS_VBUS_RATE: 50 ms
BTS_VBUS_EN: Disable
VBAT_DEB: 100
VBUS_DEB: 100
0x0011 0x0A

PMC_SYS_03
SYS_WAIT: 1
WD_TMR: 160
WD_EN: No action
RST_TMR: 12
RST_REG: No action
0x0012 0x34

PMC_SYS_04
BOOST_PWM: Auto-mode
SEQ_BOOST: BOOST_EN is set w...
DLOAD_VMID_SEL: 30
DLOAD_VMID_EN: Disable
REV_VBUS_EN: Disable
BOOST_EN: Disable
0x0013 0x38

PMC_SYS_05
REV_VBUS_ILIM: 1.0
BOOST_VOUT: 5.0
0x0014 0x9A

PMC_SYS_06
RST_SYS: No action
RIN_N_SHIP_EXIT_TMR: 20 ms
VBUS_OVSEL: 5.6
HIZ_MODE: VBUS when available
SHIP_DLY: 10
SHIP_MODE: No action
0x0015 0x06

VSYS_OV_SHUTDOWN_DIS: Disable VSYS shutdown once VSYS_OV triggered
VSYS_UV_SHUTDOWN_DIS: Disable VSYS shutdown once VSYS_UV triggered
IINDPM_EN: IINDPM setting by ILIMIT pin option (Not support this function)
IINDPM setting: 0.1 A to 2.5 A with 0.1 A/step

BTS_VBAT_RATE: BAT temp sense interval @ battery operation
BTS_VBAT_EN: Enable BAT temp sense @ battery operation
BTS_VBUS_RATE: BAT temp sense interval @ VBUS supply present
BTS_VBUS_EN: Enable BAT temp sense @ VBUS supply present
VBAT_DEB: VBAT detection debounce time (ms)
VBUS_DEB: VBUS detection debounce time (ms)

Read-on-clear event register function enable/disable

VSYS minimum voltage setting: 3.4 V to 3.7 V with 0.1 V/step

VINDPM setting: 3.8 V to 4.8 V with 0.1 V/step

Boost operation mode option

Boost enable by EN pin option

VMID dummy-load setting (mA)

VMID dummy-load enable/disable

Reverse VBUS (OTG) enable/disable

Reverse boost enable/disable

Reverse boost VOUT setting: 4.0 V to 5.5 V with 0.1 V/step

Reverse VBUS (OTG) current limit setting: 0.1 A to 1 A with 0.1 A/step

SYS_WAIT: VSYS power-off time for system power recovery cycle (s)
WD_TMR: watch-dog timer expire time (s)
WD_EN: watch-dog timer enable/disable
RST_TMR: RIN_N button press time (s) to reset the system
RST_REG: Triggers registers initialization

System reset while set to high

RIN_N debounce time to exit from ship mode: 2 s/20 ms

VBUS over voltage threshold setting

HIZ mode option

Ship mode enter delay (s)

Ship mode enter/exit

Status

Console Log

Clear Mark Save to file Filter (reg expr): Log level: Info

2020-12-18, 10:43:42 [INFO] USB connected: U
2020-12-18, 10:43:42 [INFO] ready...
2020-12-18, 10:43:42 [INFO] Startup took: 0.90 sec
2020-12-18, 10:43:44 [INFO] no callables left to run...

Bitfield Info

Bitfield: WD_TMR
Register: PMC_SYS_03 (0x12)
Bits: [5:4]
Access: R/W
POR: 3
Current Value: 3
Enumerated Value: 160

CHARGER REGISTERS

BC Silicon New option at charging mode:

Recharge voltage threshold offset setting
0: 100 mV; 1: 200 mV

Charger safety timer rate reduced to half while relevant events triggered.

Charger safety timer enable/disable

Charger termination enable/disable

Charger enable/disable
(CHG_EN_N pin pulldown at the same time to enable charger)

CHG_TMR_SAFE: charger safty timer setting (h)
CHG_TMR_PRE: Pre-charge safty timer setting (min)
CHG_TOPOFF: Topoff timer setting (min) or disable

CHG_IPRE_MSB: Adds offset to pre-charge current setting (mA) while set to 1
CHG_RANGE_TERM: Charging current range settings for CHG_ITERM. For Higher range, CHG_RANGE need set to 1
CHG_RANGE_PRE: Charging current range settings for CHG_IPRE. For Higher range, CHG_RANGE need set to 1
CHG_ITERM: Termination charge current setting (mA)
CHG_IPRE: Pre-charge current setting(mA)

CHG_RANGE: Fast charge current range
0: 20 mA to 500 mA
1: 80 mA to 2000 mA
CHG_ICHG: Fast charge current setting

Fast charge current setting during TS event@ CHG_TS_COOL_I =1
CHG_RANGE = 0: TS_ICHG 20 mA to 500 mA
CHG_RANGE = 1: TS_ICHG 80 mA to 2000 mA

Battery regulation voltage setting: 4.0V to 4.5V with 10mV/step

- IO_INT_N_PD: INT_N pin internal pull-up
- IO_EN_PD: EN pin internal pull-down
- IO_CHG_EN_N_PD: CHG_EN_N pin internal pull-down
- TS_VBATREG_SHIFT: Battery regulation voltage shift down 100 mV/200 mV during temp sense warm event triggered @ CHG_TS_WARN_V=1

The screenshot shows the DA9168Charger configuration tool interface. It features several tabs: FUNCTIONAL REGISTERS, SYSTEM, CHARGER, and LDO. The CHARGER tab is active, displaying a grid of register settings for PMCHG_00 through PMCHG_06. The settings include:

- PMCHG_00:** BUCK_PWM, CHG_VRCHG (100), CHG_TMR_HALF_EN (Enable), CHG_TMR_EN (Enable), CHG_TERM_EN (Enable), CHG_EN (Disable).
- PMCHG_01:** CHG_TMR_SAFE (5), CHG_TMR_PRE (30), CHG_TOPOFF (Disable-TOPOFF).
- PMCHG_02:** CHG_IPRE_MSB (+0), CHG_RANGE_TERM (5-25 mA, in 5), CHG_RANGE_PRE (5-15 mA, in 5), CHG_ITERM (CHG_RANGE = 0), CHG_IPRE (CHG_RANGE = 0).
- PMCHG_03:** CHG_RANGE (Fast-charge 20 mA), CHG_ICHG (CHG_RANGE = 0).
- PMCHG_04:** HG_VBATREG (4.20).
- PMCHG_05:** IO_INT_N_PD (Disable), IO_EN_PD (Disable), IO_CHG_EN_N_PD (Disable), TS_VBATREG_SHIFT (100), CHG_TS_WARM_V (Disable), CHG_TS_COOL_I (Disable).
- PMCHG_06:** TS_ICHG (CHG_RANGE = 0).

At the bottom, there is a Console window with a Log button and a Bitfield Info window showing details for the CHG_RANGE register (PMCHG_03, bit 7).

LDOs/LSWS REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

LDO settings

PMC_LDO_00

LDO2_OCP Disable

LDO2_PD Enable

LDO2_LSW LDO mode

LDO2_EN Disable

LDO1_OCP Disable

LDO1_PD Enable

LDO1_LSW LDO mode

LDO1_EN Disable

0x001D 0x44

PMC_LDO_01

SEQ_LDO1 LDO1 not enabled

LDO1_VOUT 3.0

0x001E 0x22

PMC_LDO_02

SEQ_LDO2 LDO2 not enabled

LDO2_VOUT 3.0

0x001F 0x22

PMC_LDO_04

SYS_WAIT_CFG Default setting

RST_OPT_PWRCYC Triggers power-cycle

SHIP_DLY_DIS After SHIP_DLY

RST_OPT On RIN_N rise

VBAT_OV_CFG Shut-down

CHG_TRICKLE_CYC Cyclic mode enabled

CHG_TRICKLE 14 / 7

0x0021 0x55

PMC_LDO_05

DO2_ILIM 487

DO1_ILIM 487

0x0022 0xAA

LDOx VOUT setting:
1.6 V to 5.2 V with 0.1 V/step

LDOx current limit setting

LDOx OCP option:
0: LDOx disable while trigger OCP
1: LDOx hiccup while trigger OCP

LDOx PD SW option:
0: LDOx PD switch disable
1: LDOx PD switch enable

LDOx_LSW mode option:
0: LDO mode
1: Load SW mode

LDOx_EN:
0: LDOx disable
1: LDOx enable

LDOx sequence option:
0: LDOx not enabled by EN pin
1: Enable LDOx ASAP after EN pin rise
2: Enable LDOx 0.25 ms after EN pin rise
3: Enable LDOx 0.5 ms after EN pin rise

New options for BC silicon

Console Log

Clear Mark Save to file Filter (reg expr): Log level: Info

```

2021-12-14, 10:52:32 [INFO] poller stopped
2021-12-14, 10:53:08 [INFO] starting poller
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0000, value: 0x0b <-
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0001, value: 0x00 <-
2021-12-14, 10:53:13 [INFO] poller stopped
2021-12-14, 10:53:30 [INFO] DA9168 addr: 0x0013, value: 0x39 -->
2021-12-14, 10:53:35 [INFO] starting poller
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0000, value: 0x07 <-
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0001, value: 0x08 <-
2021-12-14, 10:53:37 [INFO] poller stopped
    
```

Bitfield Info

Bitfield: LDO1_ILIM
Register: PMC_LDO_05 (0x22)
Bits: [3:0]
Access: R/W
POR: 13

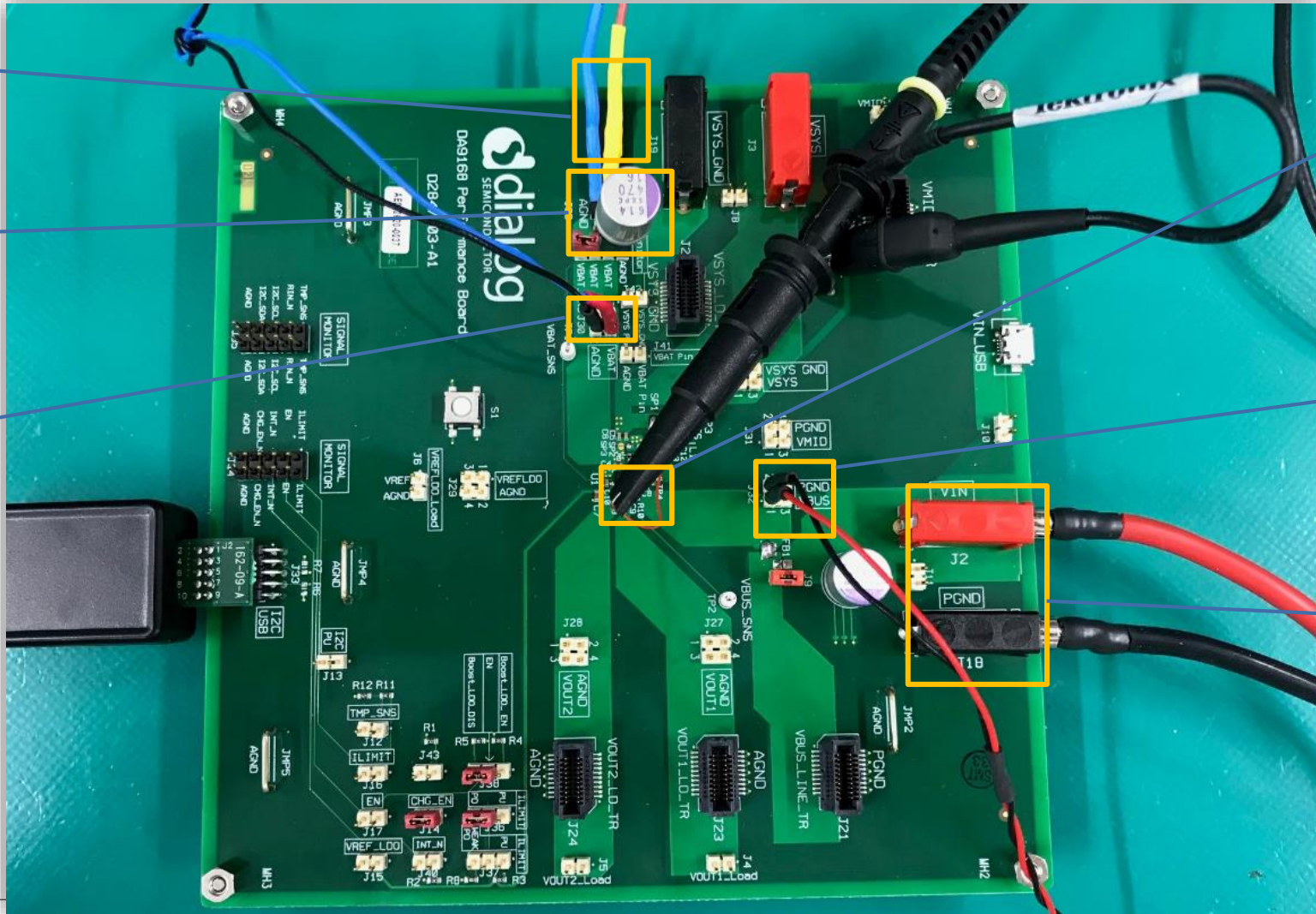
Current Value: 10
Enumerated Value: 487

Chipmodel Blocks:
PMC: LDO1_ILIM

Description:
VOUT1 current limit (mA)

TEST BENCH SETUP

CHARGE MODE BOARD SETUP



VBAT Connection

VLX Signal

Highly recommend:
Bulk electrolytic cap for
VBAT connector to prevent
VBAT voltage oscillation due to
the long cable

VBUS Sense

VBAT Sense

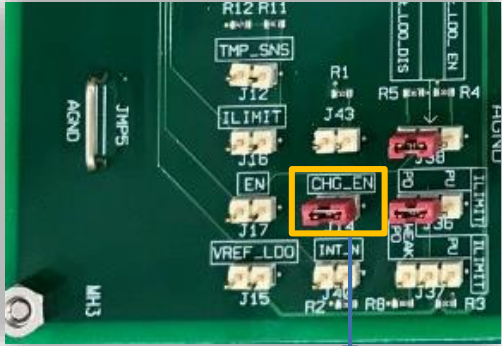
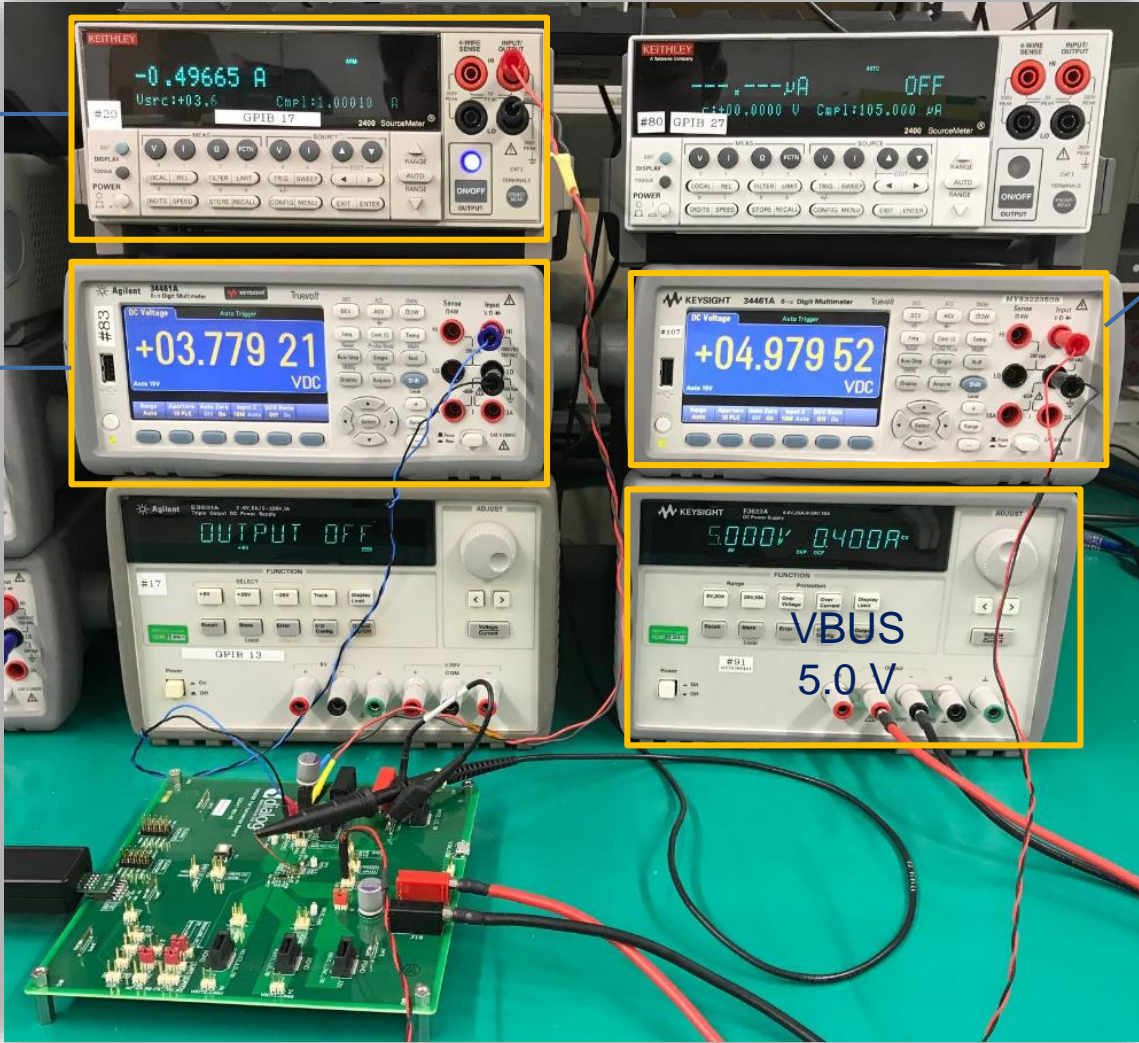
VBUS Connection

CHARGE MODE TEST BENCH SETUP

VBAT charging current

VBAT Sense
3.779 V

VBUS Sense
4.979 V



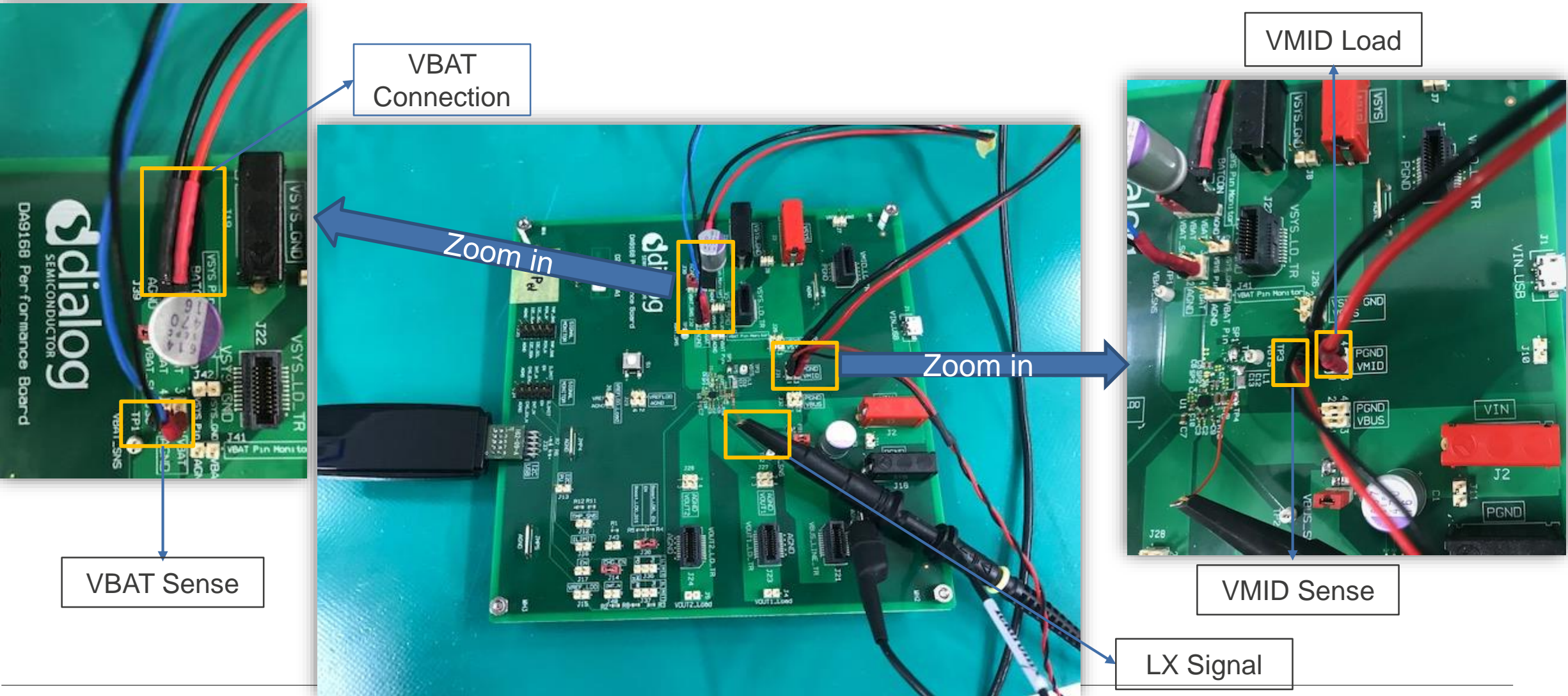
CHG_EN_N pin pulldown

PMC_CHG_00

BUCK_PWM	Auto-mode
CHG_VRCHG	100
CHG_TMR_HALF_EN	Enable
CHG_TMR_EN	Enable
CHG_TERM_EN	Enable
CHG_EN	Enable
0x0016	0x0F

CHG_EN set to High

REV-BOOST MODE BOARD SETUP



REV-BOOST MODE TEST BENCH SETUP

VBAT Sense
3.68 V

VBAT
3.7 V

VMID Load
(200 mA)

VMID Output
4.982 V

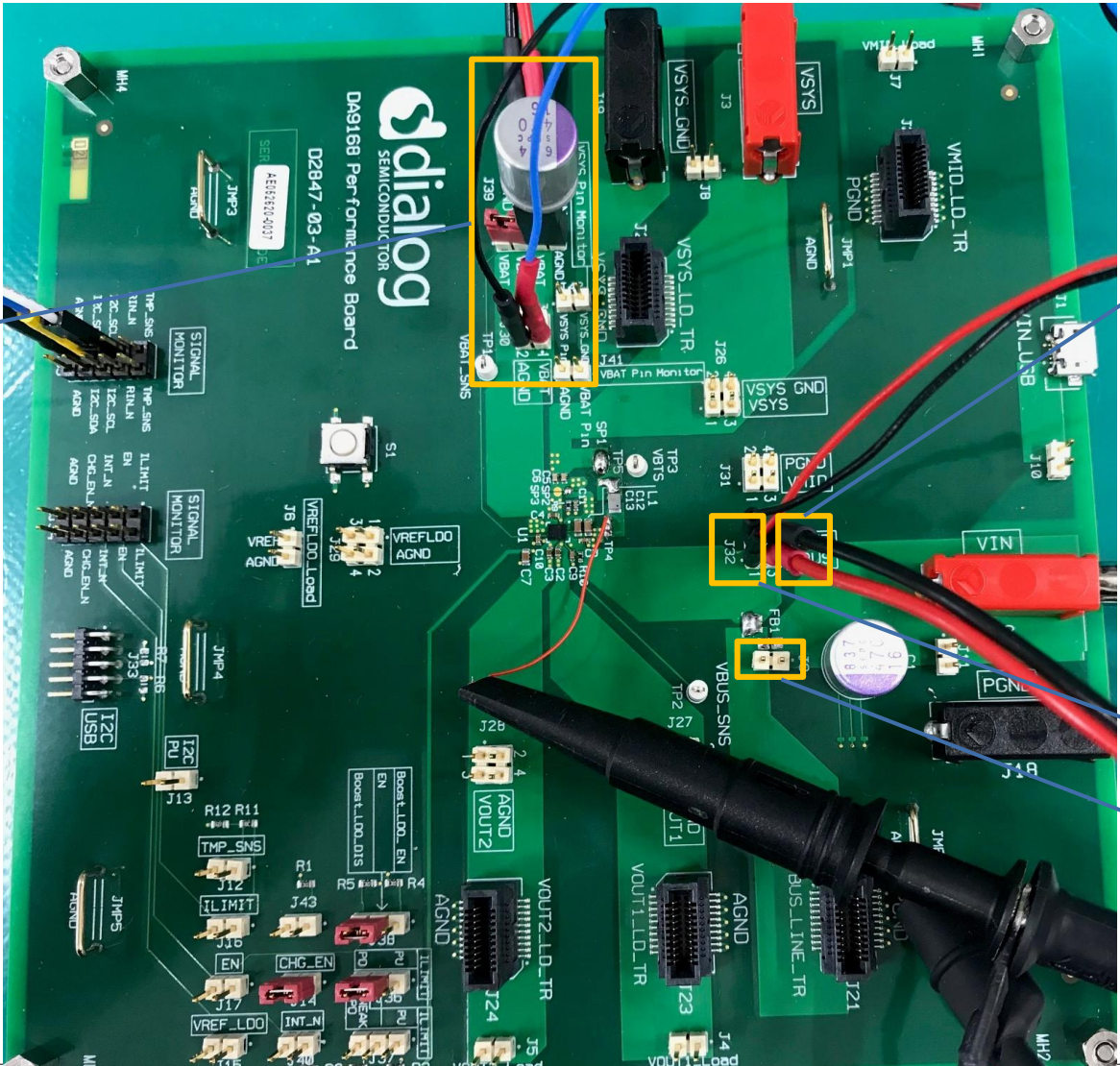
PMC_SYS_04

BOOST_PWM	Auto-mode
SEQ_BOOST	BOOST_EN is set w...
DLOAD_VMID_SEL	30
DLOAD_VMID_EN	Disable
REV_VBUS_EN	Disable
BOOST_EN	Enable
0x0013	0x39

BOOST_EN set to High

REV-VBUS (OTG) BOARD SETUP

VBAT and VBAT sense connections are same with Rev_boost setup

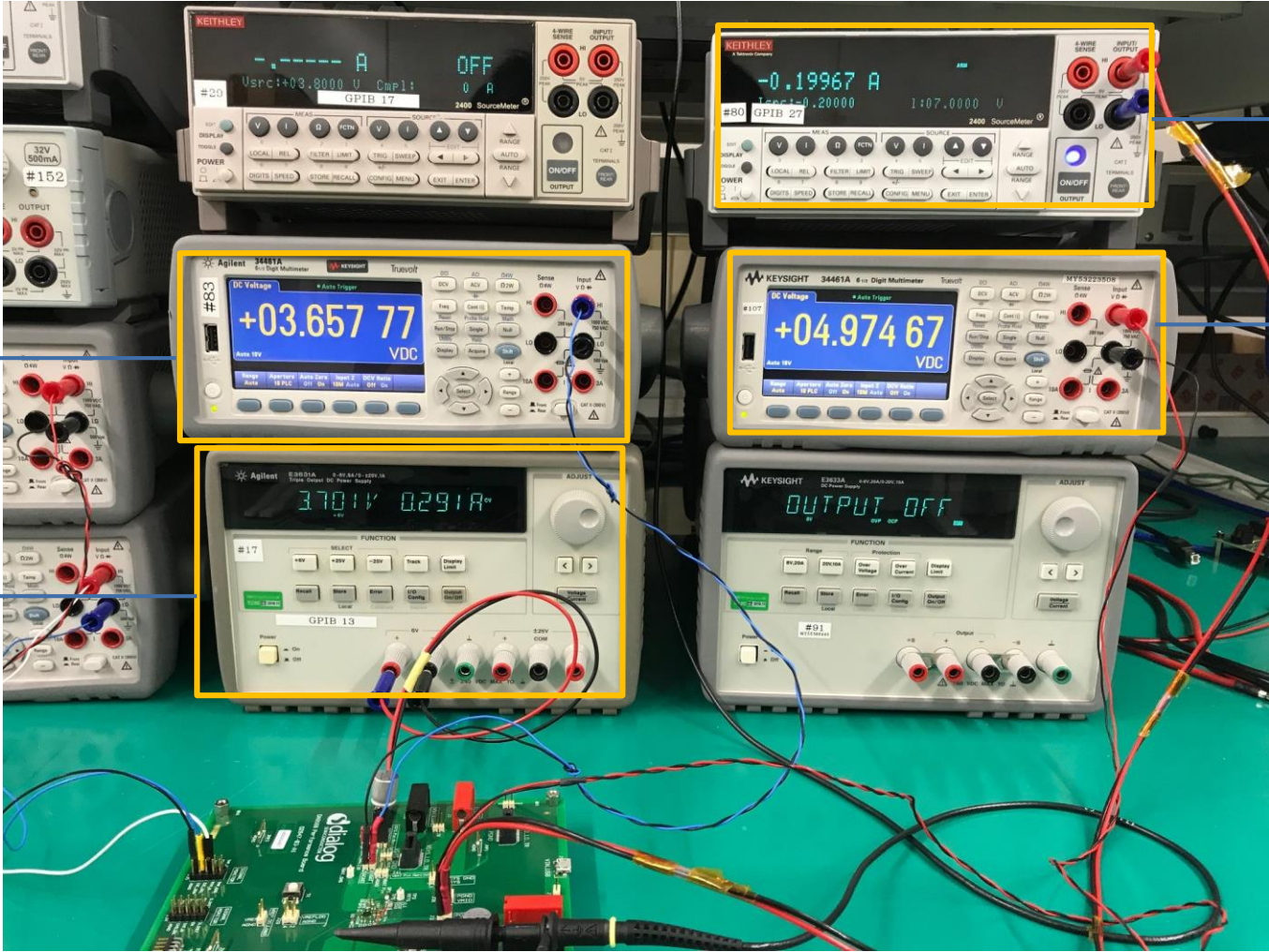


Rev-VBUS Load

Rev-VBUS Sense

Remove jumper J9

REV-VBUS (OTG) TEST BENCH SETUP



VBAT Sense
3.657 V

VBAT
3.7 V

Rev-VBUS Load
(200 mA)

Rev-VBUS Output
4.974 V

PMC_SYS_04

BOOST_PWM	Auto-mode
SEQ_BOOST	BOOST_EN is set w...
DLOAD_VMID_SEL	30
DLOAD_VMID_EN	Disable
REV_VBUS_EN	Enable
BOOST_EN	Enable
0x0013	0x3B

REV_VBUS_EN set to High
BOOST_EN set to High

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