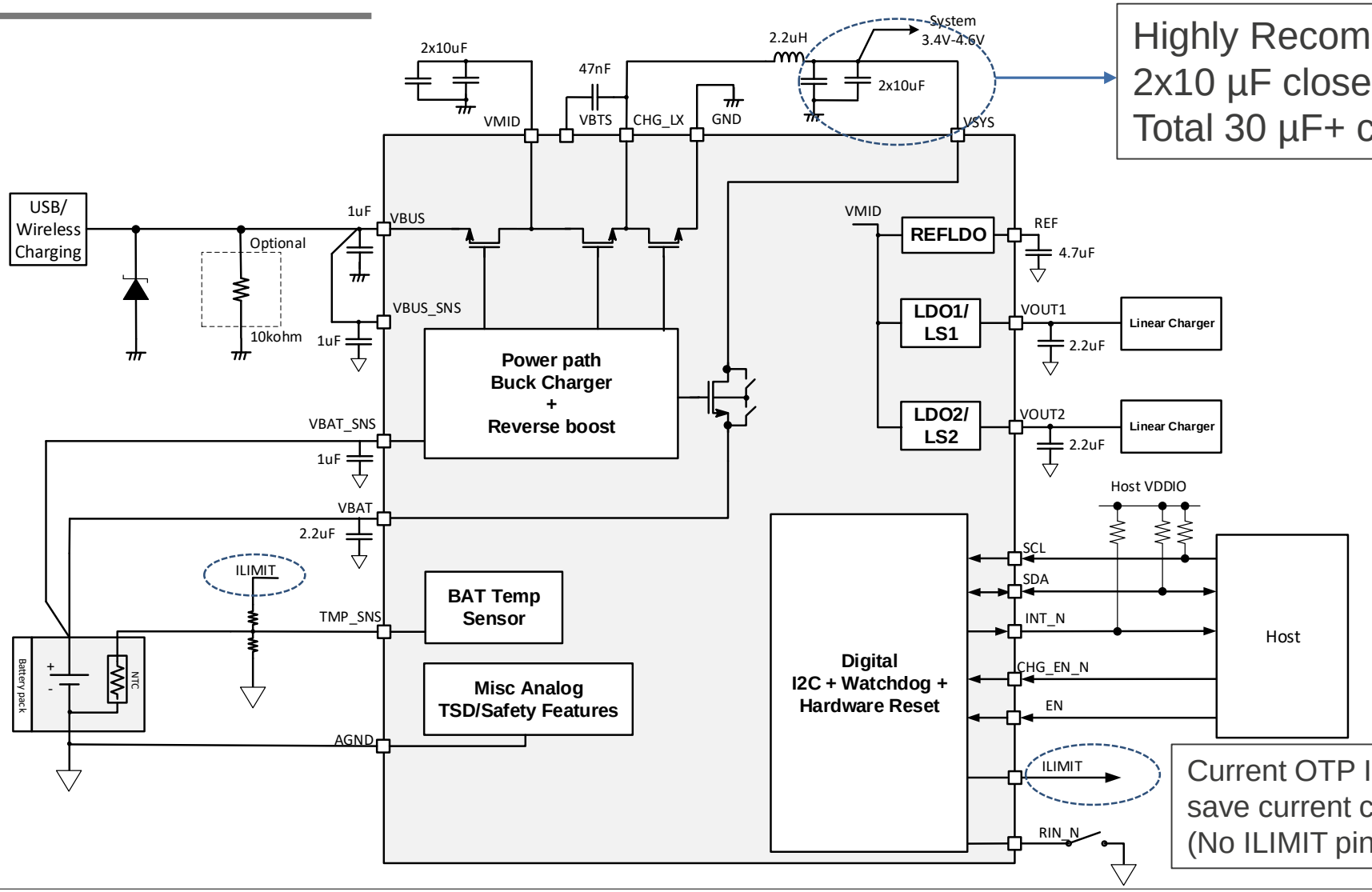
DA9168BC APPLICATION NOTE

FEB 2022
RENESAS ELECTRONICS CORPORATION

TYPICAL TWS APPLICATION WITH CURRENT OTP



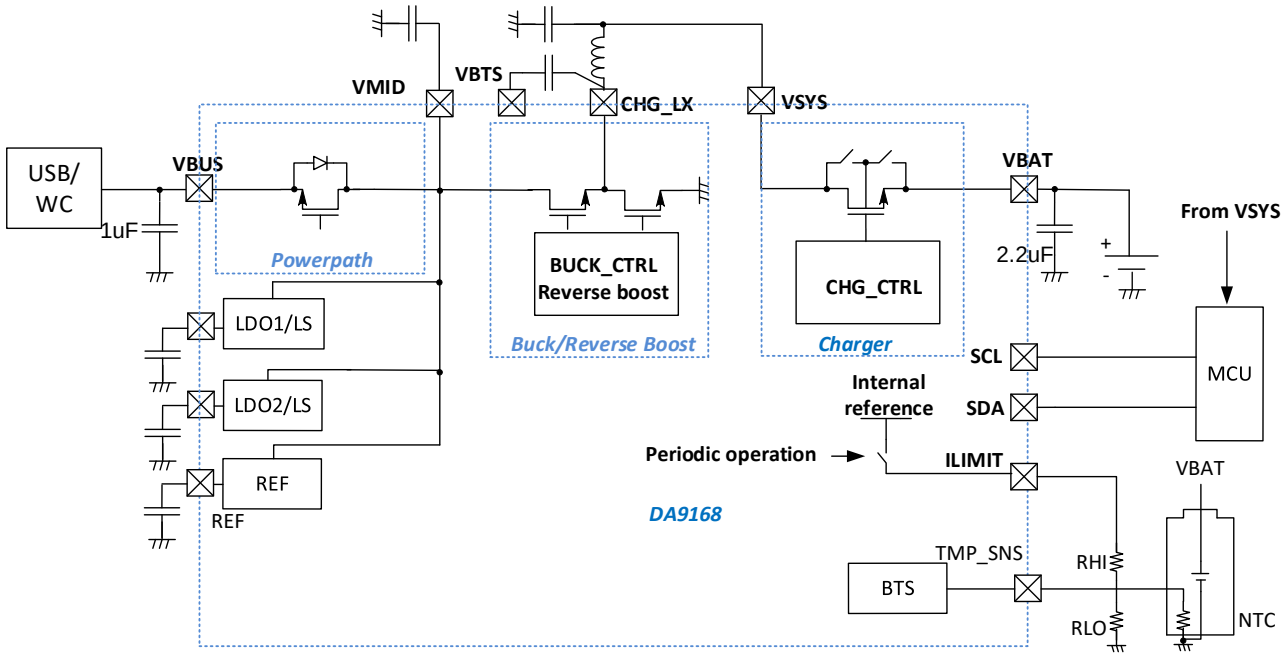
Highly Recommend:
2x10 µF close to DA9168 side.
Total 30 µF+ cap for the system power rail.

Current OTP ILIMIT pin is used as BTS power rail to save current consumption.
(No ILIMIT pin status control IINDPM function)

DA9168 BTS WITH ILIMT PIN

BTS WITH ILIMIT - VBUS IQ

Using ILIMIT pin (instead of REF) for BTS has large I_Q savings

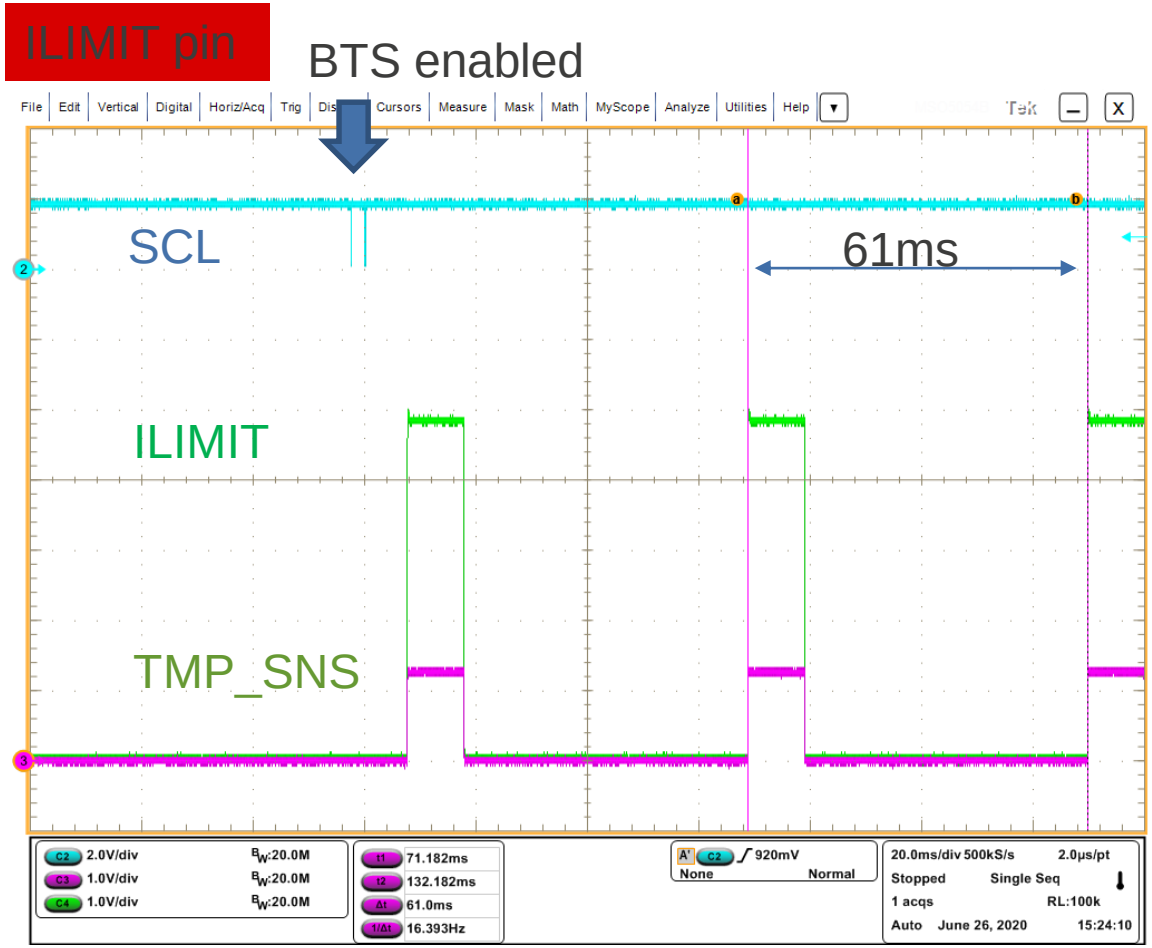


BTS Reference	BTS	Condition	I_Q from VBAT (µA)	Savings (µA)
REF	Disabled	Reverse boost + REFLDO	377	-
REF	Enabled	Reverse boost + REFLDO + BTS (50msec)	380	-
REF	Enabled	Reverse boost + REFLDO + BTS (2 sec)	377	-
ILIMIT	Disabled	Standby (boost disable)	10	367
ILIMIT	Enabled	Standby (boost disable) + BTS (50 msec)	41	339
ILIMIT	Enabled	Standby (boost disable) + BTS (2 sec)	11	366

I_Q increase from BTS just ~1 µA

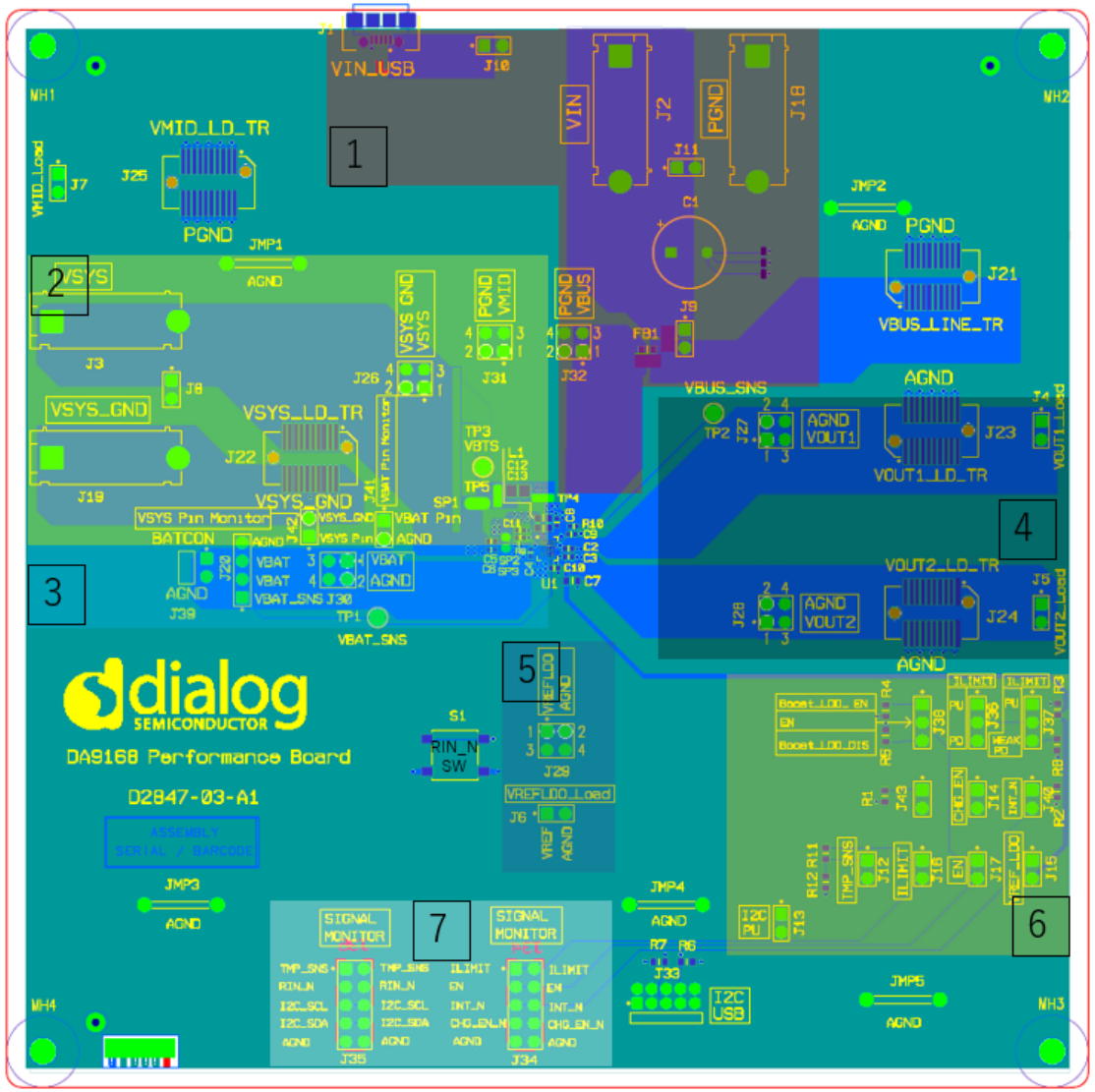
BTS WITH ILIMIT - PERIODIC OPERATION

✓ BTS periodic operation working as expected



DA9168 PERFORMANCE BOARD

PERFORMANCE BOARD OVERVIEW

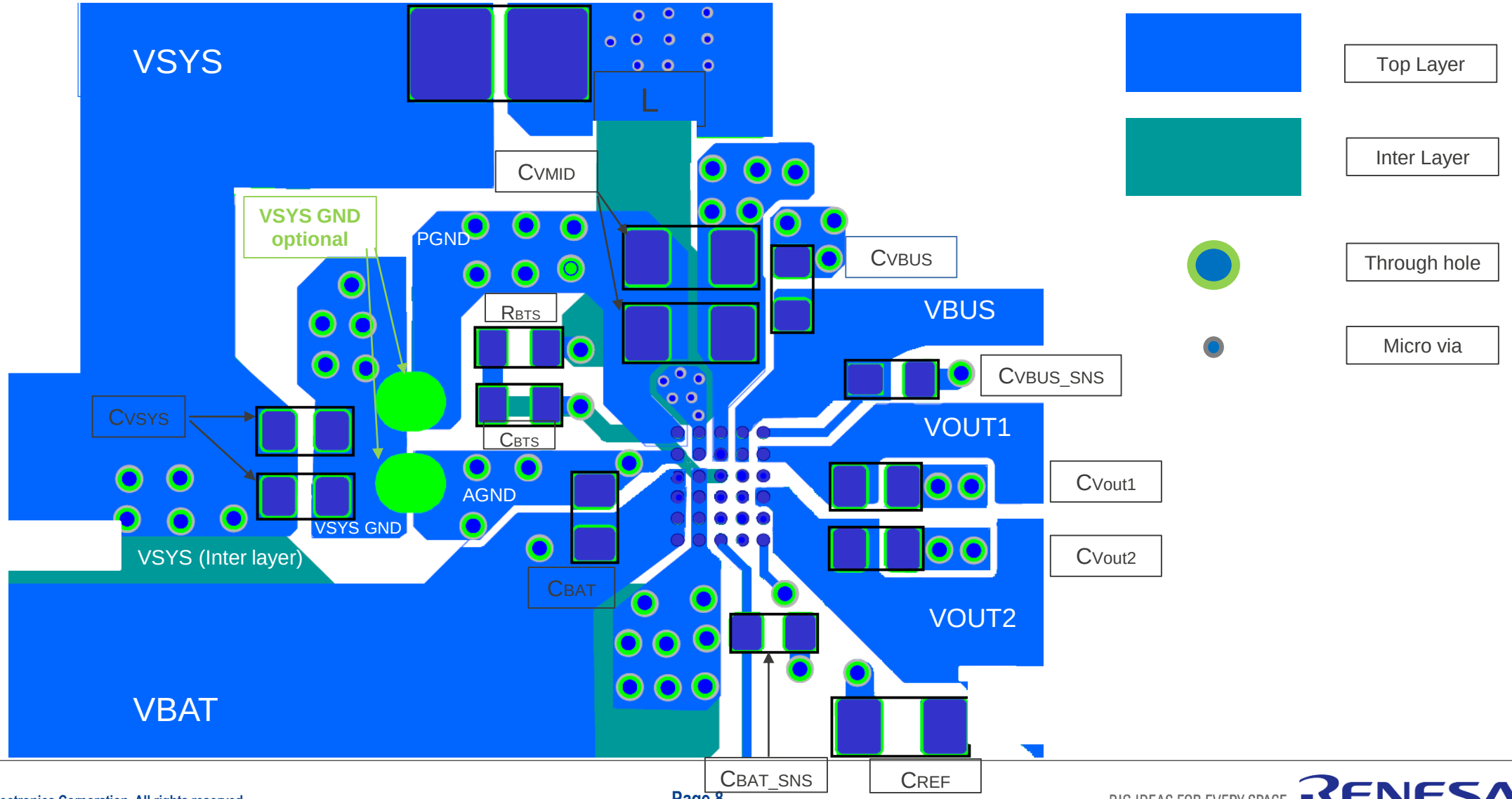


CAUTION

Apply high current to J26, J27, J28, J29, J30, J31, J32, J41 and J42 headers pin 1 and 2 may causes the voltage sensing traces burn out.

1. VBUS input section: Power supply and USB power supply connectors.
2. VSYS output section.
3. VBAT input/output section.
4. VOUT1 and VOUT2 outputs section.
5. REFLDO output section.
6. GPIOs network section.
7. GPIOs signal monitors section.

DA9168 PERFORMANCE BOARD LAYOUT CONCEPT



LAYOUT GUIDELINES

1. Minimize high frequency current path loop (VMID – CHG_LX – VSYS – GND and CHG_LX – VSYS - GND) to reduce EMI.
2. The two VMID capacitors (2x10 µF) need to be placed as close as possible to the device DA9168.
3. The inductor input pin connected to GHG_LX pin should be as short as possible to reduce switching noise.
4. Make sure decoupling capacitors trace to the device pins as short as possible.
5. Split AGND (analog ground) and GND (power ground), and tie the analog ground and power ground with single ground connection.
6. For high current paths, ensure that the vias number and copper area is enough to support the operation current.

Note:

1. *Currently, there are two options for VSYS GND connection. Based on device evaluation results, recommend VSYS GND connect to AGND.*
2. *VBAT_SNS Capacitor can be removed if the battery connection is short enough.*

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

- Inductors

Manufacturers	Part #	Size (mm)	Inductance (µH)	Rdc (mΩ)		Heat Rating Current (A)		Saturation Current (A)	
				Typ	Max	Typ	Max	Typ	Max
Cyntec	HTEH20160H-1R0MSR	L = 2.0; W = 1.6 T = 0.8 (max)	1.0	29	35	4.4	4.0	4.0	3.6
Cyntec	HTEH20160H-2R2MSR	L = 2.0; W = 1.6 T = 0.8 (max)	2.2	75	90	2.6	2.3	2.9	2.7

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

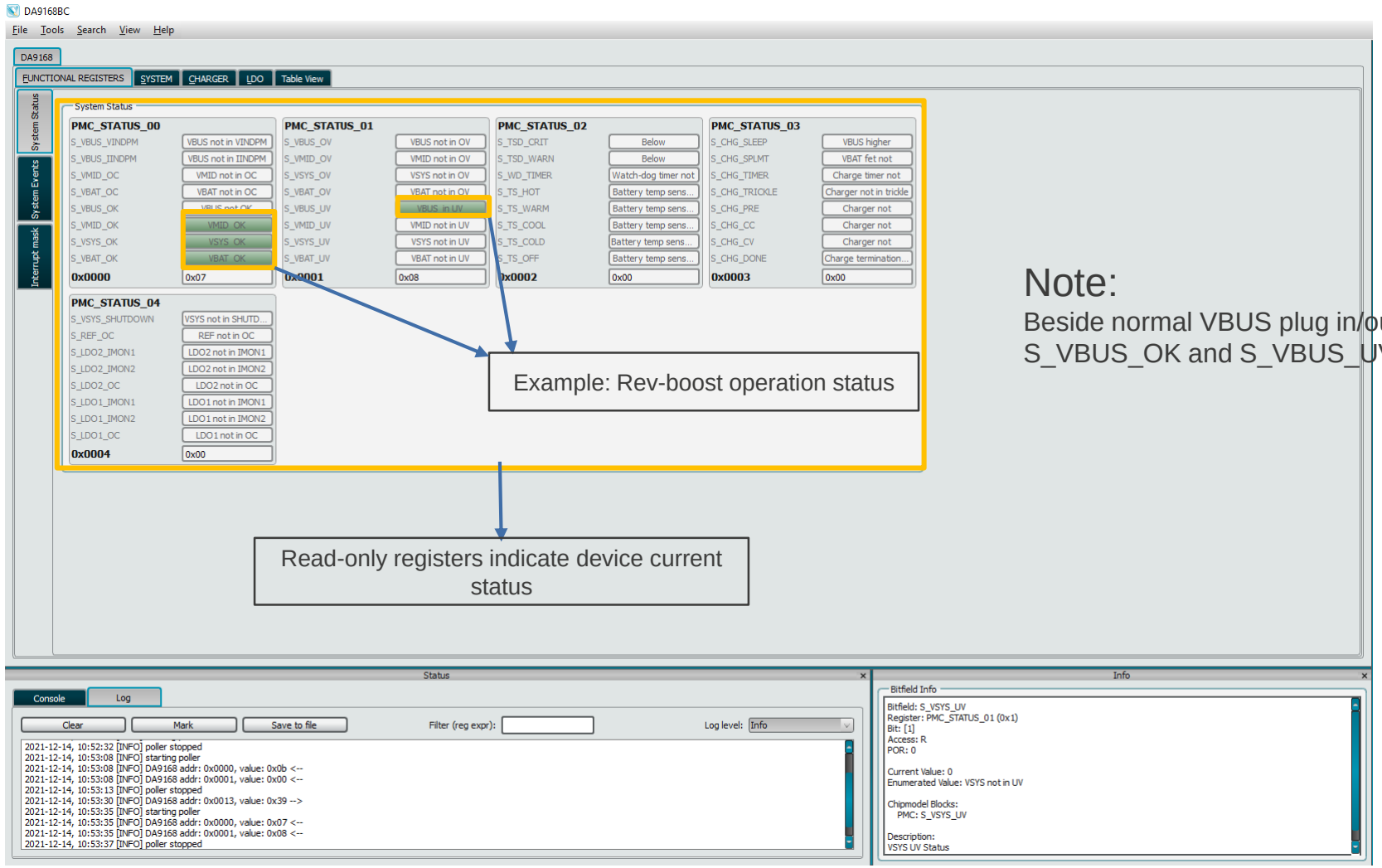
- MLCC

Manufacturers	Part #	Size (mm)	Height (mm)	Capacitance (µF)	Rated voltage	Temp characteristics	ESR @1 MHz (Ω)	Position
Murata	GRM155R6YA105KE11	1005	0.5 ±0.1	1.0 ±10%	35 V	X5R	0.01	VBUS VBUS_SNS (*VBAT_SNS)
Murata	GRM155R61A106ME11	1005	0.5 ±0.2	10.0 ±20%	10 V	X5R	-	VSYS(2x)
Murata	GRM188R61E106MA73D	1608	0.8 ±0.2	10.0 ±20%	25 V	X5R	-	VMID (2x)
Taiyo Yuden	TMK105BJ473KV-F	1005	0.55 (Max)	0.047±10%	25 V	X5R	0.1	VBTS
Murata	GRM155R61C225KE11	1005	0.5 ±0.2	2.2 ±10%	16 V	X5R	0.008	VBAT VOUT1 VOUT2
Murata	GRM155R61C105KA12	1005	0.5 ±0.05	1.0 ±10%	16 V	X5R	0.02	VBAT_SNS
Murata	GRM185R61C475KE11	1608	0.5 ±0.05	4.7 ±10%	16 V	X5R	0.006	VREF

DA9168 GUI

For GUI Install and Setup, please refer to document:
“UM_PM_051_DA9168_Performance_Board_User_Manual”

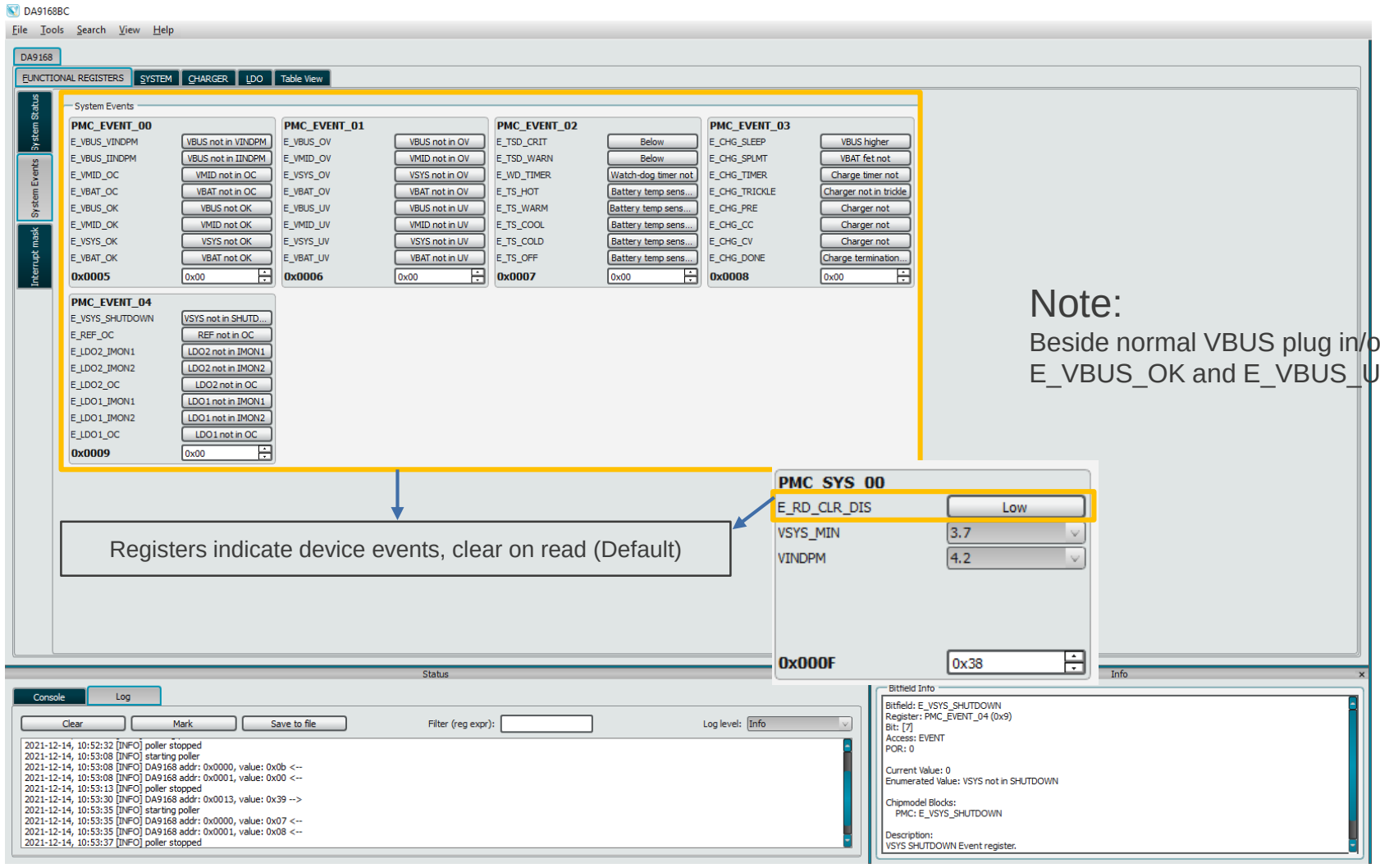
SYSTEM STATUS REGISTERS



Note:

Beside normal VBUS plug in/out condition,
S_VBUS_OK and S_VBUS_UV status flags by REV_VBUS on/off

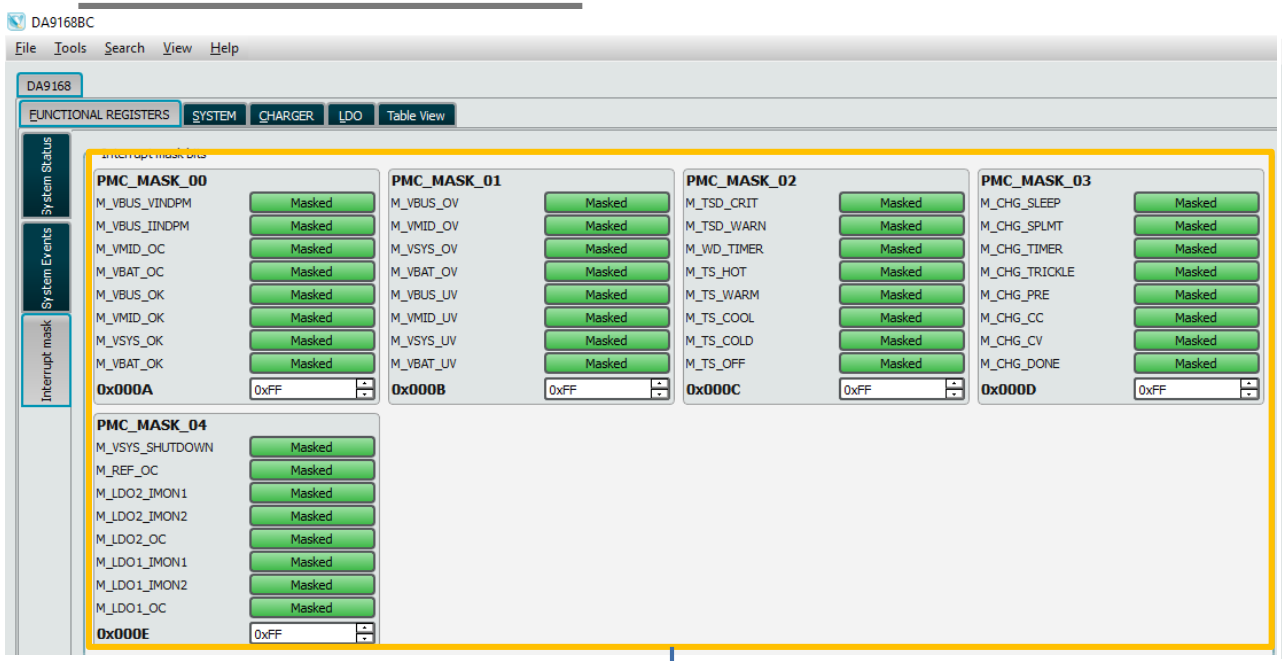
SYSTEM EVENTS REGISTERS



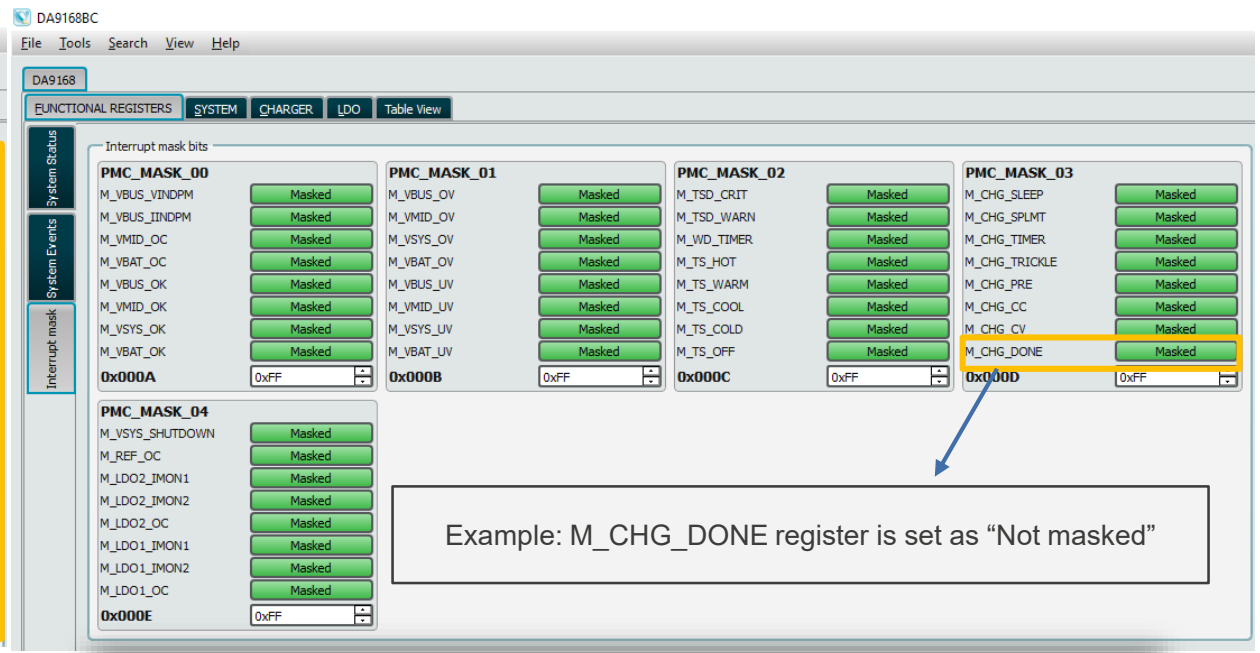
Note:

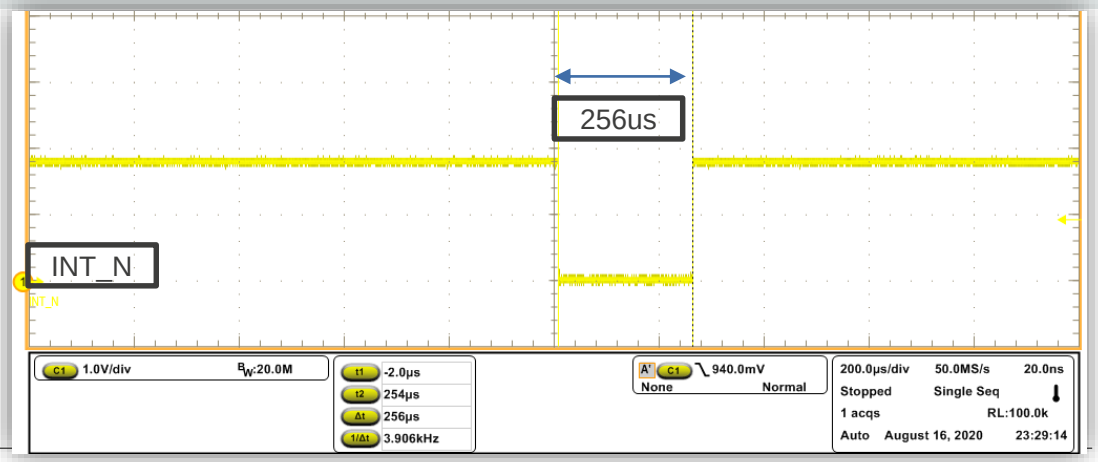
Beside normal VBUS plug in/out condition,
E_VBUS_OK and E_VBUS_UV events asserted by REV_VBUS on/off

INTERRUPT MASK REGISTERS

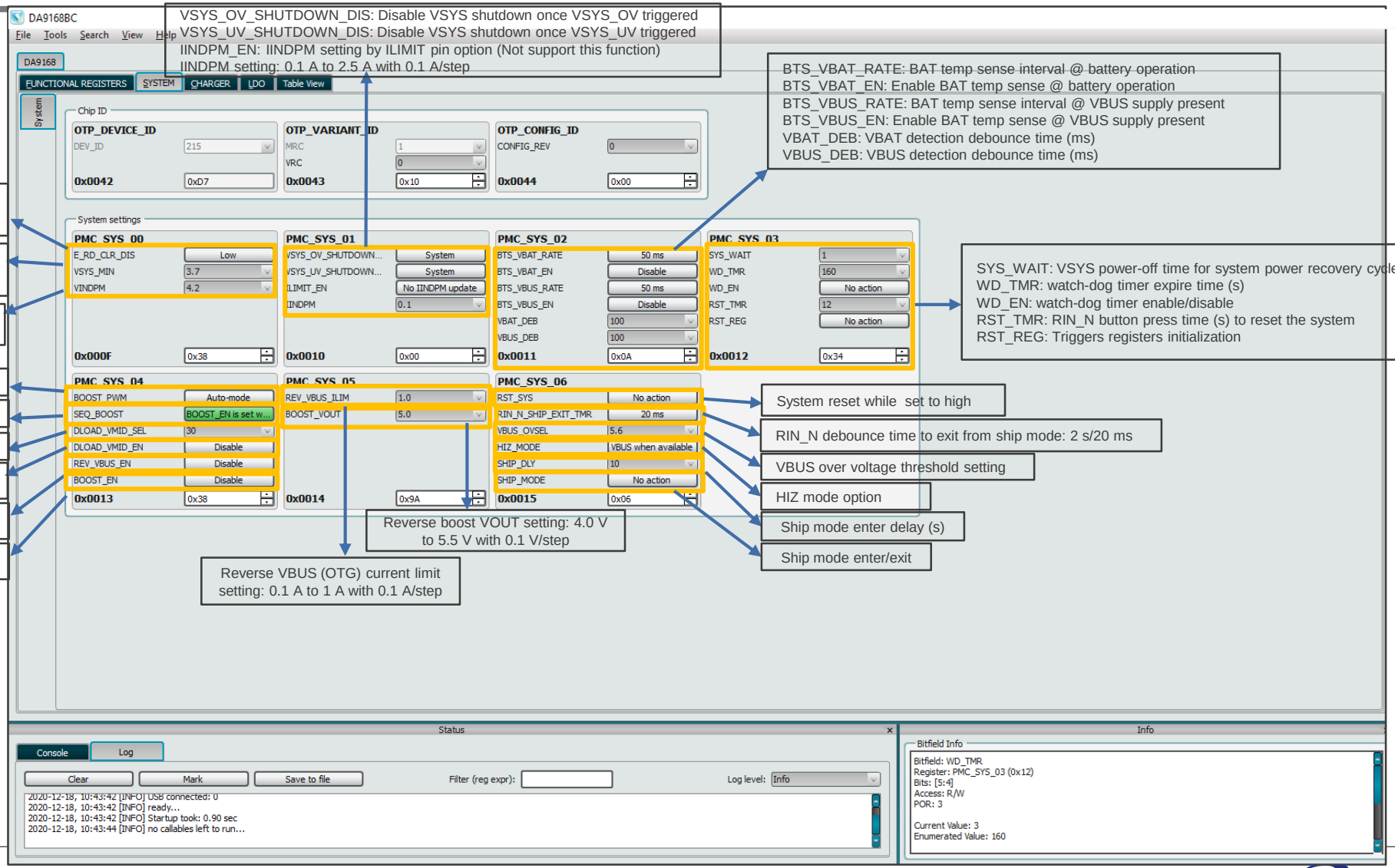


INT_N signal masked for all events (Default) which means INT_N no react while these events triggered.





SYSTEM REGISTERS



CHARGER REGISTERS

BC Silicon New option at charging mode:

Recharge voltage threshold offset setting
0: 100 mV; 1: 200 mV

Charger safety timer rate reduced to half while relevant events triggered.

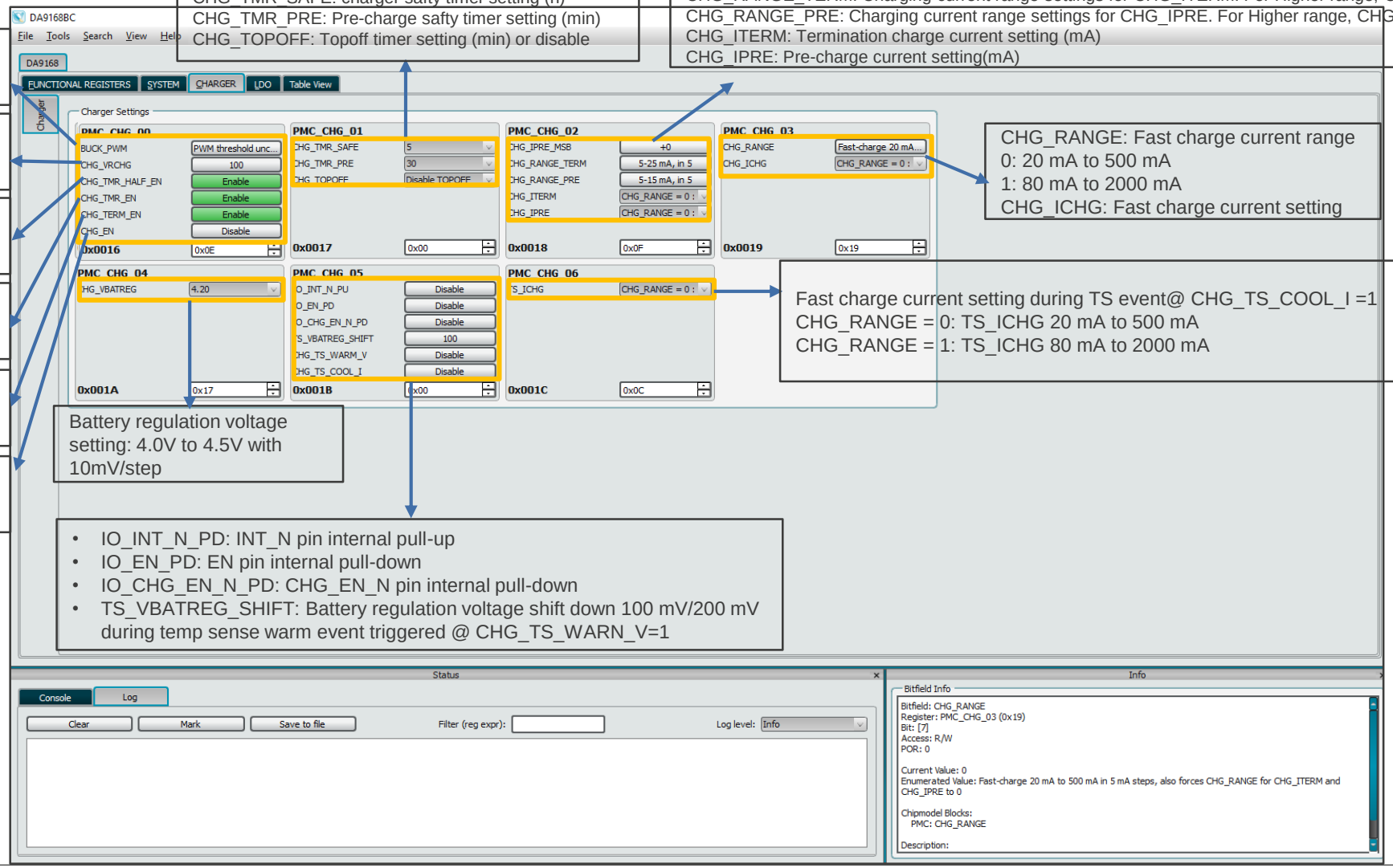
Charger safety timer enable/disable

Charger termination enable/disable

Charger enable/disable
(CHG_EN_N pin pulldown at the same time to enable charger)

CHG_TMR_SAFE: charger safty timer setting (h)
CHG_TMR_PRE: Pre-charge safty timer setting (min)
CHG_TOPOFF: Topoff timer setting (min) or disable

CHG_IPRE_MSB: Adds offset to pre-charge current setting (mA) while set to 1
CHG_RANGE_TERM: Charging current range settings for CHG_ITERM. For Higher range, CHG_RANGE need set to 1
CHG_RANGE_PRE: Charging current range settings for CHG_IPRE. For Higher range, CHG_RANGE need set to 1
CHG_ITERM: Termination charge current setting (mA)
CHG_IPRE: Pre-charge current setting(mA)



CHG_RANGE: Fast charge current range
0: 20 mA to 500 mA
1: 80 mA to 2000 mA
CHG_ICHG: Fast charge current setting

Fast charge current setting during TS event@ CHG_TS_COOL_I =1
CHG_RANGE = 0: TS_ICHG 20 mA to 500 mA
CHG_RANGE = 1: TS_ICHG 80 mA to 2000 mA

Battery regulation voltage setting: 4.0V to 4.5V with 10mV/step

- IO_INT_N_PD: INT_N pin internal pull-up
- IO_EN_PD: EN pin internal pull-down
- IO_CHG_EN_N_PD: CHG_EN_N pin internal pull-down
- TS_VBATREG_SHIFT: Battery regulation voltage shift down 100 mV/200 mV during temp sense warm event triggered @ CHG_TS_WARN_V=1

LDOS/LSWS REGISTERS

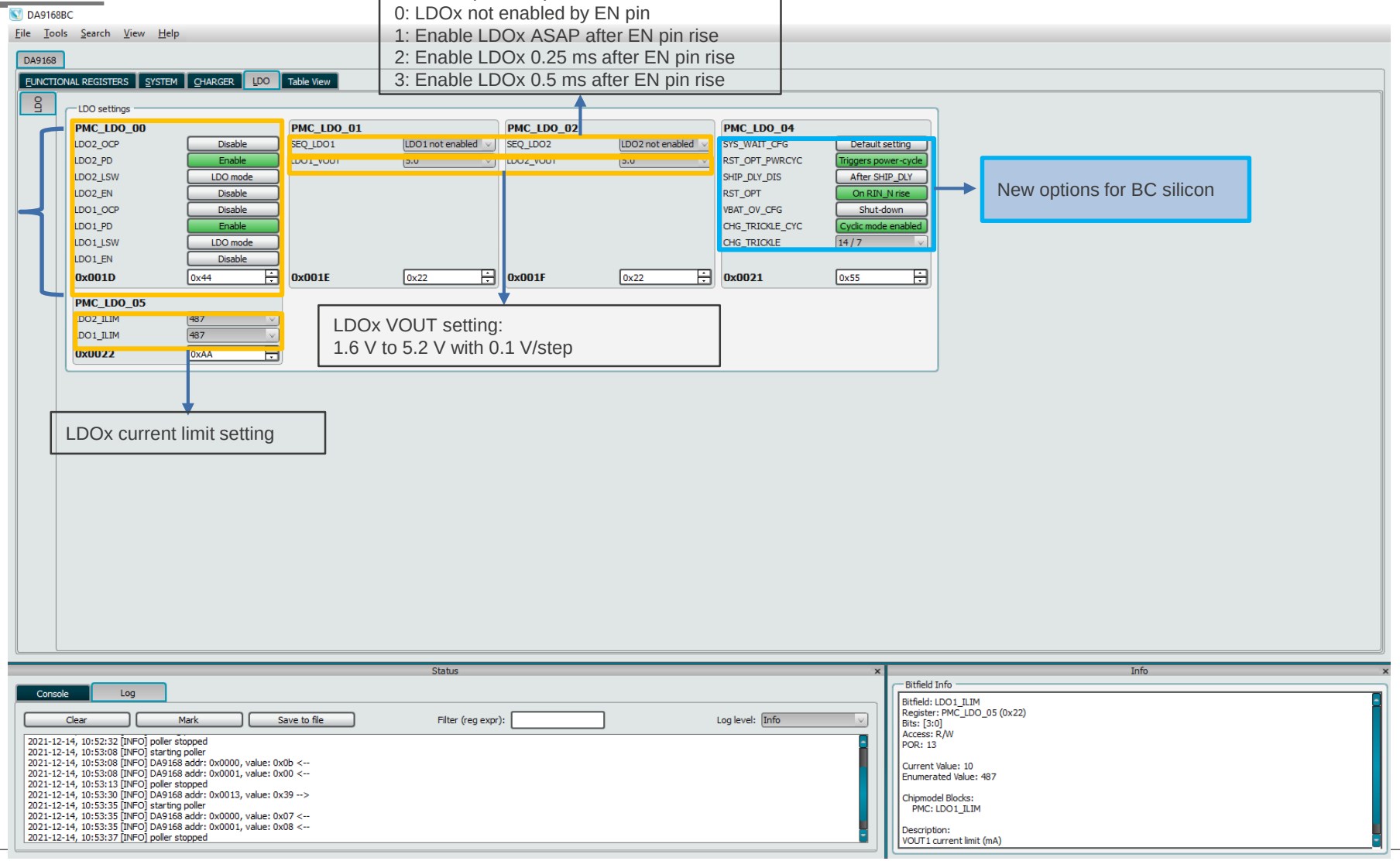
LDOx OCP option:
0: LDOx disable while trigger OCP
1: LDOx hiccup while trigger OCP

LDOx PD SW option:
0: LDOx PD switch disable
1: LDOx PD switch enable

LDOx_LSW mode option:
0: LDO mode
1: Load SW mode

LDOx_EN:
0: LDOx disable
1: LDOx enable

LDOx sequence option:
0: LDOx not enabled by EN pin
1: Enable LDOx ASAP after EN pin rise
2: Enable LDOx 0.25 ms after EN pin rise
3: Enable LDOx 0.5 ms after EN pin rise



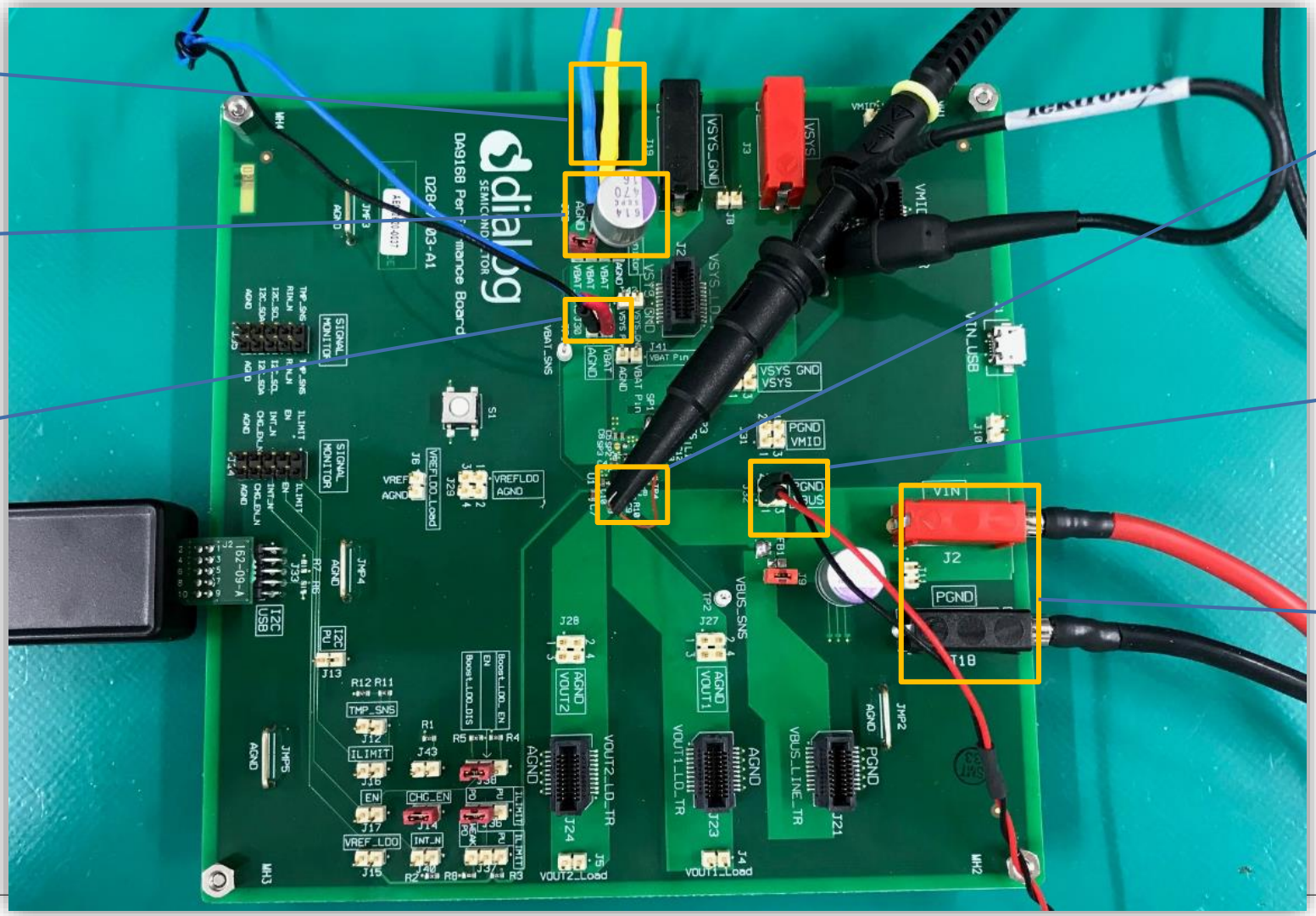
TEST BENCH SETUP

CHARGE MODE BOARD SETUP

VBAT Connection

Highly recommend:
Bulk electrolytic cap for VBAT connector to prevent VBAT voltage oscillation due to the long cable

VBAT Sense



VLX Signal

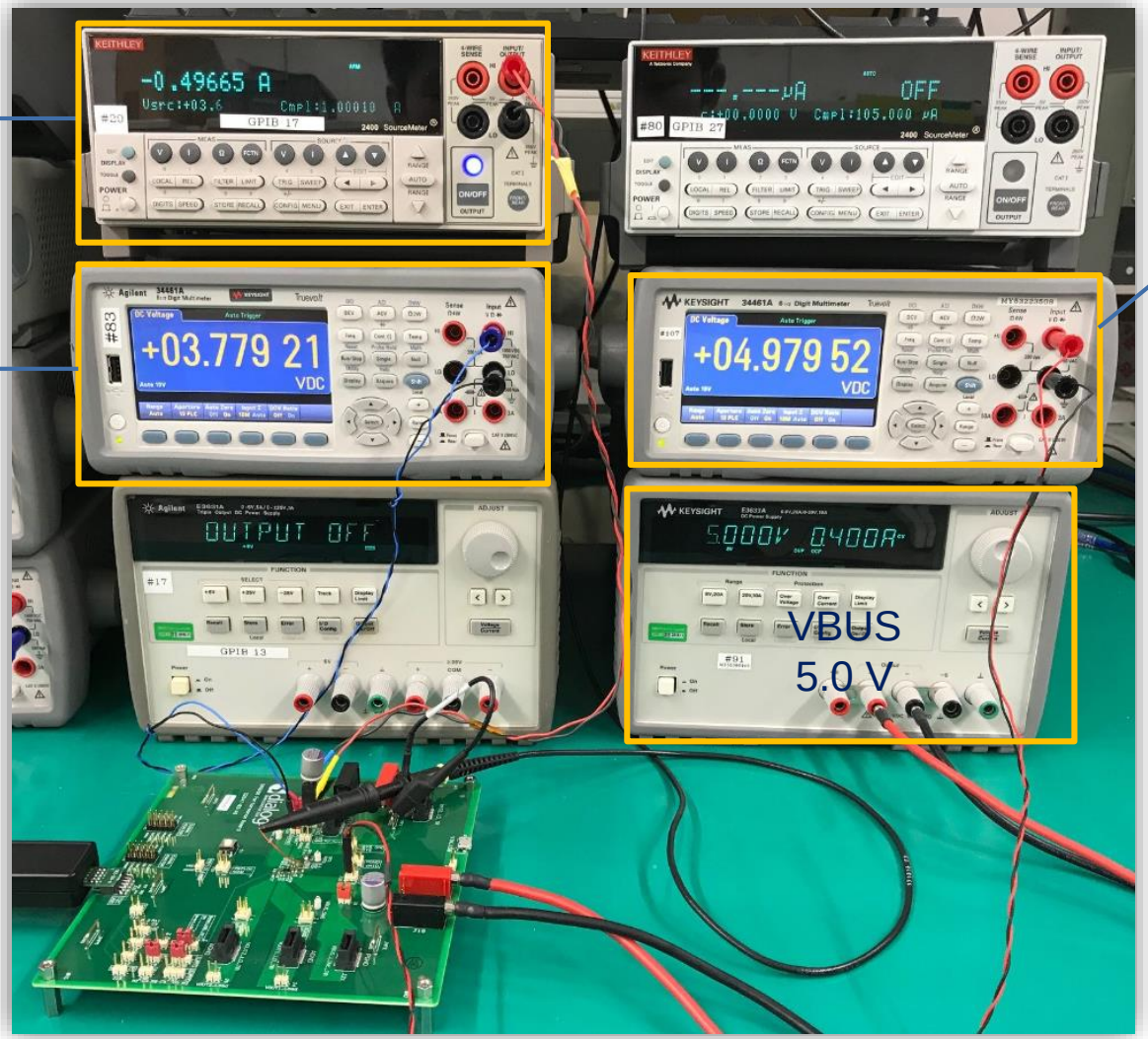
VBUS Sense

VBUS Connection

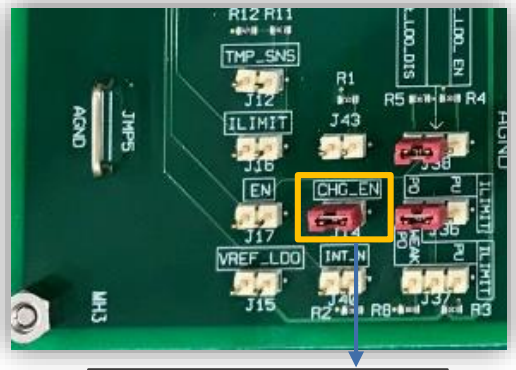
CHARGE MODE TEST BENCH SETUP

VBAT charging current

VBAT Sense 3.779 V



VBUS Sense 4.979 V



CHG_EN_N pin pulldown

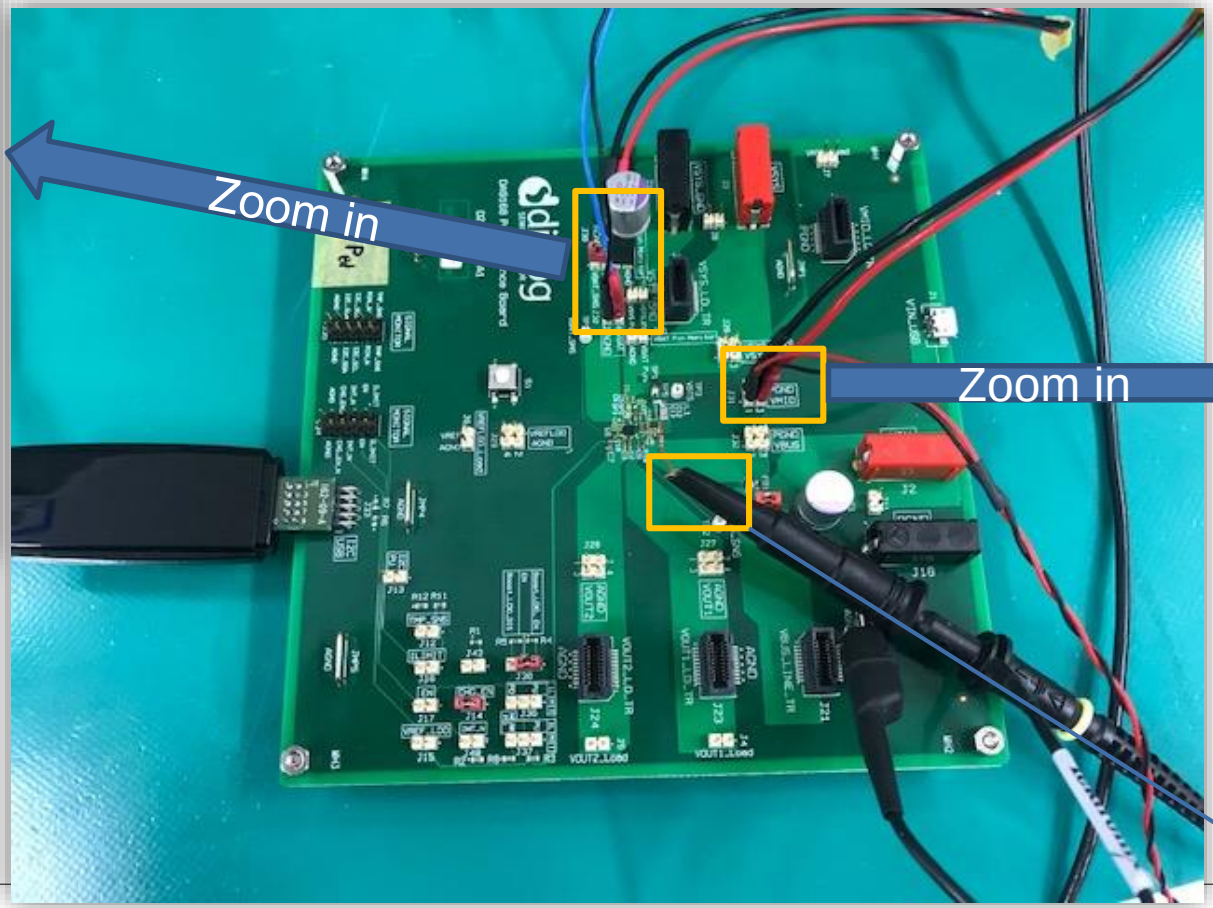
PMC_CHG_00	
BUCK_PWM	Auto-mode
CHG_VRCHG	100
CHG_TMR_HALF_EN	Enable
CHG_TMR_EN	Enable
CHG_TERM_EN	Enable
CHG_EN	Enable
0x0016	0x0F

CHG_EN set to High

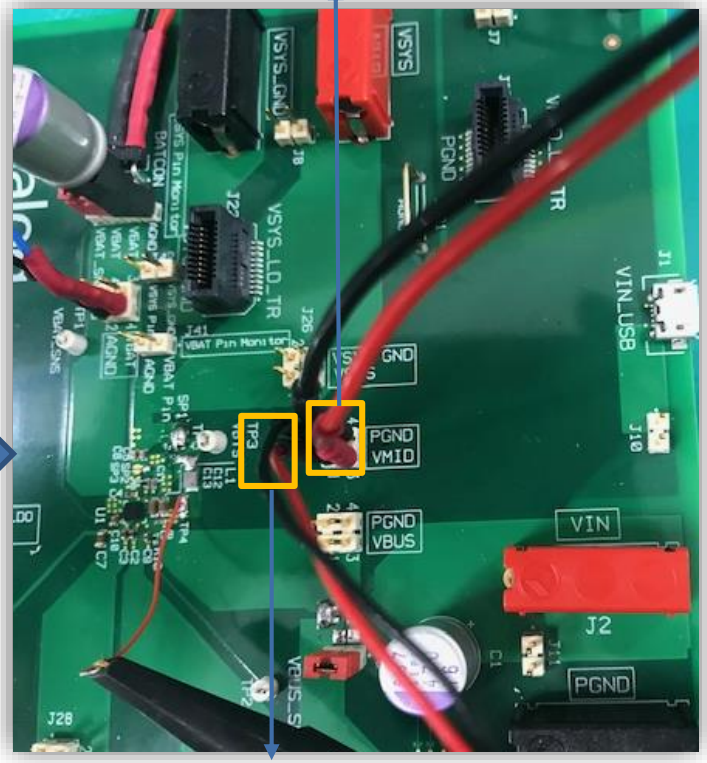
REV-BOOST MODE BOARD SETUP

VBAT Connection

VBAT Sense



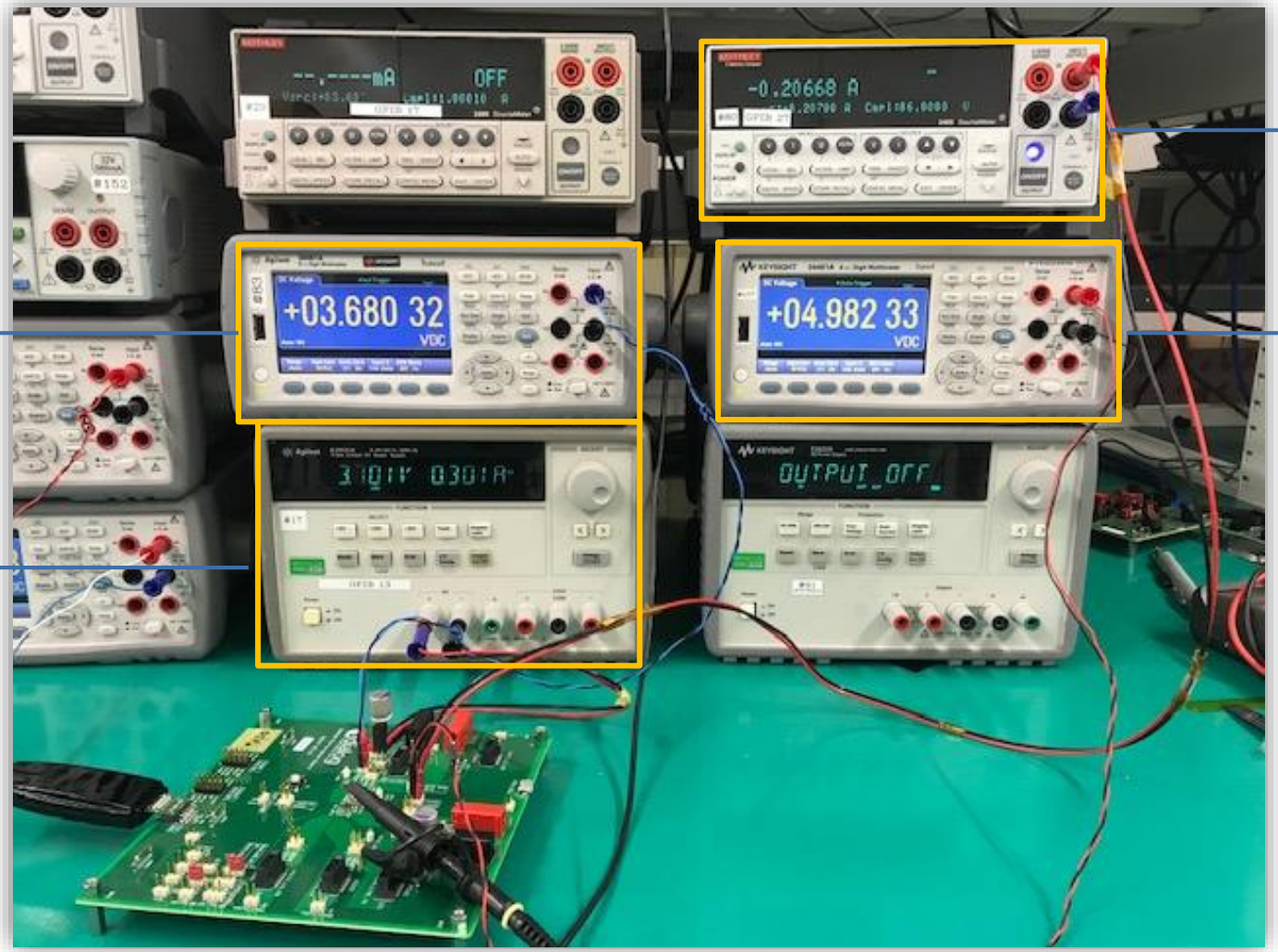
VMID Load



VMID Sense

LX Signal

REV-BOOST MODE TEST BENCH SETUP

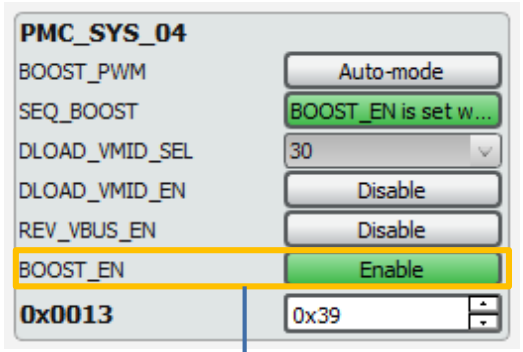


VMID Load
(200 mA)

VBAT
Sense
3.68 V

VMID Output
4.982 V

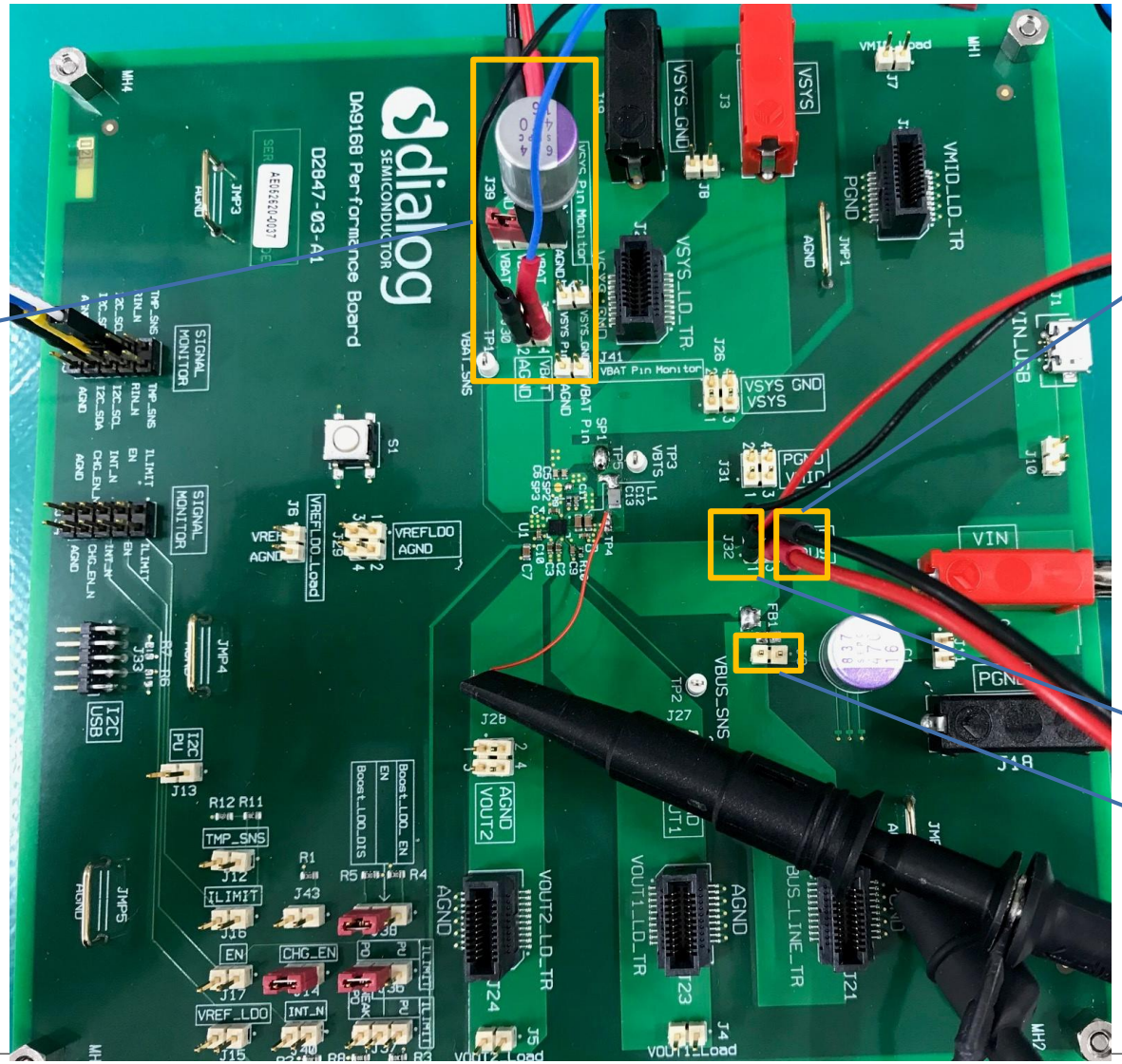
VBAT
3.7 V



BOOST_EN set to High

REV-VBUS (OTG) BOARD SETUP

VBAT and VBAT sense connections are same with Rev_boost setup

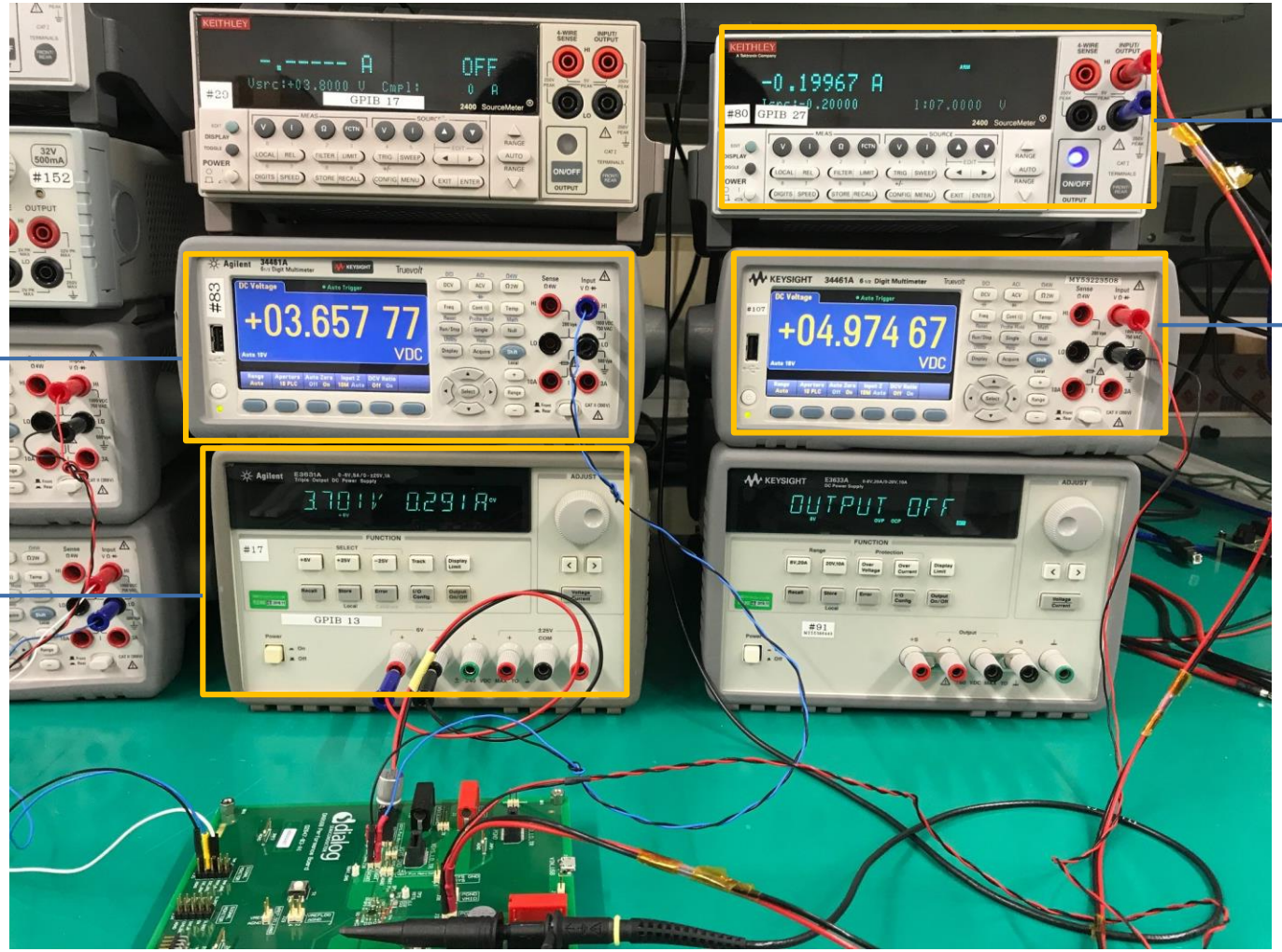


Rev-VBUS Load

Rev-VBUS Sense

Remove jumper J9

REV-VBUS (OTG) TEST BENCH SETUP

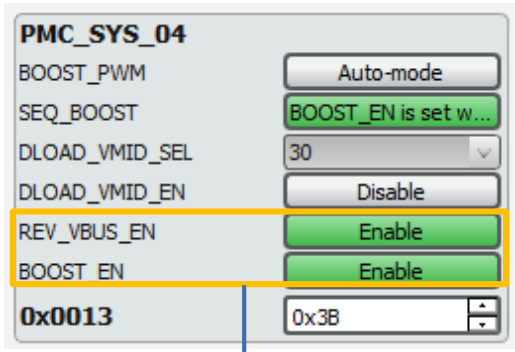


Rev-VBUS Load
(200 mA)

Rev-VBUS Output
4.974 V

VBAT
Sense
3.657 V

VBAT
3.7 V



REV_VBUS_EN set to
High
BOOST_EN set to High

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