Application note

DA9210-xxUK2 48-WLCSP PFM mode limitations

AN-PM-052

Abstract

This application note is related to DA9210-xxUK2 in 48-WLCSP package and explains some limitations of the buck converter when used in PFM and AUTO mode. The not expert user should consider reading only the relevant summary of chapter 4. Advanced users will more deeply understand some aspects of the design in the following chapters and how to prevent issues arising. Dedicated countermeasures will not limit the operability in most application use cases. They will be extensively explained in the following chapters.

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1 Terms and definitions

AP	Application Processor
CPU	Central Processing Unit
DDR	Double Data Rate SDRAM (Synchronous Dynamic Random Access Memory)
DVC	Dynamic Voltage Control
GPU	Graphic Processing Unit
IC	Integrated Circuit
OTP	One Time Programmable memory
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
POL	Point Of Load

2 References

1. DA9210-01 PDS1k, Data sheet, Dialog Semiconductor
2. AN-PM-039, DA9210 OTP variants

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3 Introduction

DA9210 is a multi-phase synchronous step down converter suitable for the supply of CPU in smartphones, tablets, ultra books and other handhelds applications, which require high currents to run the processor core.

DA9210 is designed to operate with 4 phases, each channel using a small external 0.47 µH inductor. The buck is capable of delivering up to 12 A continuous output current at an output voltage in the range 0.3 - 1.57 V. The input voltage range of 2.8 – 5.5 V makes it suited for a wide variety of low voltage systems, including all Li-Ion battery supplied applications.

The Buck converter can be forced to operate in either PMW mode, with selectable number of phases enabled, or in Low Power mode, where the efficiency is optimized for output currents lower than 1 A. In Low Power Mode the buck can be forced to operate in PFM Mode and frequency varying with the output load current. The configuration of the Low Power Mode is a programmed parameter and cannot be changed on a specific variant. Please contact your local Dialog Semiconductor support for more information. An automatic transition to PFM Mode (including also automatic phase shedding) can be configured via AUTO_DEF. When the bit is set, in addition to the phase shedding a PFM Mode operation is entered in case the output current load becomes low and the efficiency is maximized.

In PFM mode the output voltage is monitored and a PWM burst is generated when V_{OUT} drops below a certain low voltage threshold. The switching frequency is fixed during the PWM burst. The burst is stopped when the coil current is back to zero. Most of the internal circuits are off during the non-switching time, thereby optimizing the efficiency.

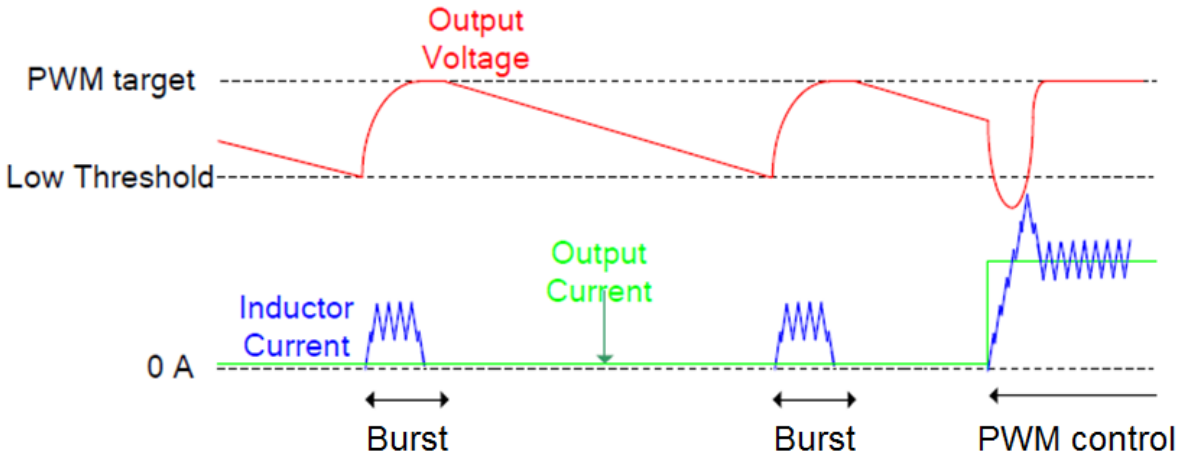

Figure 1: Principle of operation of the PFM mode in DA9210

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4 V_{OUT} spikes: summary

When DA9210's buck converter operates in PFM, or equivalently in AUTO mode at low load, a minimum load current of typically 2 mA must be guaranteed in static V_{OUT} conditions to achieve stability.

However during DVC transitions some voltage spikes are still possible and this application note will detail what happens in this case.

When the buck is turned off without a controlled ramped power down (PWR_DOWN_CTRL = 111) and then turned on again dynamically in a short time, some voltage spikes can be generated as well, so you should understand how to avoid them.

4.1 Conditions

a) Negative DVC in PFM mode. In this case the condition for V_{OUT} spikes to happen is a long no switching time, means the time between two consecutive bursts is too long (see Figure 1).

b) The buck is enabled and the output voltage was still floating close to the target level after the buck was disabled because the power down was not actively ramped by DA9210. This happens if you turn on the buck immediately after having turned it off.

4.2 Reasons

a) DA9210 design uses an integrated hold capacitor to keep the error amplifier output voltage during no switching period. This allows storing the status of the previous switching in PFM mode and is essential for the buck control unit. A long no switching period causes large voltage shift on the hold capacitor due to leakage current.

b) After being enabled, the buck converter will start switching when the output voltage is at least a few mV below the target level. When this threshold is reached and the target level is already higher, a high voltage difference is present at the inputs of the high gain error amplifier.

4.3 Symptom: V_{OUT} spike

a) A shifted voltage on the hold capacitor causes a switching re-start with very high duty cycle, next time a switching burst is needed during PFM mode (see Figure 1). For this reason spikes may happen at V_{OUT}.

b) A high voltage difference at the inputs of the high gain error amplifier cause an over-reaction of the compensation loop with over-shoot at V_{OUT}.

4.4 Work around

a) To avoid spikes at V_{OUT}, negative DVC transitions must be started in PWM mode. This can be achieved by using the voltage selection via VBUCK_SEL from VBUCK_A to VBUCK_B or vice versa. In fact you can associate a specific operating mode to VBUCK_A and VBUCK_B, for instance PWM mode if VBUCK_A is selected and PFM mode if VBUCK_B is selected. The way DA9210 operates the transition from VBUCK_A to VBUCK_B voltage is such that PWM is used during DVC, thereby there are no voltage spikes at V_{OUT}.

   Note that V_{OUT} spikes will never happen during positive DVC, that is when changing from a lower to a higher voltage, because in that case the PWM operation is always forced.

b) To avoid spikes at V_{OUT} during dynamic turn off/on of the buck converter, make sure that you actively ramp down the output voltage after turn off, i.e. that you have a value different from 111 in PWR_DOWN_CTRL. The suggested value on this register field is PWR_DOWN_CTRL = 011, equivalent to 10mV/µs.

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5 Negative DVC in PFM mode

When a negative DVC is operated starting from PFM mode, the target voltage is internally ramped down to the next value and the burst re-start threshold is ramped down too (see Target – 5 mV curve in Figure 2). Thus the V_{OUT} is above the re-start threshold for a long time, actually the time needed for the specific output load to discharge the output capacitor. This time increases with the size of the output capacitor and decreases at higher load levels.

A long non-switching period happens during negative DVC in PFM. This causes the internal hold capacitor of the error amplifier to discharge, so the next PWM burst starts with high duty cycle, whilst this shouldn't be the case as the V_{OUT} is only 5 mV away from the target. An over-shoot is determined by the over-reaction to a small voltage deviation.

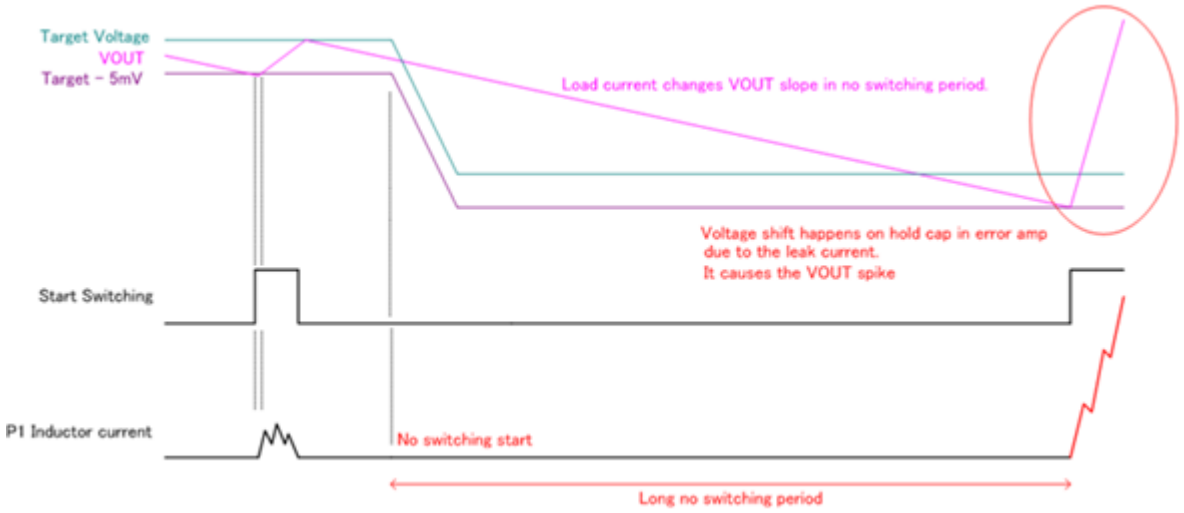

Figure 2: Negative DVC started from PFM mode

From the analysis of Figure 2 you can see that the output voltage is faster discharged to the next target value, if there's a load current applied at the output node. In fact, if the load is high enough, the internal hold capacitor of the error amplifier will not be discharged significantly, so there will be no over-shoot at the output and no work around required as in chapter 4.4.

The minimum load required to avoid over-shoots depends on different specific application details: the initial and final values of the DVC voltages, the size of the output capacitor, the temperature, the specific sample under test, etc. Higher DVC delta voltages require a higher load. Similarly, bigger output capacitors require a higher load to avoid over-shoots.

For instance, if you have V_{BAT} = 3.8 V, C_{OUT} = 4x 47 µF + 2x 22 µF + 2x 10 µF, and you decrease the V_{OUT} from 1.1 V to 0.7 V, the minimum load current required to avoid over-shoot is 5.9 mA. See also the table below for an overview of the results at different temperatures and on different corner lot samples. Consider that a minimum load represents an additional performance loss, if this load has to be introduced only to solve the over-shoot issue. So in general it's preferable to select the work around introduced in chapter 4.4.

Temp (°C)	FF Iout min (mA)	FS Iout min (mA)	SF Iout min (mA)	SS Iout min (mA)	STD Iout min (mA)
-20	3,6	1,8	2,4	5,3	2,7
0	3,9	1,9	2,5	5,7	2,9
25	4,2	2,2	2,7	5,9	3,1
45	4,5	2,3	2,9	2	3,4
65	4,8	1	3,3	1,5	3,4
85	1	1	3,4	1	1

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6 Negative DVC in PWM mode

When a negative DVC is operated starting from PWM mode, there's no V_{OUT} spike because during the ramp down DA9210 is still in PWM mode and there's no internal node to hold or subject to leakage. After the DVC transition, the buck can operate seamless in PWM or PFM mode.

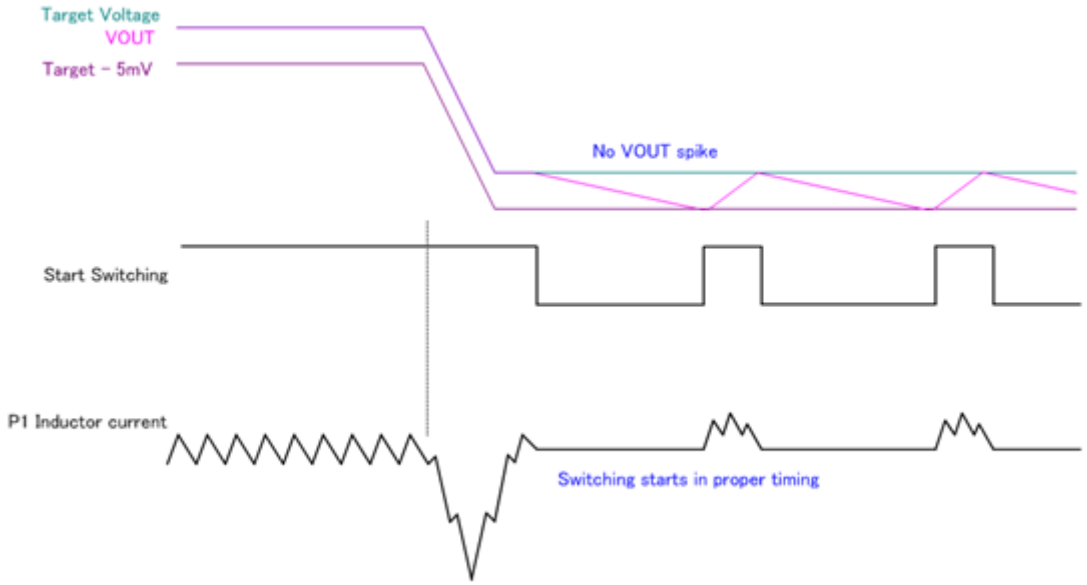

Figure 3: Negative DVC started from PWM mode

7 Positive DVC

Positive DVC transitions never show issues, because the switching starts with the proper timing, so positive DVC always happens in PWM mode, even if the buck is forced to operate in PFM mode. There's no internal node to hold or subject to leakage.

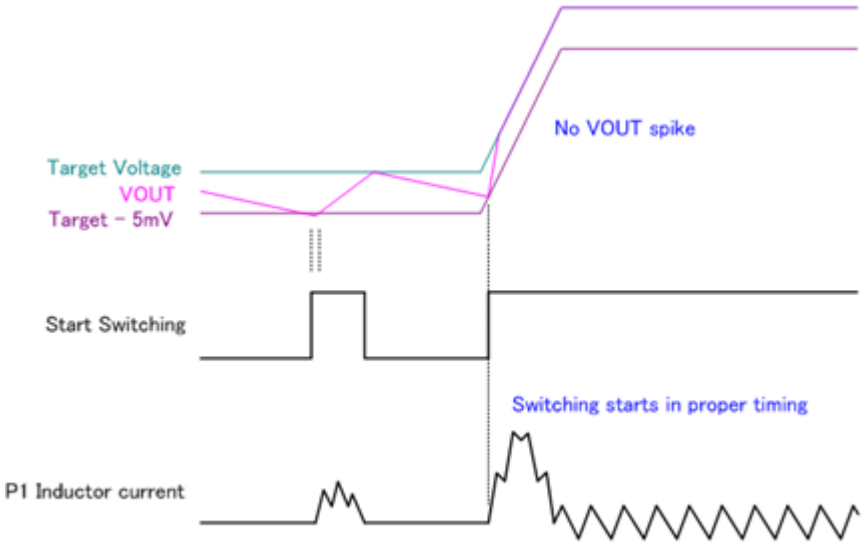

Figure 4: Positive DVC

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8 Dynamic buck off/on with PD_DIS = 1

When the buck is disabled and then enabled again dynamically in a short time, a V_{OUT} spike is generated if there's no pull down active at the output and there's no ramped power down (PWR_DOWN_CTRL = 111).

In order for the switching to re-start, the output node must be discharged 5 mV below the target voltage. If there's no active discharge for the output capacitor, the discharge can take a long time, because the output node is floating with high impedance.

When the buck converter is enabled again in a short time, the target voltage is ramped up according to the setting in STARTUP_CTRL and the final value is reached before the output node has been discharged by 5 mV.

So when the PWM switching starts again the high gain error amplifier has a high voltage delta at its inputs and over-reacts creating an over-shoot.

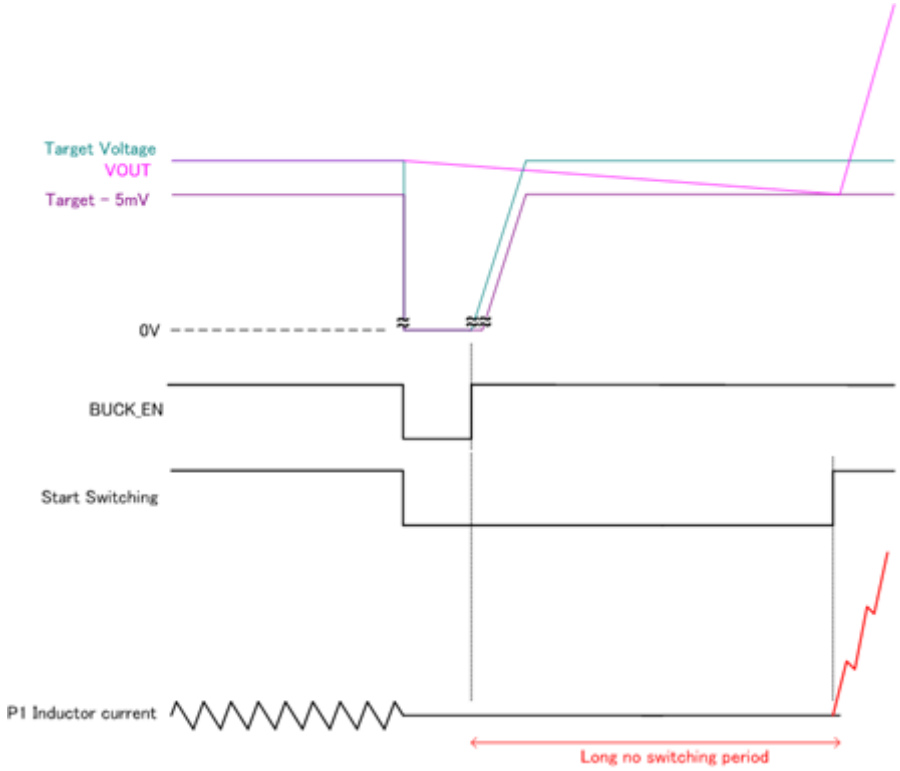

Figure 5: Buck dynamically re-enabled with PD_DIS = 1 and no ramped power down

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9 Dynamic buck off/on with PD_DIS = 0

When the buck is disabled without ramped power down (PWR_DOWN_CTRL = 111) and then dynamically enabled again in a short time, with a pull down active at the output, there are two different scenarios.

If the off time was long enough to discharge the output node through the pull down resistor, there's no spike at V_{OUT} (see Figure 6).

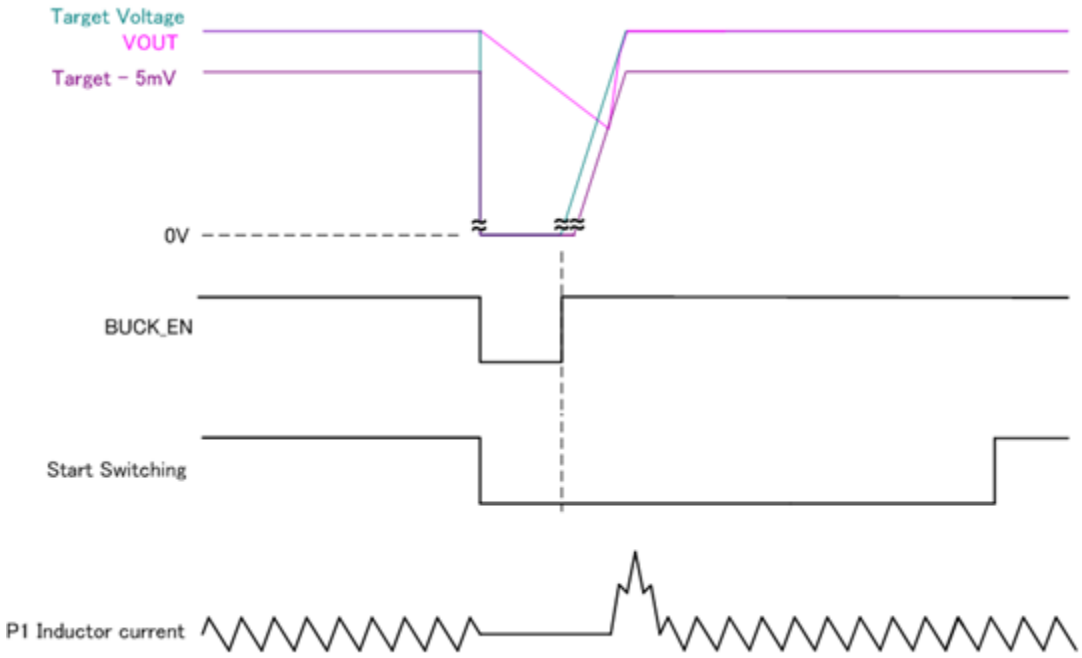

Figure 6: No spike with PD_DIS = 0 and no ramped power down

However, if the off time was extremely short (e.g. few µs), a similar situation as with PD_DIS = 1 may still occur (see Figure 7)

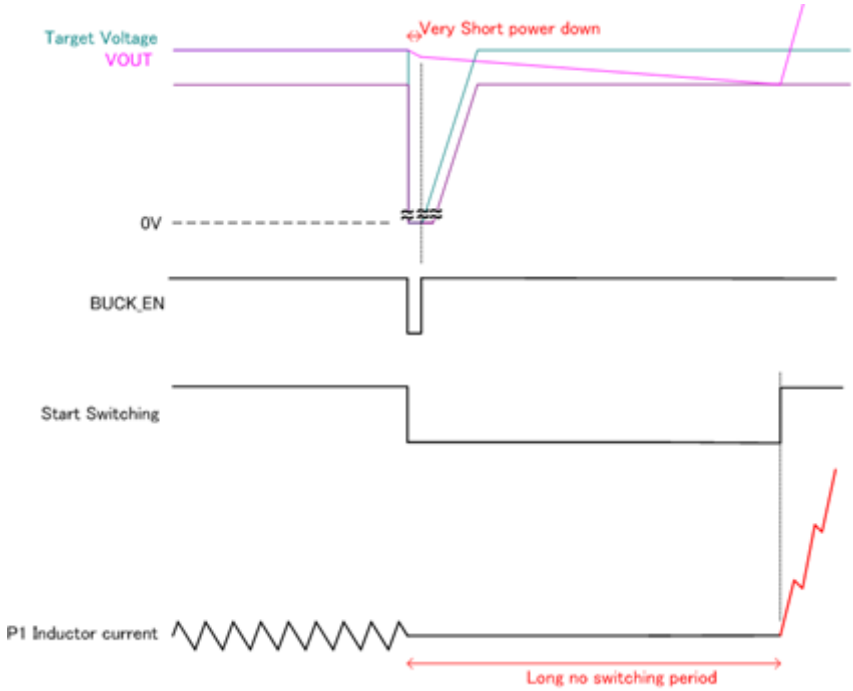

Figure 7: Spike with PD_DIS = 0 and no ramped power down

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10 Dynamic buck off/on with ramped power down

It turns out that the safest setting is the ramped setting for the power down, that is a value different from 111 in PWR_DOWN_CTRL. The suggested value on this register field is PWR_DOWN_CTRL = 011, equivalent to 10mV/µs.

You may even win efficiency in your whole application if you configure a ramped power down, because you pump back the energy from the output to the input instead of wasting it through a passive pull down.

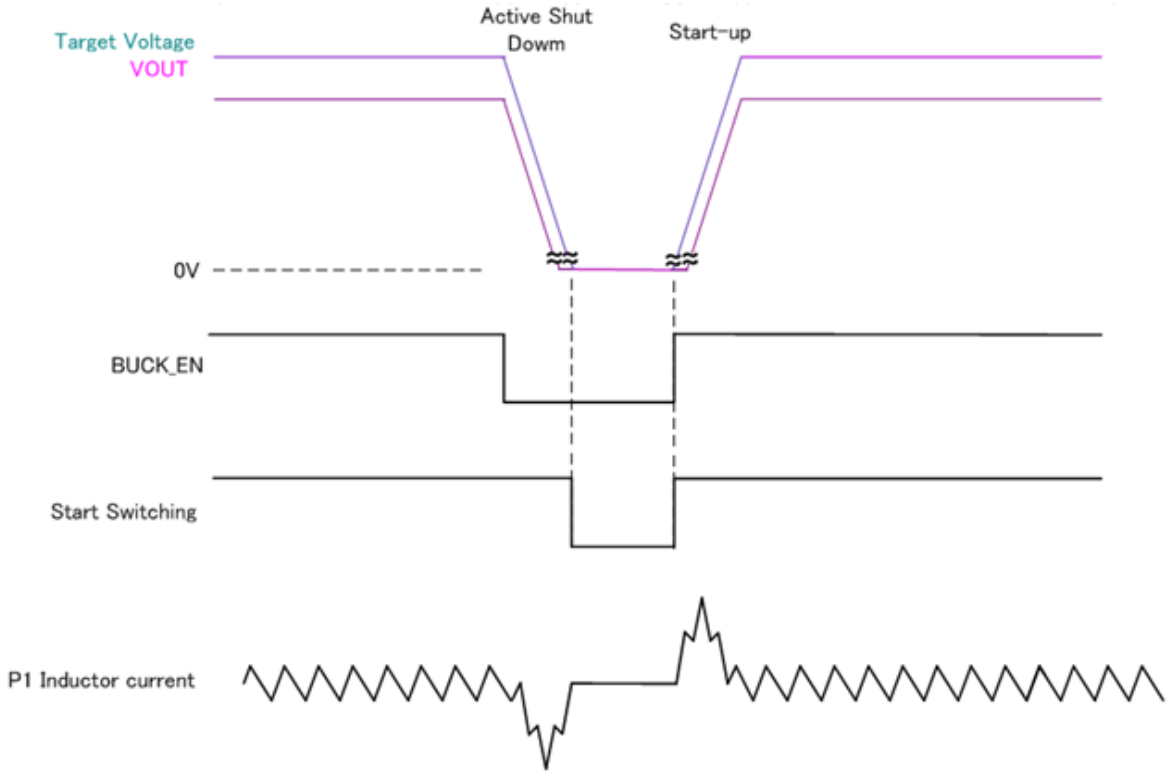

Figure 8: No spike with ramped power down

There's no issue in re-starting the buck converter even in the middle of a power down sequence, because the buck converter re-starts immediately.

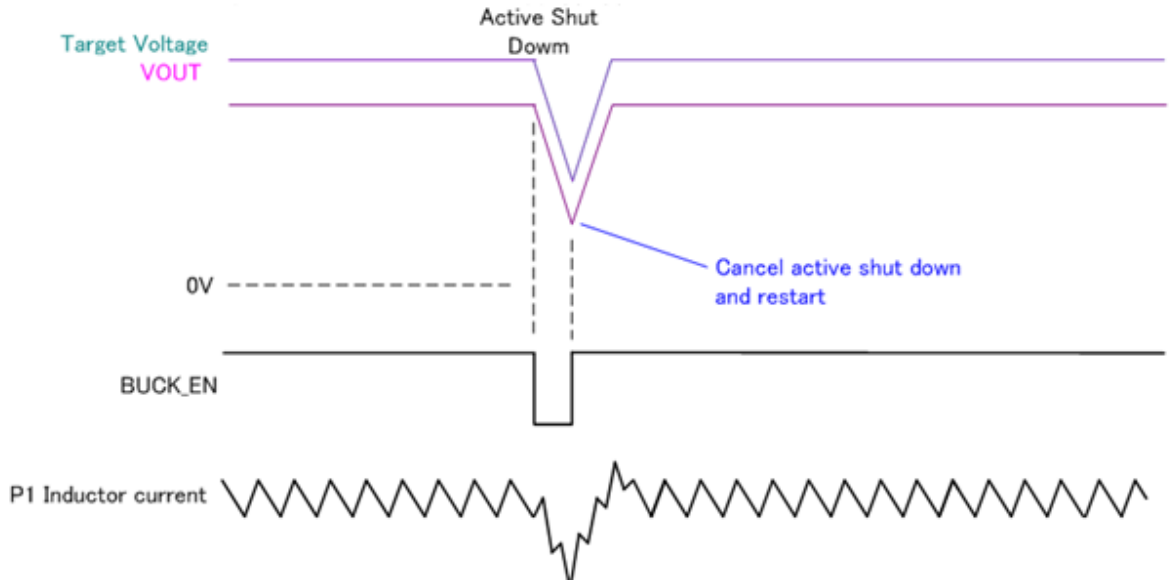

Figure 9: Re-start during a ramped power down

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11 Conclusions

An over shoot issue in PFM mode during DVC has been presented here for DA9210-xxUK2, 48-WLCSP. The conditions when the over shoot happens have been detailed, as well as the reason and easy work arounds.

If you need more information do not hesitate to contact your local Dialog Semiconductor support.

12 Revision history

Revision	Date	Description
1.0	05-Dec-2014	Initial version
1.1	17-Dec-2014	Updated chapter 4: summary Updated chapter 9 Added chapter 10

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