

F1485 – Multi-Carriers with Wider IBW

This document provides information for the F1485 under the operation of multi-carrier signals with instantaneous bandwidths (IBW) of up to 400MHz at the 3300MHz to 4200MHz frequency range. Within this document are the updated BOM table, measured ACLR with DPD performance at $f_0 = 3.55\text{GHz}$ for 1-Carrier-100MHz signal, 2-Carrier-100MHz signal with IBW = 200MHz and 400MHz, and the RF performance plots with the updated BOM.

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1. Introduction

In 5G wireless communication systems, wider radio instantaneous bandwidth (IBW) allows for more efficient use of available spectrum. Higher bandwidth allows for faster data transfer and increased capacity. Taking the 5G 3.6GHz frequency band as an example, the IBW has increased from 100MHz to 200MHz, and now up to 400MHz. Driven by the increase in IBW requirements, the F1485 Evaluation Kit BOM is optimized for better ACLR with DPD performance for 2-Carrier-100MHz with IBW = 200MHz and 400MHz. The updated BOM significantly improves the Video Bandwidth of the F1485 resulting in enhanced ACLR with DPD performance for high IBW signals.

2. Measured ACLR Results

Table 1 shows the measured ACLR with DPD performance for 1-Carrier-100MHz and 2-Carrier-100MHz with IBW = 200MHz and 400MHz.

Table 1. Measured ACLR Results of F1485 MB with Optimized BOM

BOM	Signal case	Pout (dBm)	ACLR with DPD ^[1]		ACLR without DPD	
			ACLR_L (dBc)	ACLR_R (dBc)	ACLR_L (dBc)	ACLR_R (dBc)
F1485 Optimized BOM in Table 2	f ₀ = 3.55GHz, 1C-100MHz, IBW = 100MHz, PAR = 8dB	15	-63	-63	-43.2	-38.6
	f ₀ = 3.55GHz, 2C-100MHz IBW = 200MHz, PAR = 8dB	15	-59.5	-59.1	-38.9	-37.8
	f ₀ = 3.55GHz, 2C-100MHz IBW = 400MHz, PAR = 8dB	15	-56.2	-57.8	-37.9	-41.3

1. ACLR with DPD is tested with AMD ZCU208 platform. ACLR values may vary with different DPD algorithms and test setup.

Figure 1 and Figure 2 show the ACLR at $f_0 = 3.55\text{GHz}$ for 2-Carrier-100MHz with IBW = 200MHz and 400MHz, respectively.

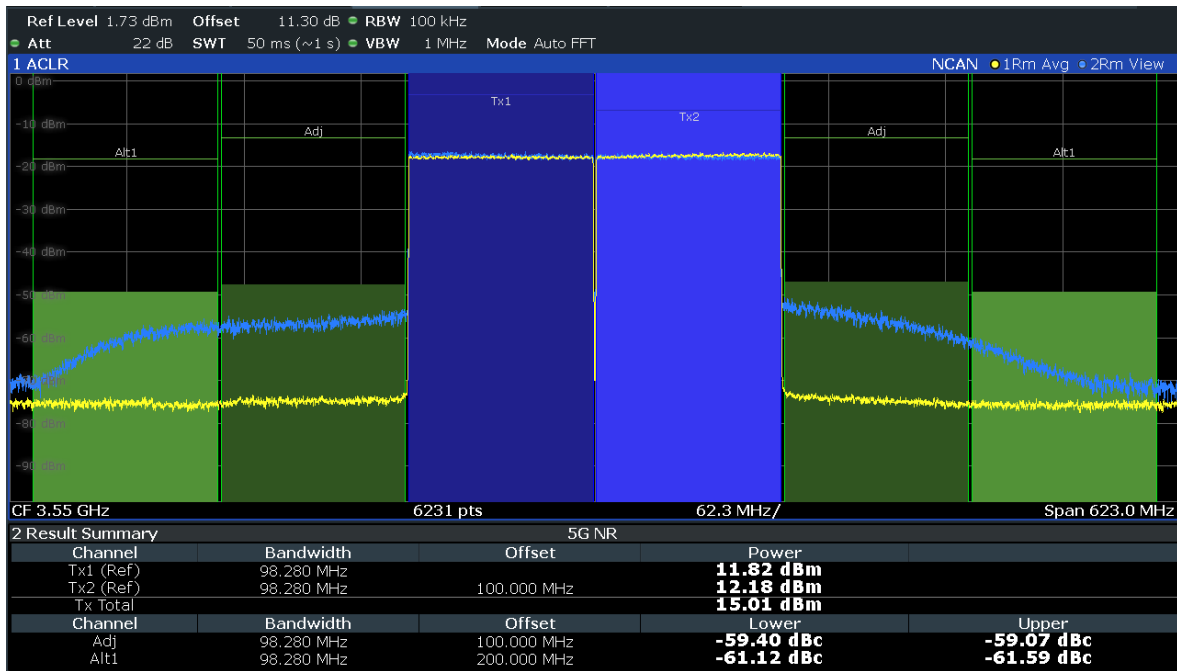


Figure 1. ACLR of F1485 MB with Optimized BOM ($f_0 = 3.55\text{GHz}$, 2C-100MHz, IBW = 200MHz)

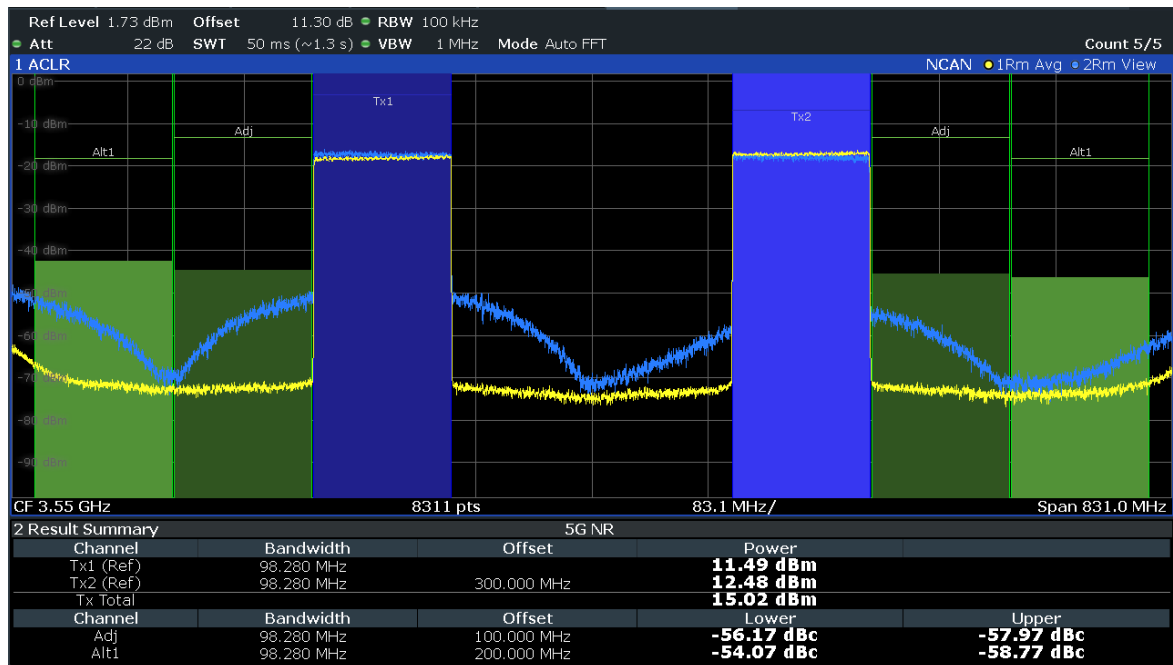


Figure 2. ACLR of F1485 MB with Optimized BOM ($f_0 = 3.55\text{GHz}$, 2C-100MHz, IBW = 400MHz)

3. Evaluation Kit Schematic

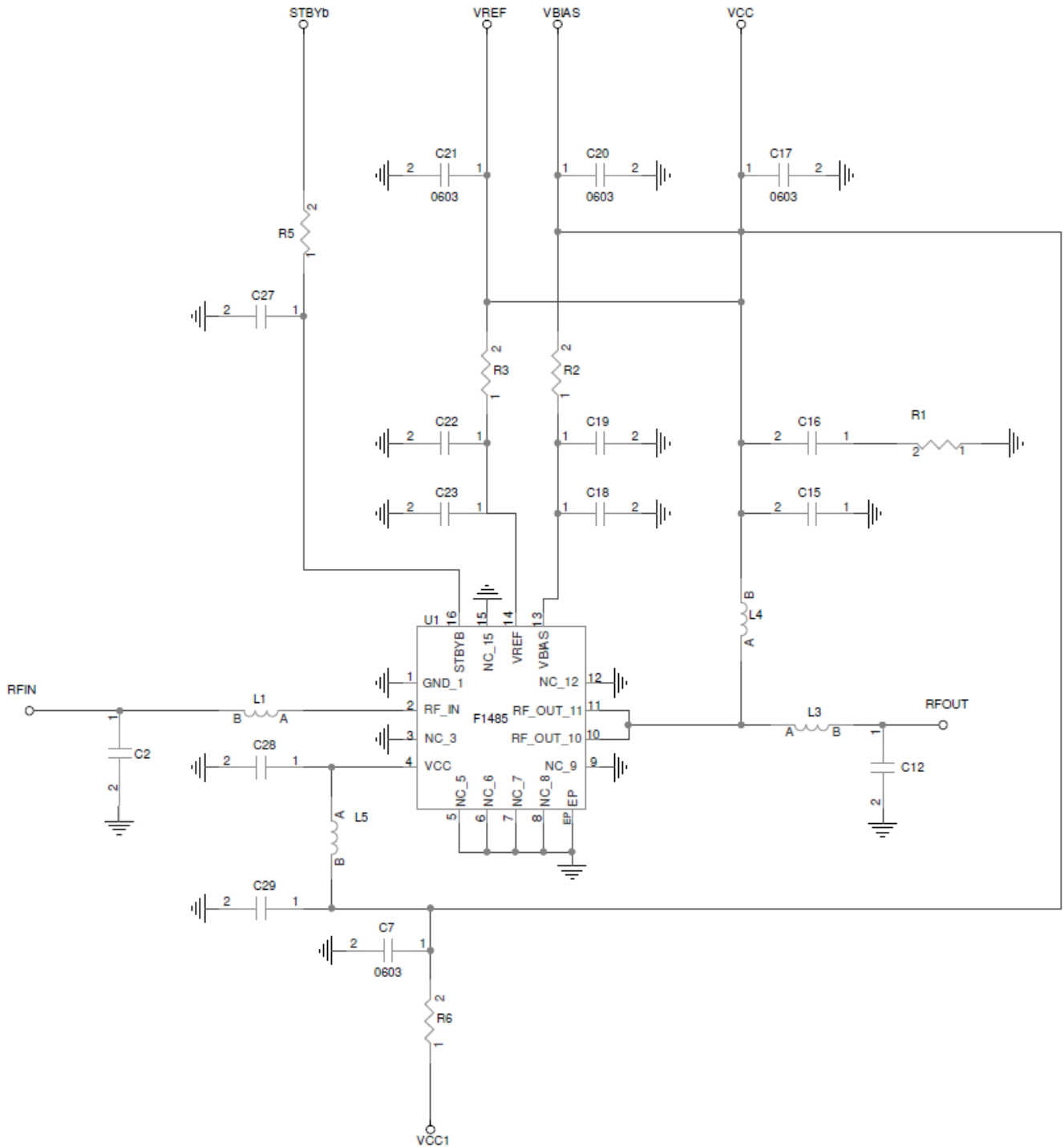


Figure 3. Application Circuit Electrical Schematic

4. Bill of Materials

Table 2. Application Circuit Bill of Material (BOM) for VBW Enhancement

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C7, C20, C21	3	47 μ F \pm 20%, 6.3V, X5R Ceramic Capacitor (0603)	GRM188R60J476ME15D	MURATA
C15	1	15pF \pm 5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H150JA	MURATA
C29	1	100pF \pm 5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101JA	MURATA
C16	1	10 μ F \pm 10%, 10V, X7R Ceramic Capacitor (0603)	GRM188Z71A106MA73	MURATA
C18, C19, C22, C23, C27, C17	6	DNP	-	-
C28	1	1 μ F \pm 10%, 16V, X6S Ceramic Capacitor (0402)	GRM155C81C105KE11	MURATA
C2	1	18nH Chip Inductor (0402)	LQP15MN18NG02D	MURATA
C12	1	1.2pF \pm 0.1pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H1R2WA	MURATA
L3	1	5.1pF \pm 0.1pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H5R1WA	MURATA
L4	1	2.2nH \pm 0.3nH, 300mA Chip Inductor (0402)	L-07C2N2SV6S	JOHANSON
L1, L5, R1, R2, R5, R6, R8	7	0 Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
R3	1	69.8 Ω \pm 1%, 1/10W, Resistor (0402)	ERJ-2RKF69R8X	PANASONIC
Module	1	F1485	-	Renesas

5. Measured RF Performance with Updated BOM

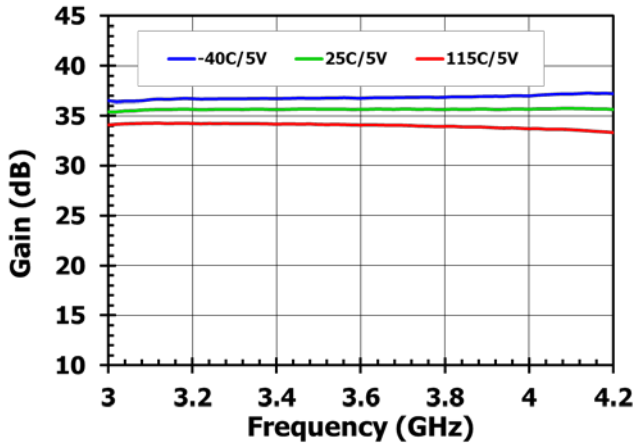


Figure 4. Gain

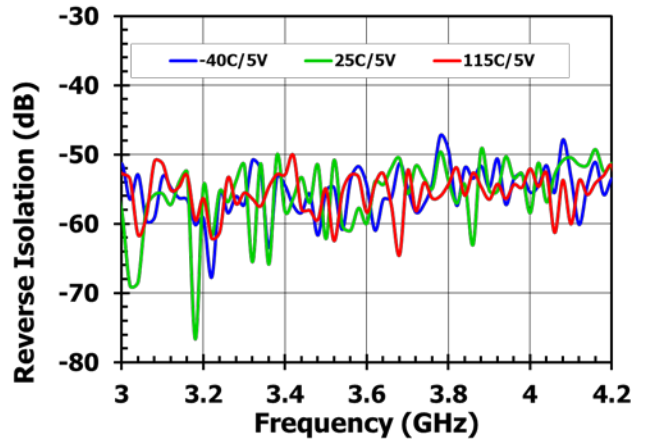


Figure 5. Reverse Isolation

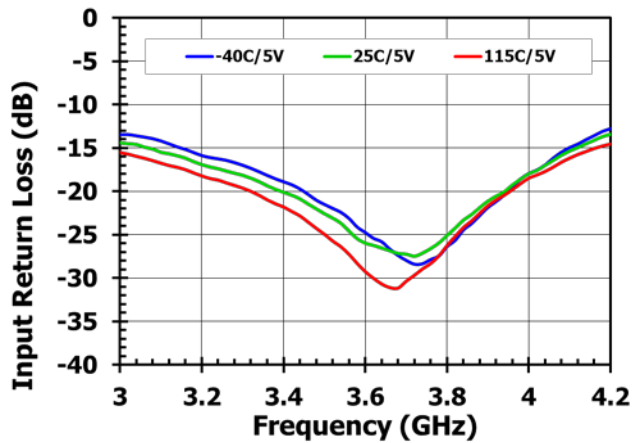


Figure 6. Input Return Loss

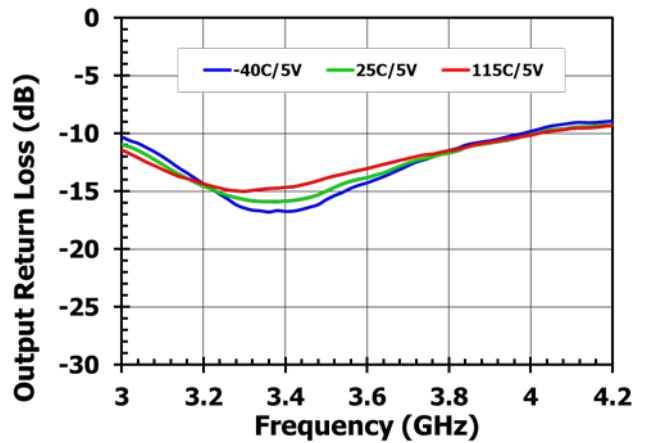


Figure 7. Output Return Loss

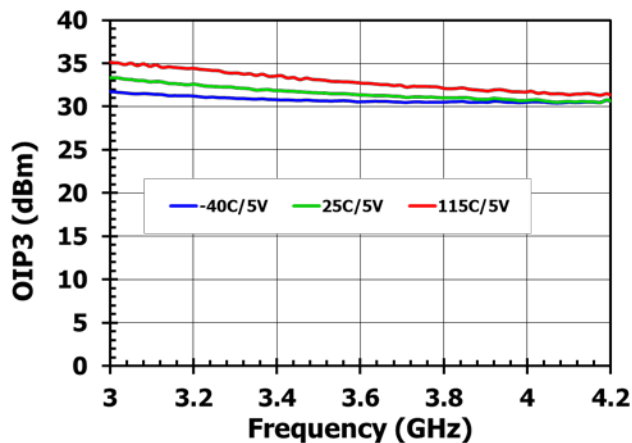


Figure 8. OIP3

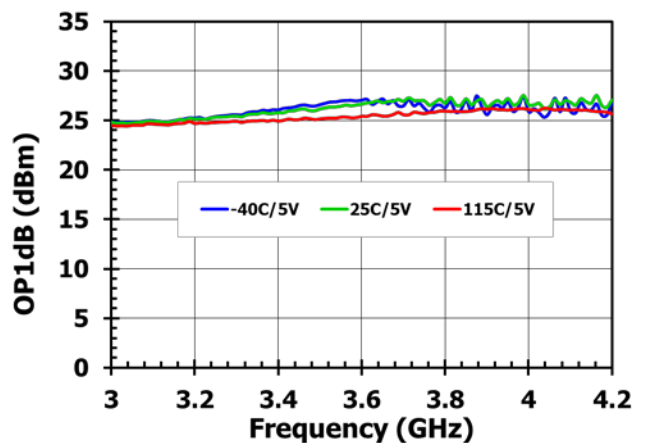


Figure 9. OP1dB

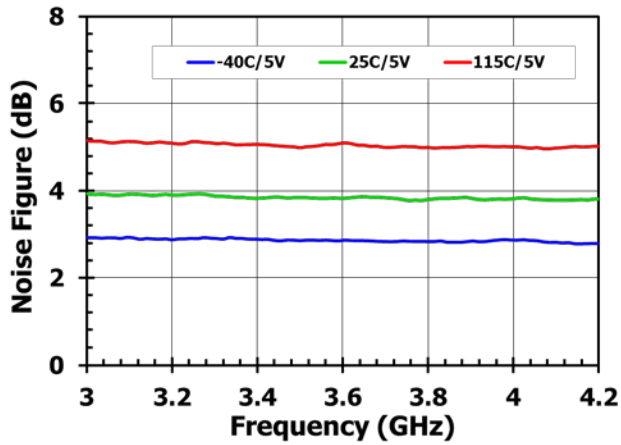


Figure 10. Noise Figure

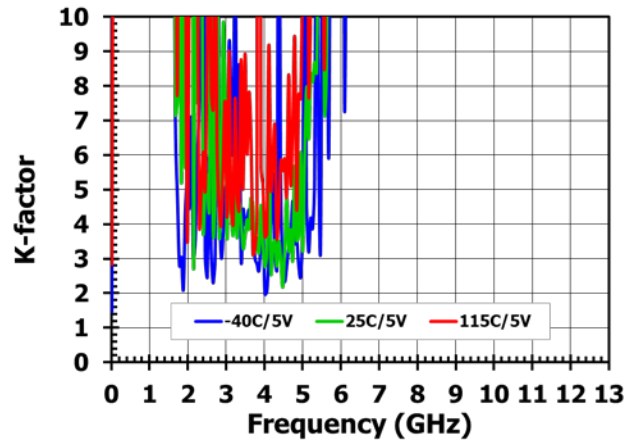


Figure 11. K-factor

6. Revision History

Revision	Date	Description
1.00	Aug 11, 2023	Initial release.

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