ISL73041SEH, ISL71441M

iSim:PE Model vs Silicon Application Report

Abstract

The ISL73041SEH (radiation hardened) and ISL71441M (radiation tolerant) PWM input 12V Half Bridge GaN FET Drivers are designed to drive low $r_{DS(ON)}$ Gallium Nitride FETs (GaN FET) for DC/DC switching regulators. An integrated programmable GaN FET gate drive voltage, high-side bootstrap switch, and strong gate drive current provide a compact and robust GaN FET half-bridge driver.

The iSim:PE model for the ISL73041SEH and ISL71441M was developed to help system designers evaluate the operation of this IC in a simulation environment before or in conjunction with proto-typing a system design. This model simulates typical performance characteristics such as PWM propagation/dead time delay, gate drive rise/fall time, power-up sequencing, and various DC thresholds at room temperature (T = 25°C).

Contents

List of Figures

1. License Statement

The information in this macro-model is protected under the United States copyright laws. Renesas Corporation hereby grants users of this macro-model, hereto referred to as Licensee, a nonexclusive, nontransferable license to use this model as long as the Licensee abides by the terms of this agreement. Before using this macro-model, the Licensee should read this license. If the Licensee does not accept these terms, permission to use the model is not granted.

The Licensee may not sell, loan, rent, or license the macro-model, in whole, in part, or in modified form, to anyone outside the Licensee's company. The Licensee may modify the macro-model to suit his/her specific applications, and the Licensee may make copies of this macro-model for use within their company only.

This macro-model is provided “AS IS, WHERE IS AND WITH NO WARRANTY OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.”

In no event will Renesas be liable for special, collateral, incidental, or consequential damages in connection with or arising out of the use of this macro-model. Renesas reserves the right to make changes to the product and the macro-model without prior notice.

2. Model Revision

At the date of this application report being published, the latest ISL73041SEH/ISL71441M iSIM:PE model revision is Version 1.0 (04/23/2023). For simulation accuracy, download the latest model at the ISL73041SEH/ISL71441M Model download page.

3. Schematic File

The schematic file (RENESAS_ae_ISL73041SEH_Switching.wxsch) is the main application schematic that should be used in the iSim:PE simulator. The schematic is set up with the driver, half bridge FETs, output inductor and capacitor for a Synchronous Buck DC/DC converter. Figure 2 through Figure 31 compare the simulation results for specified operating conditions versus the actual bench validation data. For more information on iSim: PE, visit the iSim on-line home page.

4. Simulation Schematic

Figure 1 is the base ISL73041SEH iSim:PE model schematic.

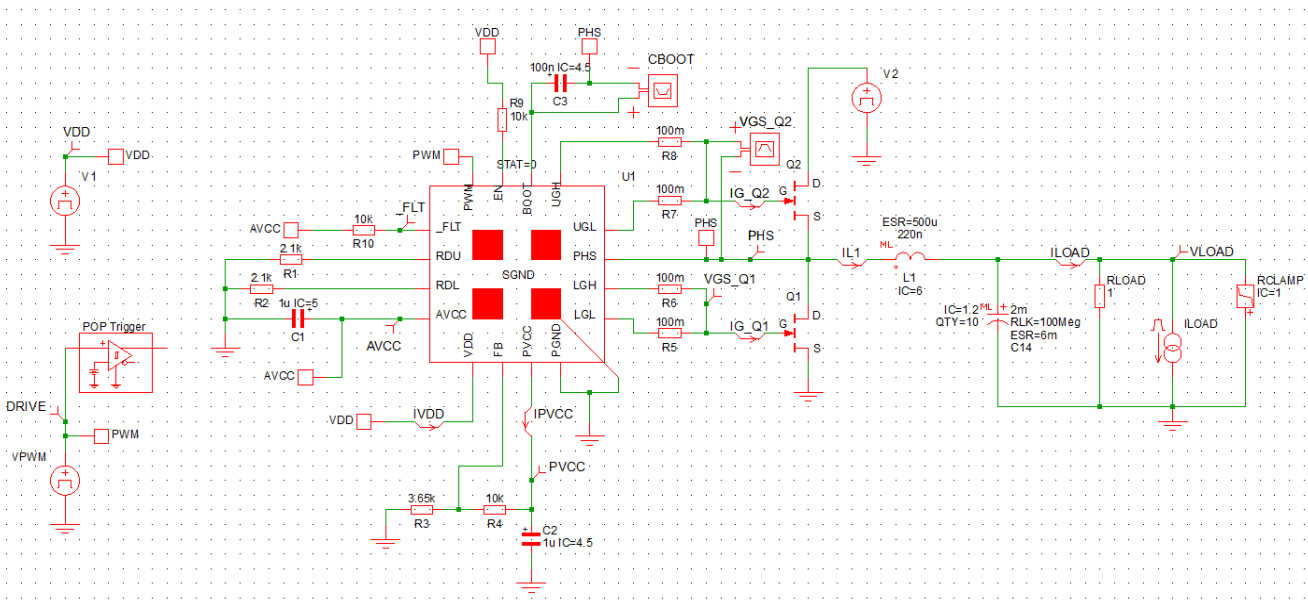

Figure 1. Base ISL73041SEH iSim:PE Model Schematic

5. Silicon vs Simulation Performance Curves

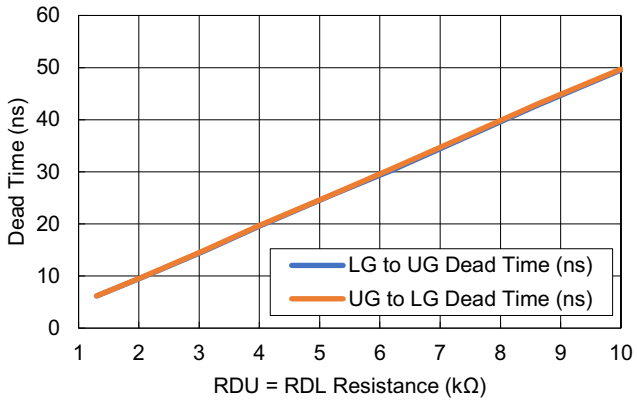

Figure 2. Dead Time vs RDU/RDL Resistor (Silicon)

Figure 3. Dead Time vs RDU/RDL Resistor (Simulation)

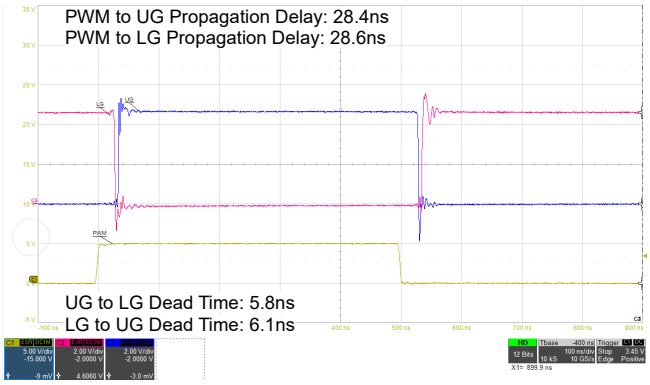

Figure 4. PWM Propagation and Dead Time Delay with RDU = RDL = 1.3kΩ; PHS = PGND; BOOT = PVCC (Silicon)

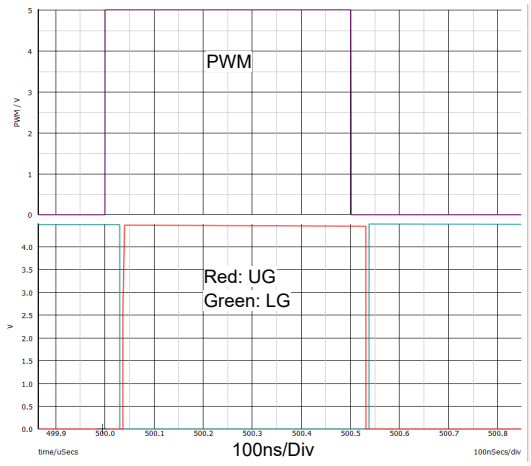

Figure 5. PWM Propagation and Dead Time Delay with RDU = RDL = 1.3kΩ; PHS = PGND; BOOT = PVCC (Simulation)

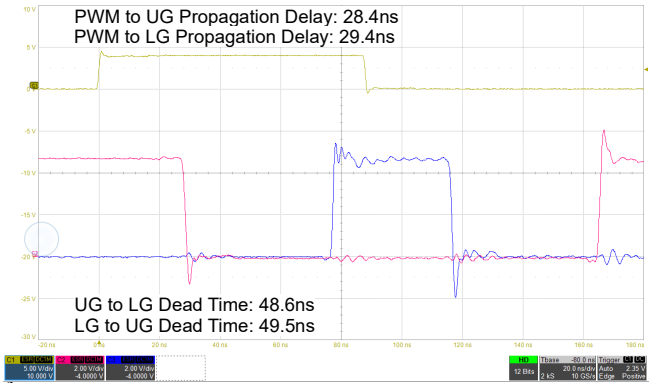

Figure 6. PWM Propagation and Dead Time Delay with RDU = RDL = 10kΩ; PHS = PGND; BOOT = PVCC (Silicon)

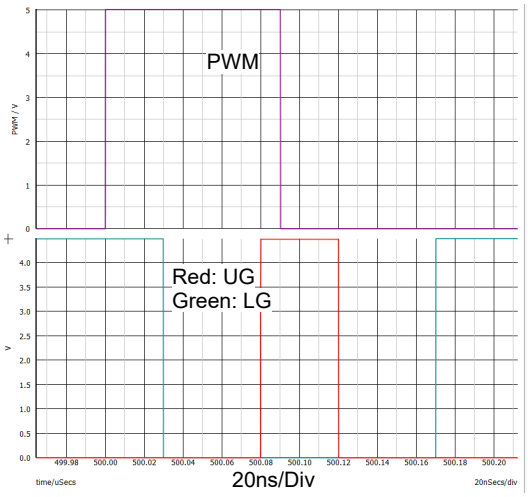

Figure 7. PWM Propagation and Dead Time Delay with RDU = RDL = 10kΩ; PHS = PGND; BOOT = PVCC (Simulation)

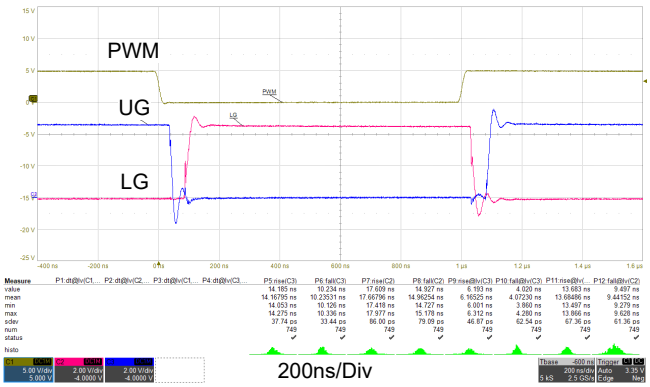

Figure 8. UG/LG Rise and Fall Time with 5.1nF on UG; 10nF on LG; PHS = PGND; BOOT = PVCC (Silicon)

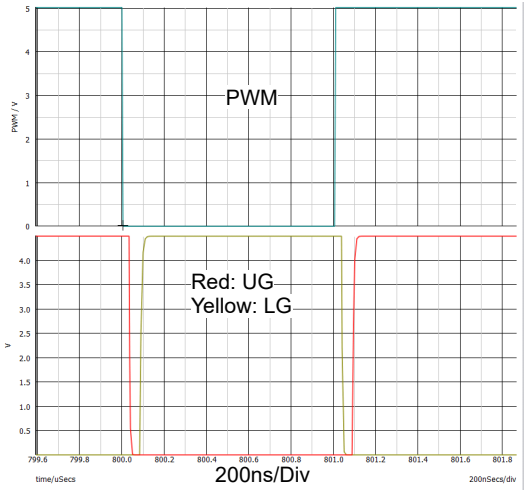

Figure 9. UG/LG Rise and Fall Time with 5.1nF on UG; 10nF on LG; PHS = PGND; BOOT = PVCC (Simulation)

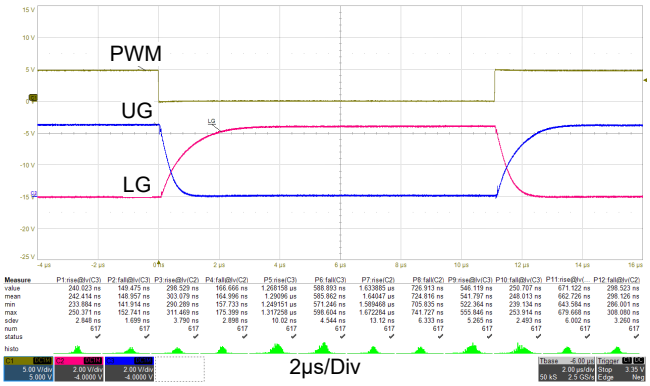

Figure 10. UG/LG Rise and Fall Time with 470nF on UG; 1000nF on LG; PHS = PGND; BOOT = PVCC (Silicon)

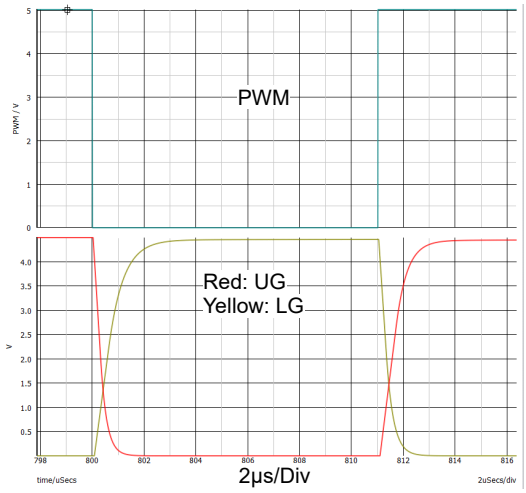

Figure 11. UG/LG Rise and Fall Time with 470nF on UG; 1000nF on LG; PHS = PGND; BOOT = PVCC (Simulation)

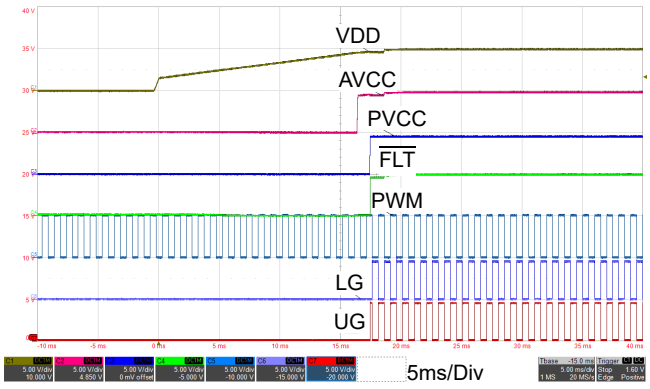

Figure 12. V_{DD} Supply Power-Up Sequence (Silicon)

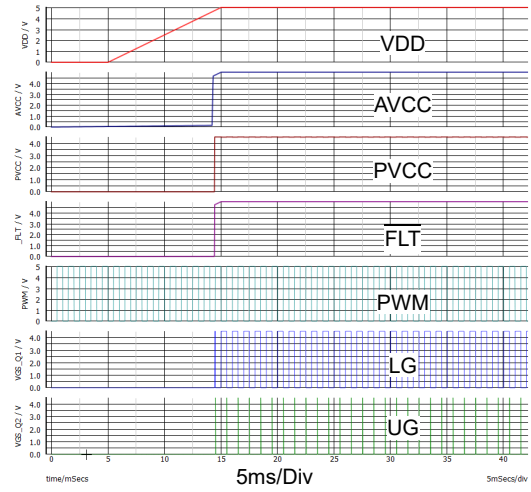

Figure 13. V_{DD} Supply Power-Up Sequence (Simulation)

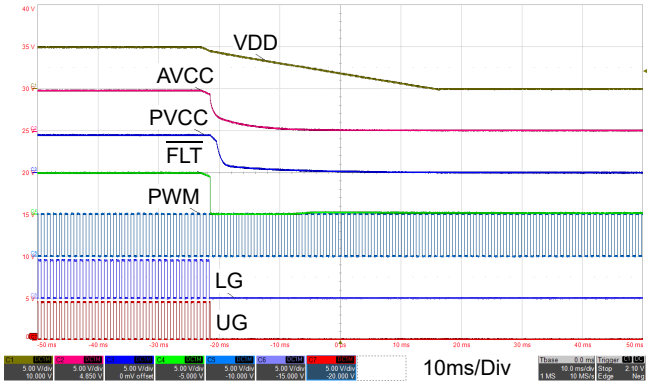

Figure 14. V_{DD} Supply Power-Down Sequence (Silicon)

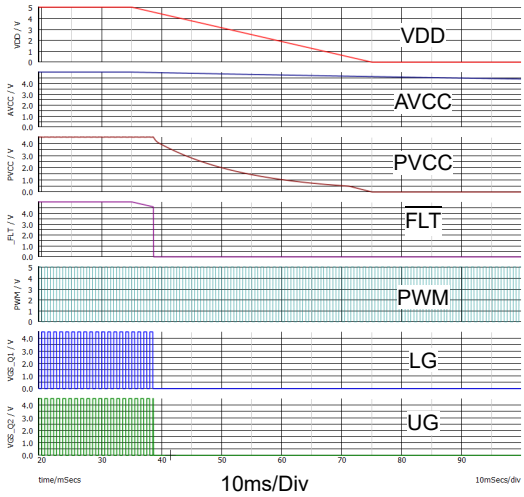

Figure 15. V_{DD} Supply Power-Down Sequence (Simulation)

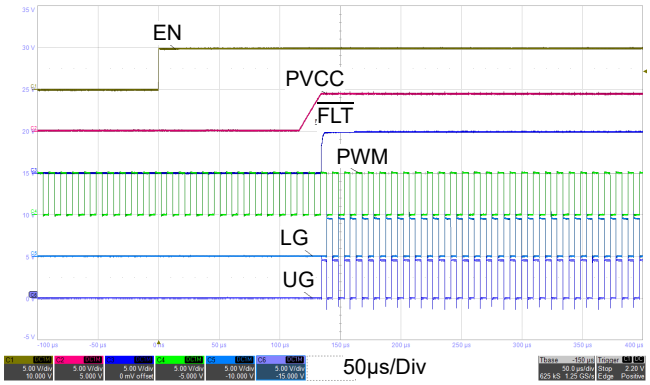

Figure 16. EN Rising Sequence (Silicon)

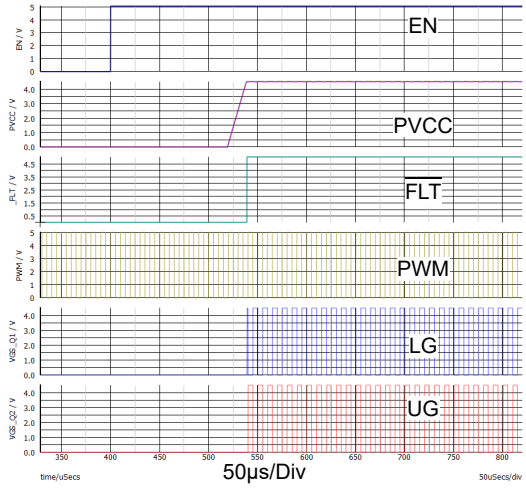

Figure 17. EN Rising Sequence (Simulation)

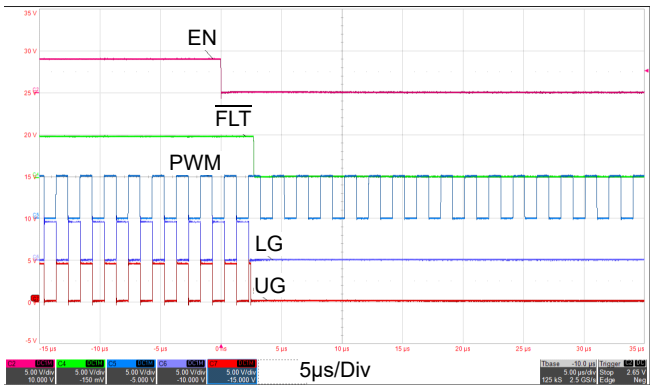

Figure 18. EN Falling Response (Silicon)

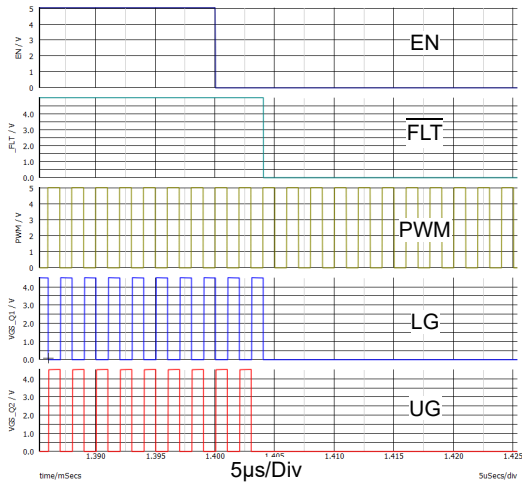

Figure 19. EN Falling Response (Simulation)

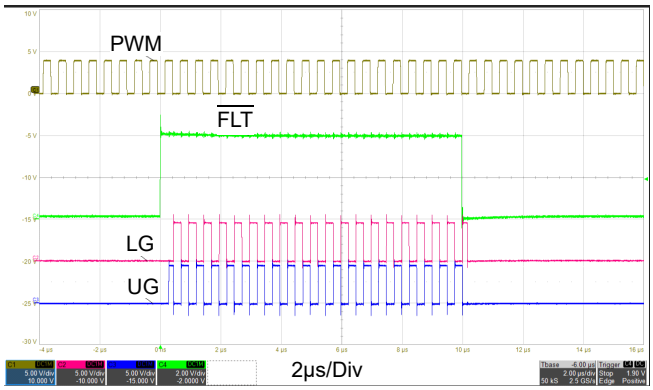

Figure 20. $\overline{FLT}$ Transient Response (Silicon)

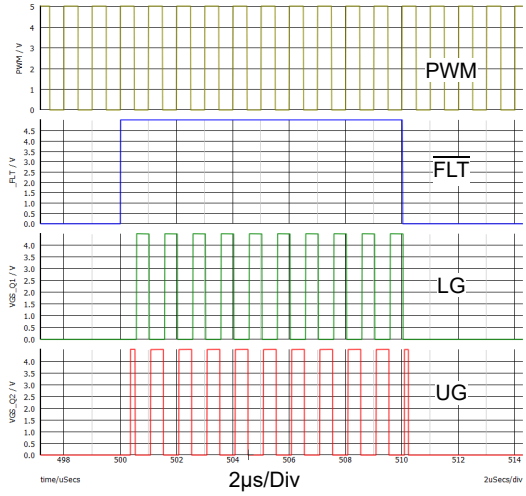

Figure 21. $\overline{FLT}$ Transient Response (Simulation)

Positive Window Detect Rising Threshold	-	PWM = 0V	-55 to +125°C	**160**	250	**400**	mV
Positive Window Detect Falling Threshold	-	PWM = 0V		**140**	220	**380**	mV
Negative Window Detect Rising Threshold	-	PWM = 0V		**-380**	-210	**-140**	mV
Negative Window Detect Falling Threshold	-	PWM = 0V		**-400**	-240	**-160**	mV

Figure 22. PHS Detect Window Voltage (Silicon)

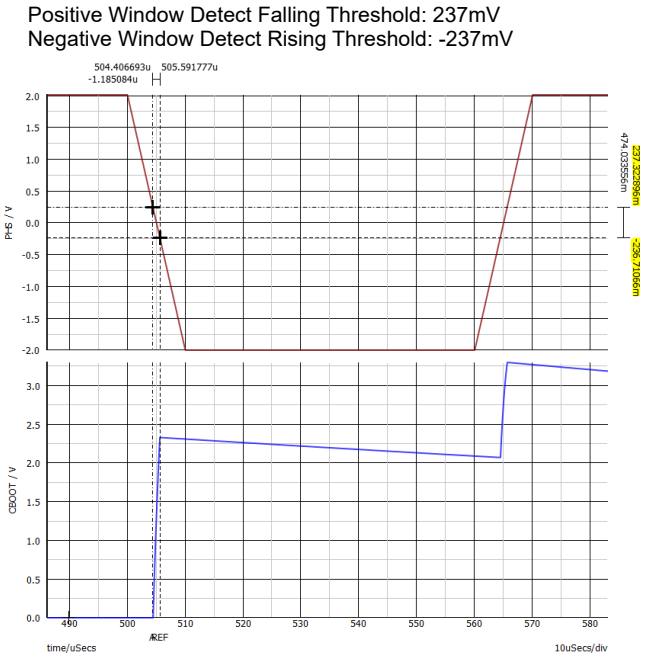

Figure 23. PHS Detect Window Voltage Showing Boot Switch Charging/Discharging BOOT (Simulation)

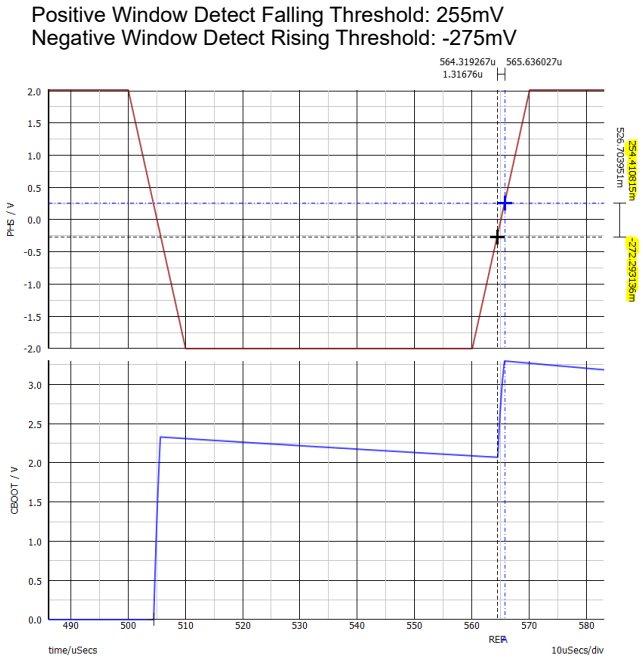

Figure 24. PHS Detect Window Voltage Showing Boot Switch Charging/Discharging BOOT (Simulation)

PWM High Threshold	V_{PWMH}	VDD = 4.75V to 13.2V	-55 to +125°C	-	2.7	**2.8**	V
PWM Middle Level Range	V_{PWMM}	VDD = 4.75V to 13.2V		**1.45**	-	**2.4**	V
PWM Low Threshold	V_{PWML}	VDD = 4.75V to 13.2V		**0.95**	1.1	-	V
Mid-High Level Hysteresis	-	VDD = 4.75V to 13.2V		-	100	**200**	mV
Mid-Low Level Hysteresis	-	VDD = 4.75V to 13.2V		-	200	**350**	mV

Figure 25. PWM Threshold Levels (Silicon)

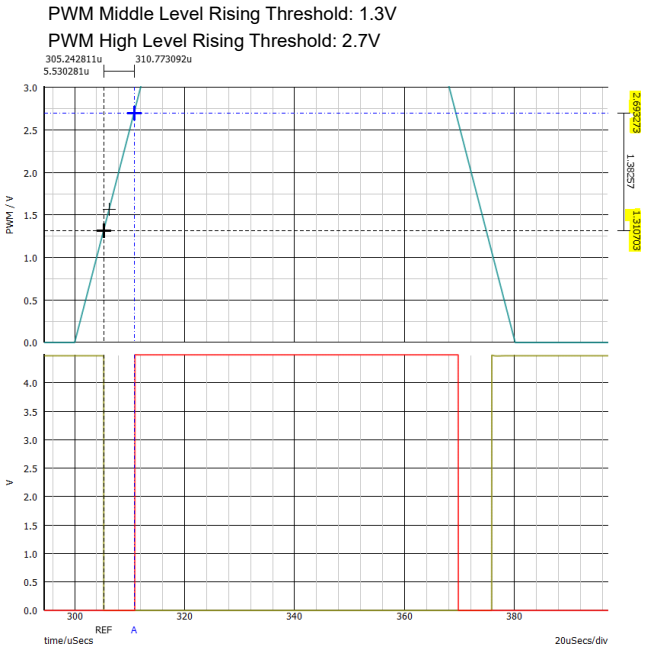

Figure 26. PWM Threshold Levels (Simulation)

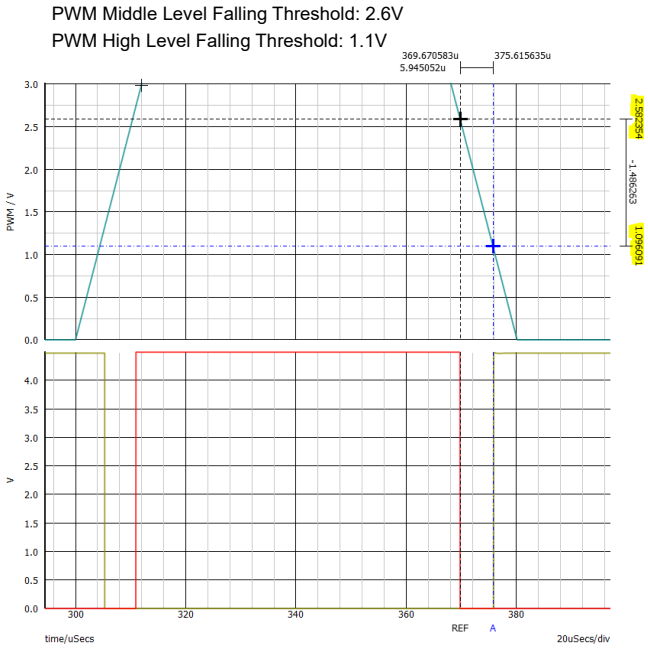

Figure 27. PWM Threshold Levels (Simulation)

PVCC Gate Drive Voltage	PVCC	PVCC = 4.5V = FB or with external resistors; I_{OUT} from 0mA to 150mA; VDD from 4.85V to 13.2V	-55°C	4.39	4.5	4.6	V
			+25°C	4.4	4.5	4.6	
			+125°C	4.39	4.5	4.6	
			+25°C (Post Rad)	4.39	4.5	4.6	
PVCC Output Current Limit	I_{LIMITP}	VDD = 4.75V; FB = PVCC; Force PVCC = 4.2V	-55 to +125°C	**190**	250	**350**	mA

Figure 28. PVCC Load Regulation and Constant Current Limit (Silicon)

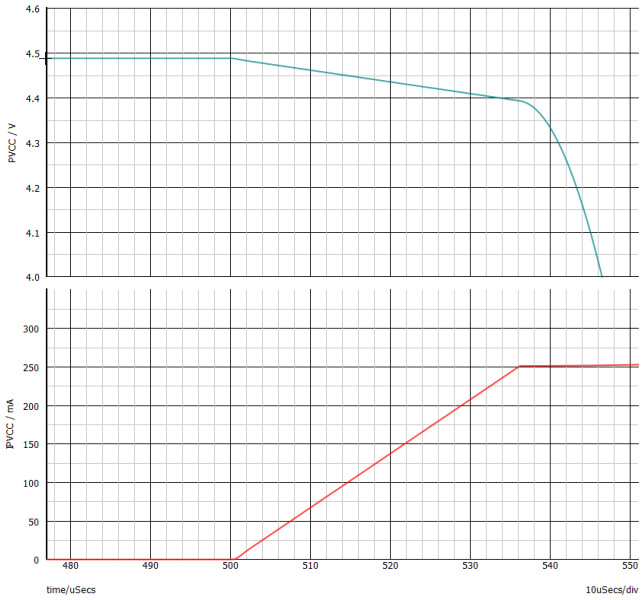

Figure 29. PVCC Load Regulation and Constant Current Limit (Simulation)

Quiescent Supply Current	I_{DDQ}	PWM = Float; RDU = RDL = 1.3kΩ	-55 to +125°C	-	9	-	mA
BOOT Quiescent Current	I_{Q_Boot}	PWM = Float; BOOT-PHS = 4.5V	-55 to +125°C	-	580	**650**	µA

Figure 30. V_{DD} and BOOT Quiescent Current with RDU = RDL = 1.3kΩ (Silicon)

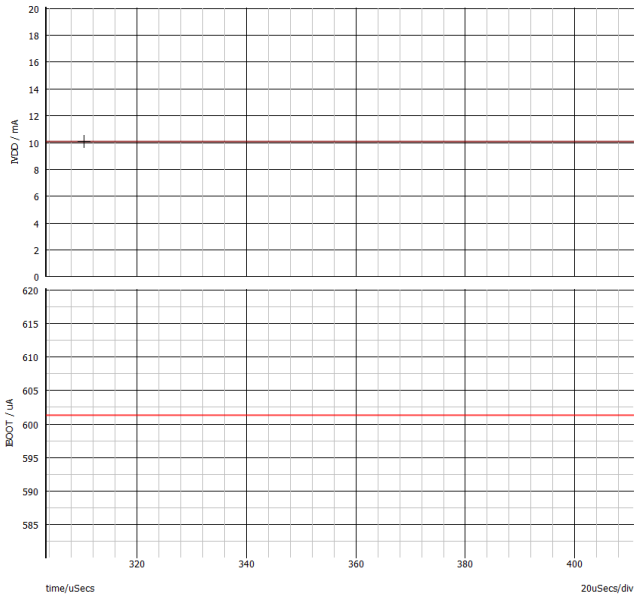

Figure 31. V_{DD} and BOOT Quiescent Current with RDU = RDL = 1.3kΩ (Simulation)

6. Revision History

Revision	Date	Description
1.00	Oct 23, 2023	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.