ISL94202 Sleep Mode Requirements

This application note reviews the ISL94202 operational modes and requirements to enter, remain in, or exit SLEEP Mode. Operation of the LDMON and CHMON pins as related to SLEEP Mode entry and exit is covered in detail.

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1. Description

The ISL94202 is a battery pack Battery Front end IC that supports three to eight series connected cells. It provides complete battery monitoring and pack control. The ISL94202 provides automatic shutdown and recovery from out-of-bounds conditions and automatically controls pack cell balancing. The internal EEPROM makes the ISL94202 a highly configurable stand-alone device, but can be used with an optional external Microcontroller (MCU), which communicates to the ISL94202 through an I^2C interface.

This document describes the modes of operation with specific attention to the function of LDMON and CHMON Pins. The reader should be familiar with the operation of the ISL94202 and the evaluation kit hardware and software as a prerequisite. See the ISL94202 datasheet for more details about the settings discussed in this document.

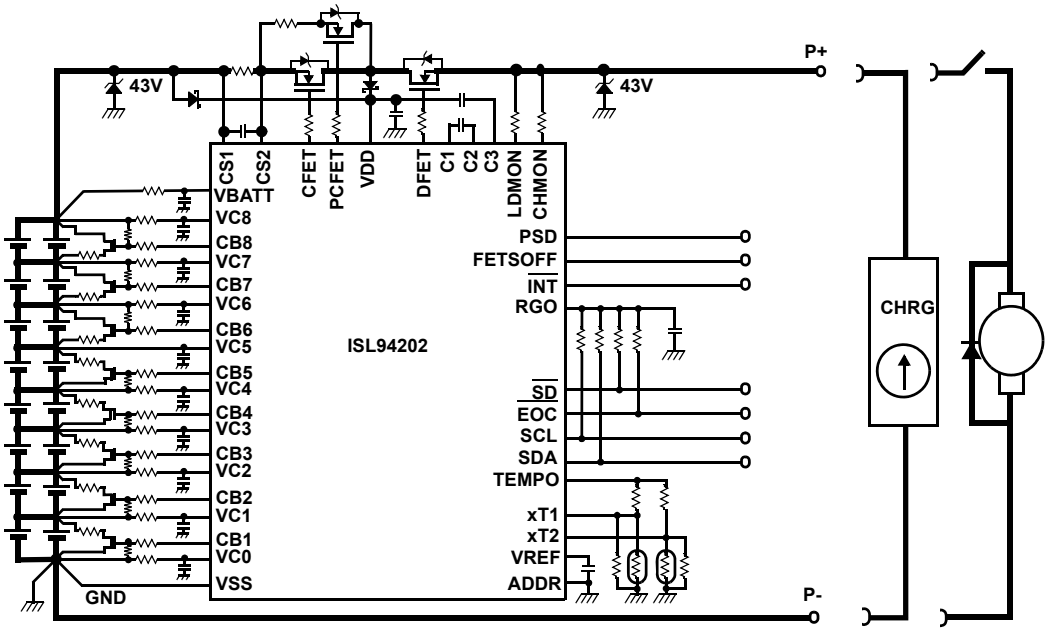

Figure 1. Typical Application Diagram

1.1 System Modes

To minimize power consumption, most circuits are kept off when not being used and system conditions are sampled at intervals. There are five power states in the device as shown in Figure 2. Power-down is a static non-operational state while the other states are also referred to as Modes because they are functional.

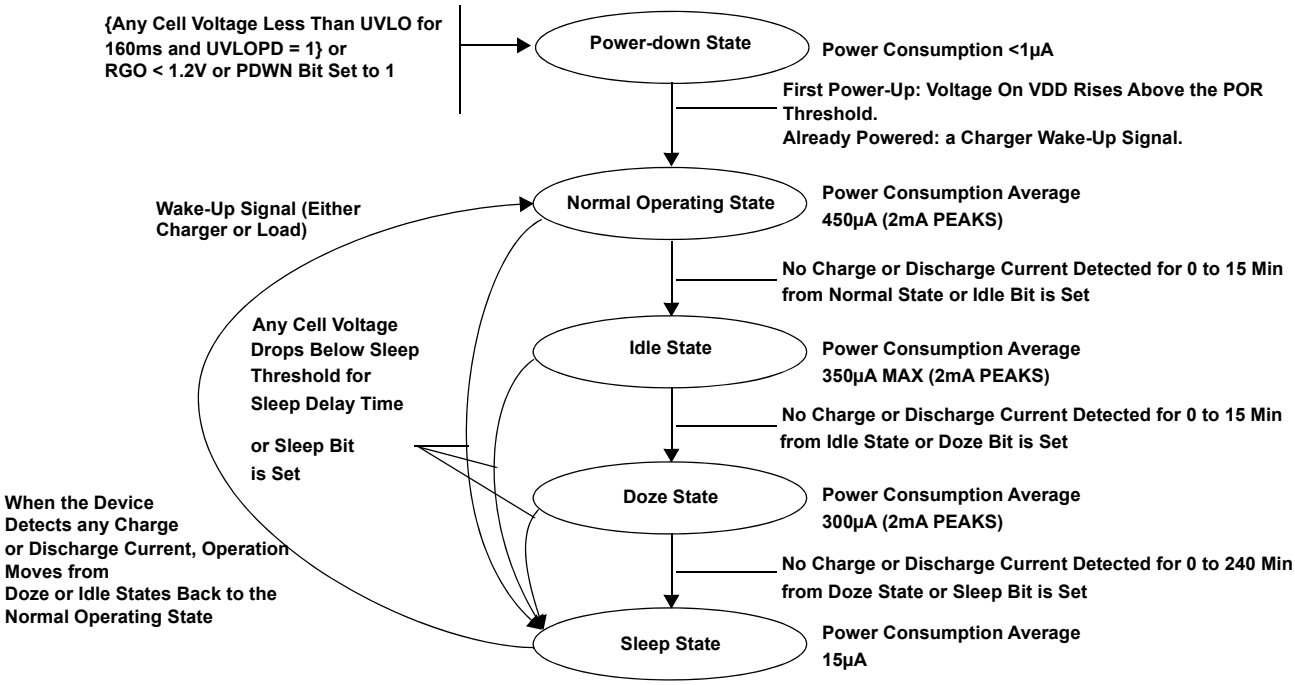

Figure 2. ISL94202 Mode transitions.

1.1.1 Power-Down State

The ISL94202 tolerates hot plug and unknown connection sequences. Often when the device PCB is first mated to a battery pack the pin connection sequence is random. After the VDD Pin (43) and VSS Pin (18, 28, 29) pins connect, the device enters the Power-down state. It remains in this state until a charger is connected. The device also powers up if the CHMON Pin (37) is connected to the top of the pack through an outside resistor to enable PCB test. This is implemented with a Wakeup button on the evaluation board.

It is possible that the pack powers up automatically when the battery stack is connected because of momentary conduction through the power FET G-S and G-D capacitors.

The device also enters the Power-down State when the voltage on the pack is too low for proper operation. This occurs when:

- VDD is less than the POR threshold and RGO < 2.25V. This condition can occur in low cell count packs, or low voltage storage components are used, or if cells discharge over a long period of time.
- VDD is less than 1V and RGO > 2.25V. This condition can occur during a short-circuit with minimum capacity cells. VDD drops out, but the RGO cap maintains the logic supply.
- A cell voltage is less than the 0x0A-0B VCELL UVLO threshold for >160ms and 0x4B.3 UVLOPD = 1.
- Commanded by an external MCU (set 0x88.3 PDWN = 1). The device no longer communicates following this command. It is typically used at the end of Pack production test in preparation for storage.

Recovering out of the Power-down state brings the ISL94202 into the NORMAL Mode. The only way to recover from this state (transition to NORMAL Mode) is through a charger detection.

Note: If a load is detected on exit from Power-down, the power FETs are disabled as a safety precaution and the load must be removed before the FETs can be enabled.

1.1.2 NORMAL Mode

This is the monitoring/scan state for the ISL94202 during charge and discharge operation. In this Mode, the device monitors for overcurrent continuously and scans the voltages every 32ms. If balancing is required, the device activates balancing components. All necessary circuits are on and unnecessary circuits are off.

During the scan, the ISL94202 draws more current as it activates the input level shifter, the ADC, and data processing. Between scans, circuits turn off to minimize power consumption. The device remains in NORMAL Mode as long as charge or discharge current is detected (0x82.2 CHING or 0x82.3 DCHING is set). The device will return to NORMAL Mode from IDLE or DOZE Modes if either charge or discharge currents are detected.

1.1.3 IDLE Mode

If there is no current flowing for 0 to 15 minutes (set by 0x48.[3:0] Idle/Doze Timer), the device transitions from NORMAL to IDLE Mode. This is governed by the time when bits 0x82.2 CHING and 0x82.3 DCHING were cleared, the time since last detecting a charge or discharge current. If there is no current flowing for this time, the device enters IDLE Mode. Measurement scans decrease to once every 256ms in IDLE Mode. The FETs and RGO remain on. The device consumes less current in IDLE Mode because of the decrease in scan frequency.

The device transitions back to NORMAL Mode if a charge (bit 0x82.2 CHING sets) or discharge (bit 0x82.3 DCHING sets) current is detected.

The device does not automatically enter the IDLE Mode if bit 0x87.2 µCSCAN is set to 1, because the MCU is responsible for triggering scans and controlling device operation.

Setting 0x88.0 IDLE to 1 forces the device to enter IDLE Mode, regardless of current flow. The device remains in IDLE Mode after the MCU sets this bit, regardless of the timer or the current. Setting the Mode control bits to 0 allows the device to control the Mode based on the timer settings.

1.1.4 DOZE Mode

If there is no current flowing for 0 to 15 minutes (set by 0x48.[3:0] Idle/Doze Timer), the device transitions from IDLE to DOZE Mode. This is determined by the time since the device entered IDLE Mode and bits 0x82.2 CHING and 0x82.3 DCHING remain cleared. If there is no current flowing for the set time, the device enters DOZE Mode. Measurement scans decrease to once every 512ms in DOZE Mode. The power FETs and RGO remain on. The device consumes less current in DOZE Mode because of the decrease in scan frequency.

The device transitions back to NORMAL Mode if a charge (bit 0x82.2 CHING sets) or discharge (bit 0x82.3 DCHING sets) current is detected.

The device does not automatically enter the DOZE Mode if bit 0x87.2 µCSCAN is set to 1, because the MCU is responsible for triggering scans and controlling device operation.

Setting 0x88.1 DOZE to 1 forces the device to enter the DOZE Mode, regardless of the current flow. The device remains in DOZE Mode after the MCU sets this bit, regardless of the timer or the current. Setting the Mode control bits to 0 allows the device to control the Mode based on the timer settings.

1.1.5 SLEEP Mode

The ISL94202 transitions to SLEEP from DOZE Mode if there was no current flow detected for more than the duration of the sleep mode timer setting (0x48.[7:4] SLEEP Timer). The device remains in DOZE Mode until there has been no current for 0 to 240 minutes (with 16 minute steps).

The device does not automatically enter the SLEEP Mode if bit 0x87.2 µCSCAN is set to 1, because the MCU is responsible for triggering scans and controlling device operation.

Setting bit 0x88.2 SLEEP to 1 forces the device to enter the SLEEP Mode regardless of the current flow. After an MCU sets the SLEEP bit, the device remains in SLEEP Mode regardless of the timer or the current. Setting the Mode control bits to 0 allows the device to control the Mode.

The ISL94202 transitions to SLEEP Mode if a cell voltage drops below the Sleep Level Voltage threshold (0x44-45 SLV) for the time specified by the Sleep Level Timer (0x47.[0] - 0x46.[7:0] SLT). The SLV register can be set to 0

to prevent the device from entering SLEEP Mode by a low voltage on the cells. If 0x87.6 µCFET = 1, the SLV setting is ignored and cannot place the device into SLEEP.

While the ISL94202 is in SLEEP, register 0x8A-8B CELMIN reads 0x000 and register 0x8C-8D CELMAX reads 0x0FFF. When waking up, these registers are restored to their previous setting (last reading before entering SLEEP) within ~540µs.

While in the SLEEP Mode, everything is off (including the power FETs) except for the 2.5V regulator (RGO) and the wake-up circuits. To wake and transition back to NORMAL Mode, either a LDMON Pin (38) load or CHMON Pin (37) charger detection must be made. Detections by these pins can wake the device 50ms after it first attempts Sleep if either a load or charger is present (Node P+ in Figure 1). A charged capacitor on P+ can cause a false charger detection if not discharged with 50ms of entry into Sleep.

The part resumes system scans ~1.5ms after waking from SLEEP.

1.1.6 Idle/Doze/Sleep Timers

Setting the Idle/Doze timer to 0 immediately forces the device from NORMAL into the DOZE Mode if there is no detected current. To transition back to NORMAL Mode, either 0x82.2 CHING or 0x82.3 DCHING bits must be set because of a charge or discharge current detection.

If 0x48.[7:4] Sleep Timer is set to 0, the device transitions from DOZE to SLEEP Mode immediately and it may appear as if it skipped DOZE Mode.

If both Idle/Doze and Sleep timers are set to 0, the device immediately goes to SLEEP Mode when there is no charge or discharge current detected. To wake the device, a charger (CHMON Pin (37)) or load (LDMON Pin (38)) detection must be followed by writing a non-zero setting to the timer registers.

1.1.7 Mode Exceptions

There is one exception to the normal sequence of Mode management. When the MCU sets bit 0x87.2 µCSCAN to 1, the internal scan stops. This means that the device no longer looks for the conditions required for Sleep. The external MCU must manage the Modes of operation. Forcing the device into different Modes can be achieved by using the following bits:

- 0x88.0 IDLE
- 0x88.1 DOZE
- 0x88.2 SLEEP
- 0x88.3 PDWN

Possible forced transitions using these bits and an external MCU are shown in Table 1.

Table 1. Forced Mode Transitions

FROM	TO				
	PDOWN	**NORM**	**IDLE**	**DOZE**	**SLEEP**
PDOWN	N/A	NO*	NO	NO	NO
NORM	YES	N/A	YES	YES	YES
IDLE	YES	NO	N/A	YES	YES
DOZE	YES	NO	YES	N/A	YES
SLEEP	NO	NO	NO	NO	N/A

Note: A transition from Power-down to NORMAL Mode is only possible through detection of a charger connection. The detection of a charger or load forces the device into NORMAL Mode from any other Mode.

2. CHMON Pin

The Charge Monitor pin tests for a charger connection. In a series path power FET configuration the CHMON pin connects through a resistor (499Ω) to the input of the positive charger connection as shown in Figure 3 (PACK+). This node includes the DFET source in a series power FET configuration.

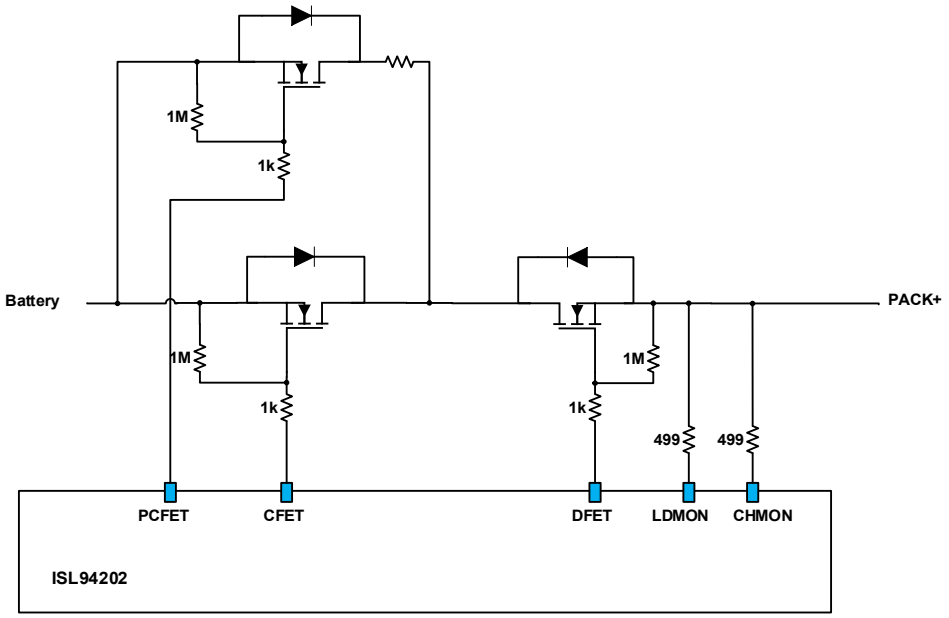

Figure 3. Series Path

In a split path configuration the CHMON pin connects through a resistor (499Ω) to the input of the positive charger connection as shown in Figure 4 (CHG+). VGS diodes are omitted from the figures for clarity. This pin should not be tied to the LDMON pin and it should not share a resistor with LDMON.

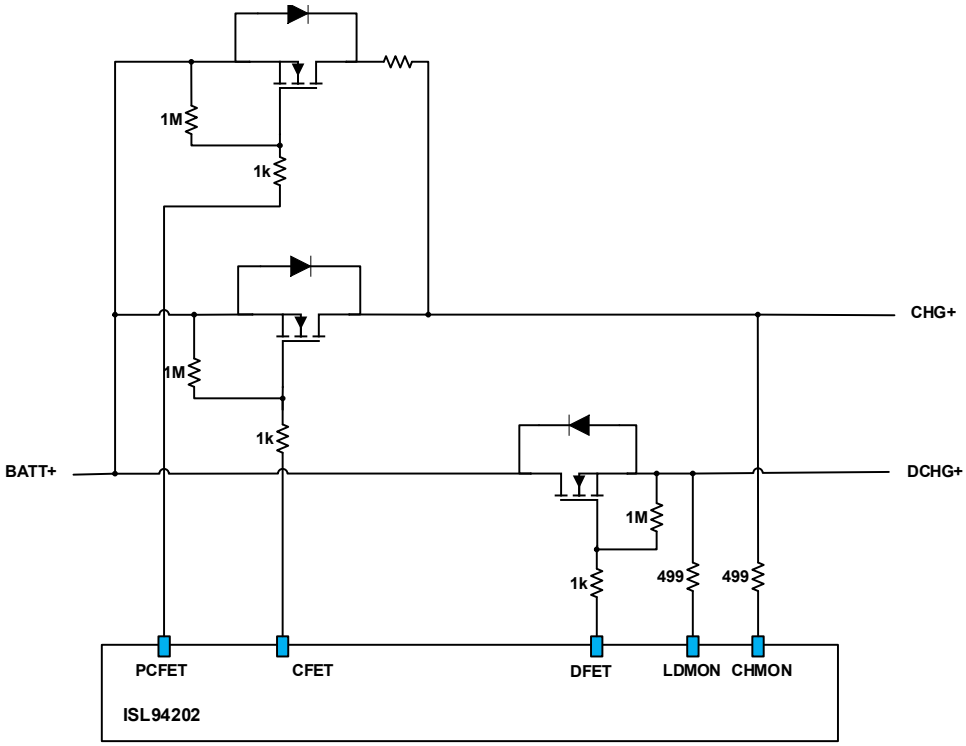

Figure 4. Parallel Path

The charge monitoring mechanism is different depending on which of two states the device is in. The first state is Charge Overcurrent Recovery, which uses the CHMON pin to detect the removal of the charger following a Charge Overcurrent Fault (0x81.1 COCF). The second state is Wake-up, which functions to wake the device up when detecting a charger if the device is in SLEEP Mode or the Power-down State, see Charger Detection.

2.1 Charge Overcurrent Recovery

If the ISL94202 detects a Charge Overcurrent condition, the Charge Overcurrent Recovery process begins (Figure 5) ~3s after the fault is detected. The CHMON pin pulls ~60µA from the node for a duration set by register 0x01.7:4 CDPW every 256ms. With a charger present the CHMON pin voltage is above the detection threshold (Figure 7) and bit 0x82.1 CH PRSNT is set to 1. After the charger is removed, the CHMON pin voltage drops below the threshold, resulting in the CH_PRSNT bit clearing.

If the µCFET bit is set to 0 and the charge monitor detects the charger has been removed for two consecutive sample periods (CH_PRSNT = 0), the power FETs are re-enabled (assuming no other faults) and the fault bit COCF is cleared. If the µCFET bit is set to 1, the external MCU must re-enable the FETs.

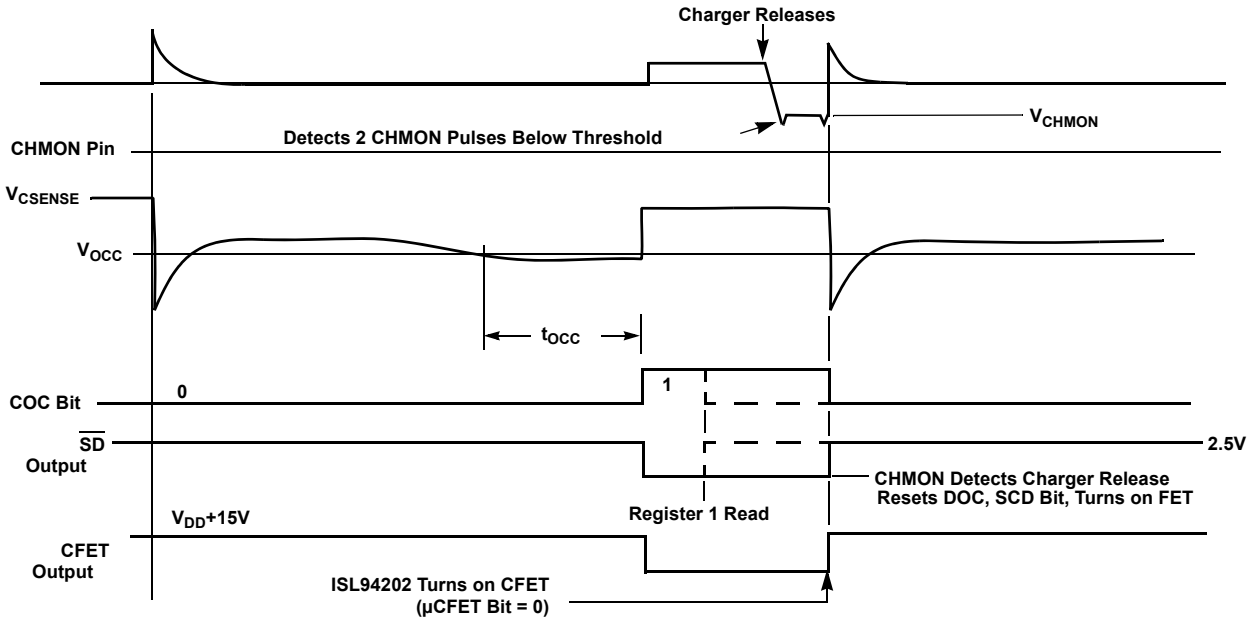

Figure 5. COC Recovery

2.2 Charger Detection

If the ISL94202 is in the Power-down State, a charger connection must be used to wake the device up. If in SLEEP Mode, a charger or load connection can be used to wake the device up.

On entering SLEEP Mode, the ISL94202 keeps the wake-up circuit disabled for ~50ms. After the this delay, the device enables both the load and charger detection circuits (Figure 6). The device exits SLEEP to NORMAL Mode if a detection is made. If after the 50ms delay there is no load or charger detection, the wakeup circuit stays enabled and the device remains in SLEEP Mode until a load or charger is detected (Figure 8). These detection circuits do not draw significant current.

Note: It is important to be aware of the timing and voltage levels. If an application has a particularly large capacitive load with a slow discharge rate, there is a possibility that the voltage seen at the CHMON pin is high enough to prevent SLEEP because the voltage triggers a false charger detection. Conversely, if the voltage at CHMON drops too low the device detects a load connection. See Figure 7.

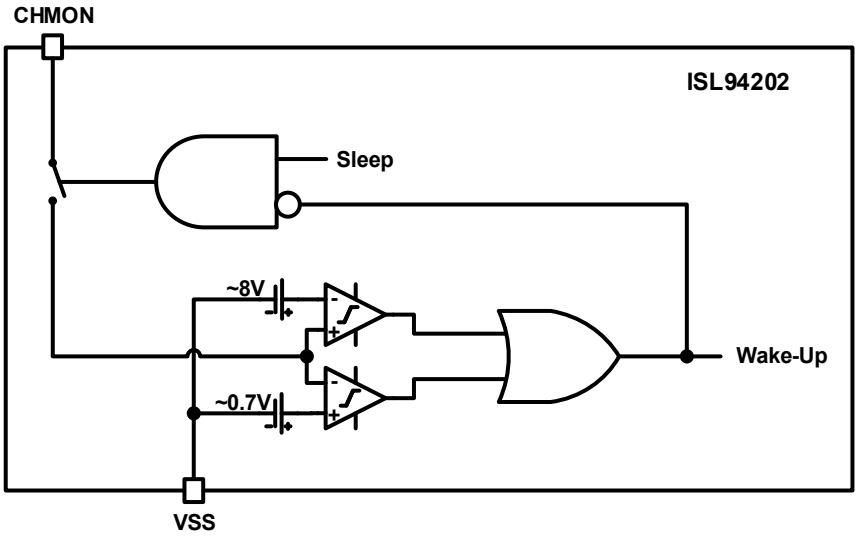

Figure 6. CHMON Wake Up

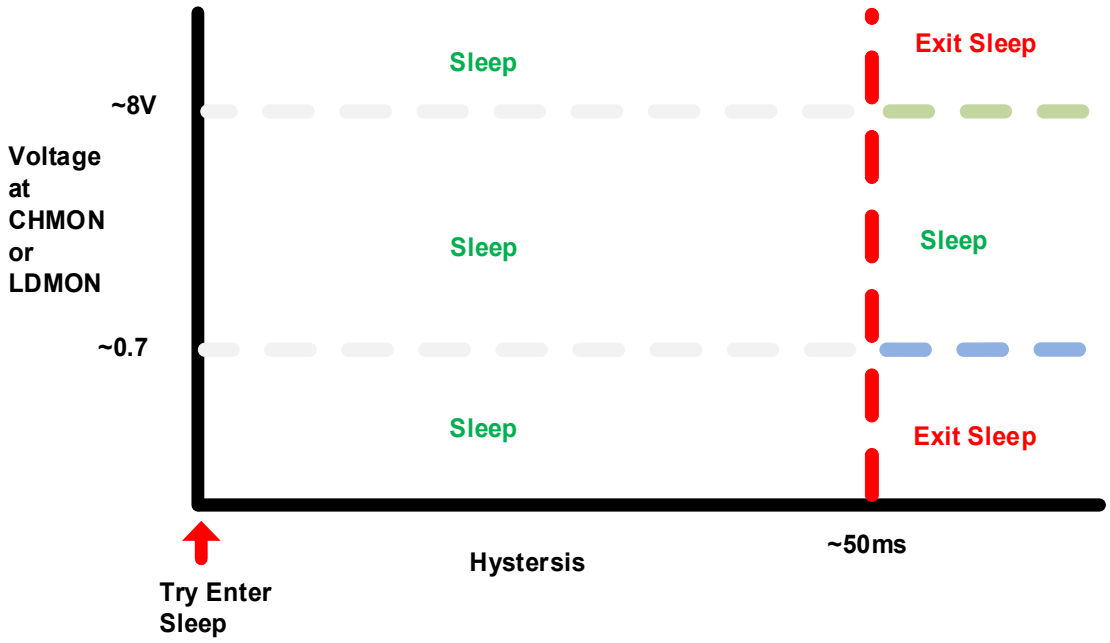

Figure 7. Sleep Qualifications

Note: It is important if the voltage after the ~50ms delay seen at either CHMON or LDMON is not between ~0.7V and ~8V, the device does not stay in SLEEP Mode. If there is a large load capacitance, it may be necessary to partially discharge this capacitor before the device sleeps. See Sleep Entry for more details.

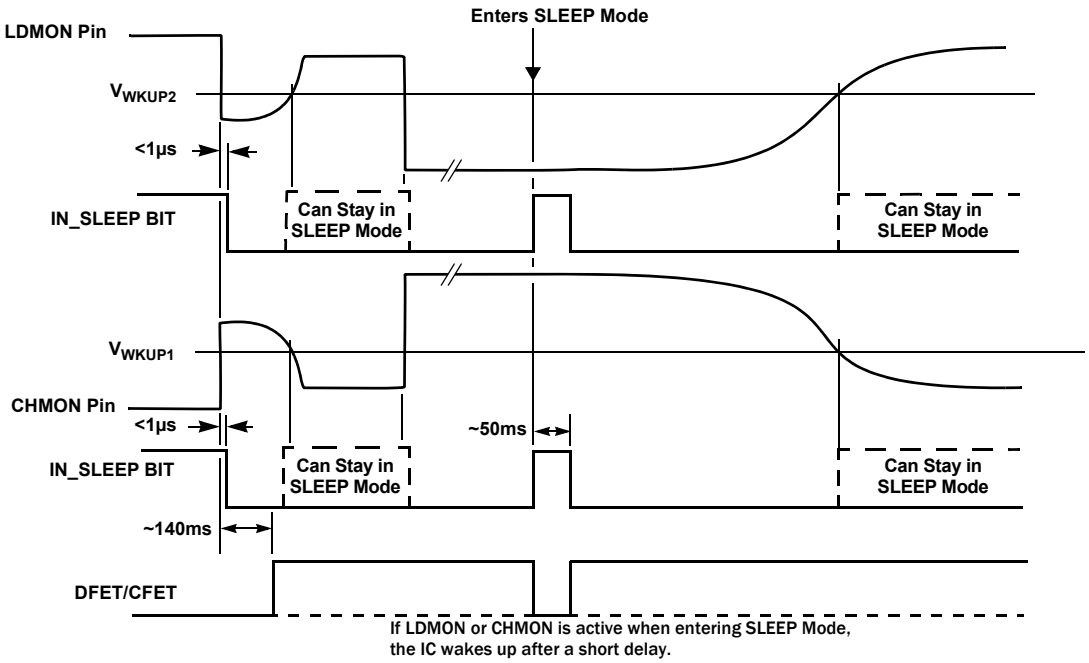

Figure 8. Wake-Up Timing (from Sleep)

When a charger is connected, it pulls the floating output node up, which can be well above the discharged pack voltage depending on the charger. To mimic a charger detection a momentary connection is made from PACK+ to the top of the battery pack. This is equivalent to using the wakeup button on the ISL94202 evaluation board.

Figure 9 shows a charger detection following a relatively long (>>50ms) period of Sleep. The initial detection is at t = 0 with the second one at ~140ms. **Note:** V_{OUT} (PACK+ in Figure 3) remains above the charge detection threshold during this period.

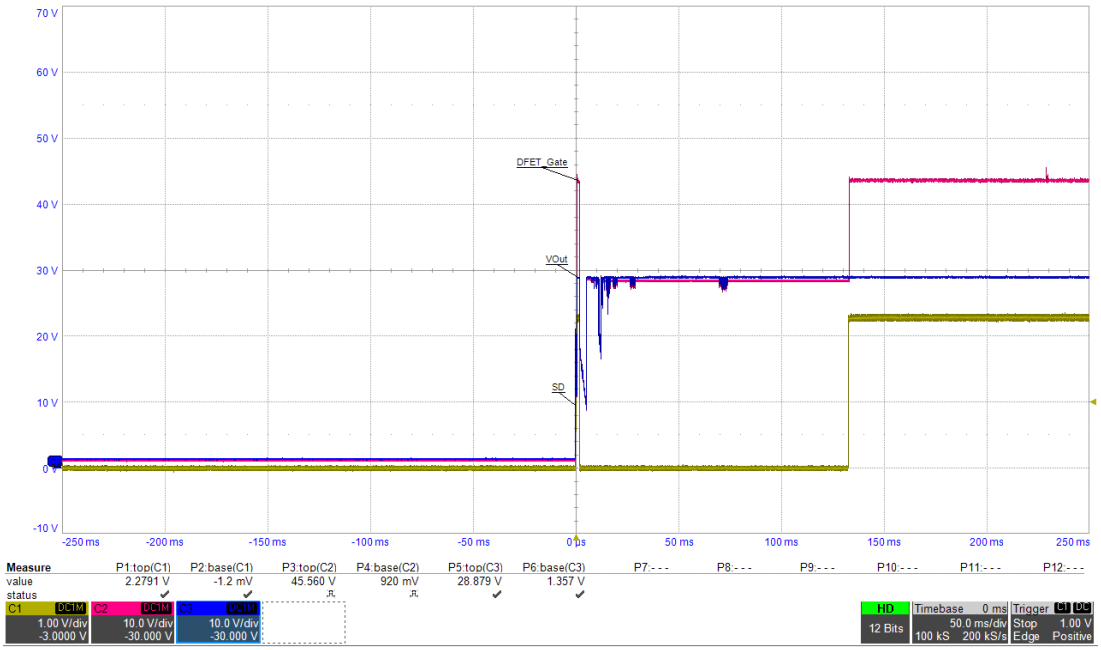

Figure 9. CHMON Detection (both)

Figure 10 is a detailed view of the first detection, V_{OUT} rises above the charge detection threshold at t = 0. When this happens $\overline{SD}$ releases, the power FETs are enabled and V_{OUT} rises to the battery pack/charger voltage. Less than 2ms later $\overline{SD}$ reasserts, Power FETs are disabled and V_{OUT} is set by the charger voltage (The pack voltage in this case). **Note:** The glitches occurring between the first and second detection are because of the act of mechanically connecting the nodes together.

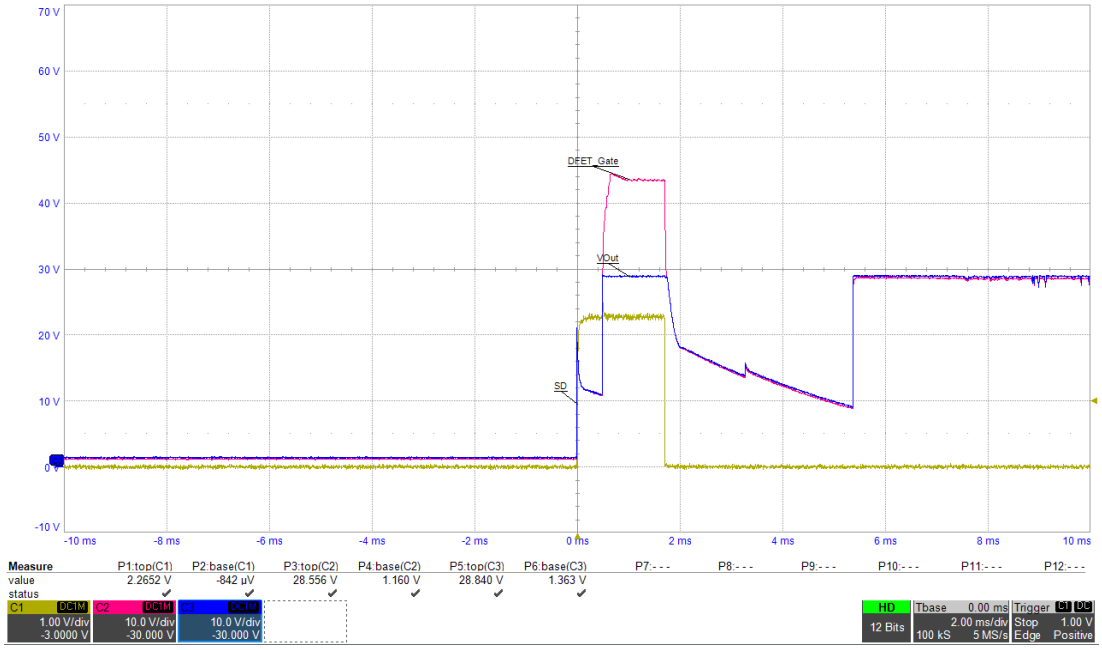

Figure 10. CHMON Detection (first)

3. LDMON Pin

The load monitor pin is designed to detect a connected load. In either a series (Figure 3) or parallel (Figure 4) path power FET configuration the LDMON pin connects through a resistor (499Ω) to the positive output of the discharge path (PACK+). This node must include the DFET source. This pin should not be tied to the CHMON pin, and it should not share a resistor with CHMON.

The load monitoring mechanism is different depending on which of two states the device is in. The first state is Discharge Overcurrent Recovery, which uses the LDMON pin to detect the removal of the load following a Discharge Overcurrent Fault (0x81.2 DOCF) or a Discharge Short Circuit Fault (0x81.3 DSCF). The second state is Wake-up, which functions to wake the device up when detecting a load if the device is in SLEEP Mode, see Load Detection.

Load detection does not bring a device out of the Power-down State, but a detection of a charger and a load in Power-down can result in the device waking into NORMAL Mode with the power FETs off. The load must be removed to recover, then the FETs are enabled.

3.1 Discharge Overcurrent Recovery

If the ISL94202 detects a DOC or DSC condition, the Discharge Overcurrent Recovery process (Figure 11) begins ~3s after the fault is detected. The LDMON pin injects ~60µA into the load for a duration set by the Load Detect Pulse Width register (0x05.7:4 LDPW) every 256ms. With a load present the LDMON pin voltage falls below the detection threshold and bit 0x82.0 LD PRSNT is set to 1. After the load is removed or rises to a sufficiently high resistance, the LDMON pin voltage rises above the threshold, which results in the LD_PRSNT bit clearing.

If the µCFET bit is set to 0 and the load monitor detects that the load has been removed (LD_PRSNT = 0), the power FETs are re-enabled (assuming no other faults) and the fault bit 0x81.2 DOCF is cleared.

If the µCFET bit is set to 1 and LD_PRSNT along with the DOC fault bit clear, the external MCU must re-enable the FETs.

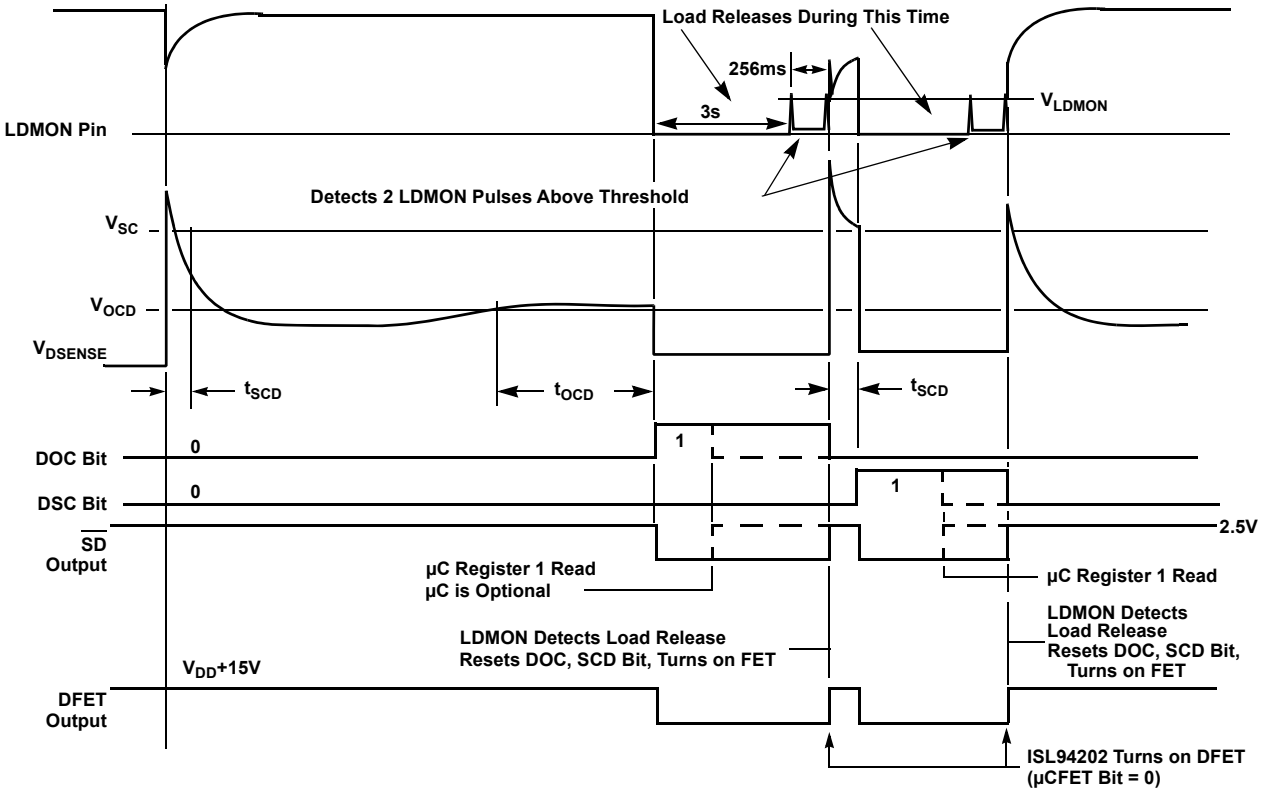

Figure 11. DOC and DSC Recovery

3.2 Load Detection

If the device is in SLEEP Mode, a load connection can be used to wake the device up. A load connection does not wake the device from Power-down, a charger connection is required.

When entering SLEEP Mode (using 0x44-45 SLV, 0x48.[3:0] Idle/Doze Timer, or 0x88.2 Sleep), the ISL94202 keeps the wake-up circuit disabled for ~50ms. During this time, the ISL94202 is in SLEEP Mode. After this delay, the ISL94202 enables the load detection (Figure 12) and charger detection circuits. If a detection is made, the device exits SLEEP to NORMAL Mode. If after the 50ms period there is no load or charger detection, the wakeup circuit stays enabled and the device remains in SLEEP Mode. The circuit does not draw significant current.

Note: A charger connection to LDMON while in SLEEP Mode also wakes the device.

Important: Be aware of the timing and voltage levels. If an application has a particularly large capacitive load with a slow discharge rate, there is a possibility that the voltage seen at the LDMON pin is large enough to stop the device from sleeping. Conversely, if the voltage at LDMON drops to ~0V to quickly (<50ms), this also stops the device from remaining in SLEEP Mode as the ISL94202 detects a load connection. See Figure 7.

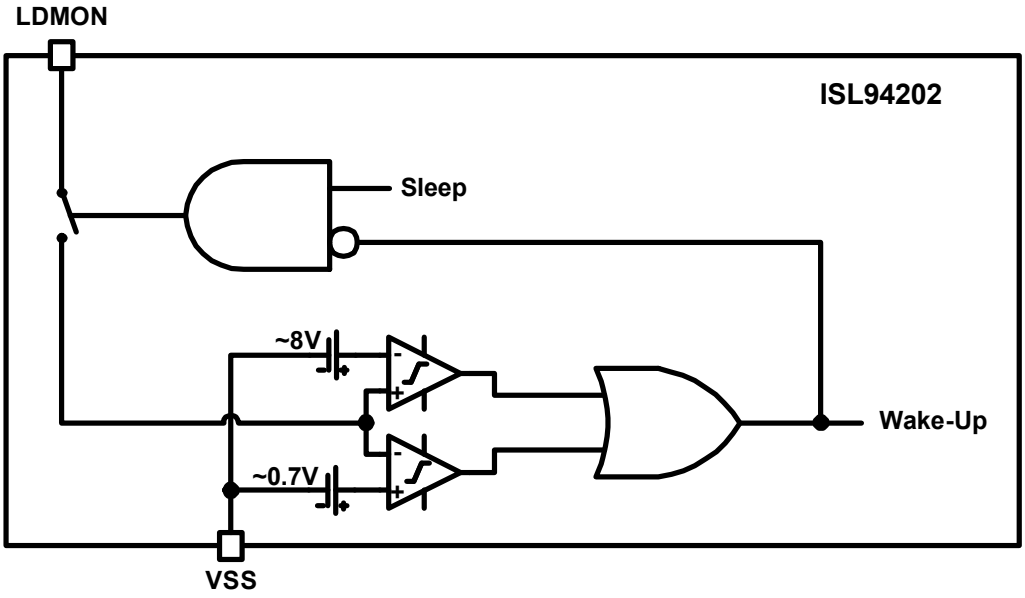

Figure 12. LDMON Wake Up

When a load is connected, it pulls the floating output node to ground. A 29.8kΩ resistor was used for the following example.

Figure 13 shows a load detection following a relatively long (>>50ms) period of Sleep. The initial detection is at t = 0 with the second one at ~140ms. Note V_{OUT} (PACK+ in Figure 3) remains below the load detection threshold during this period.

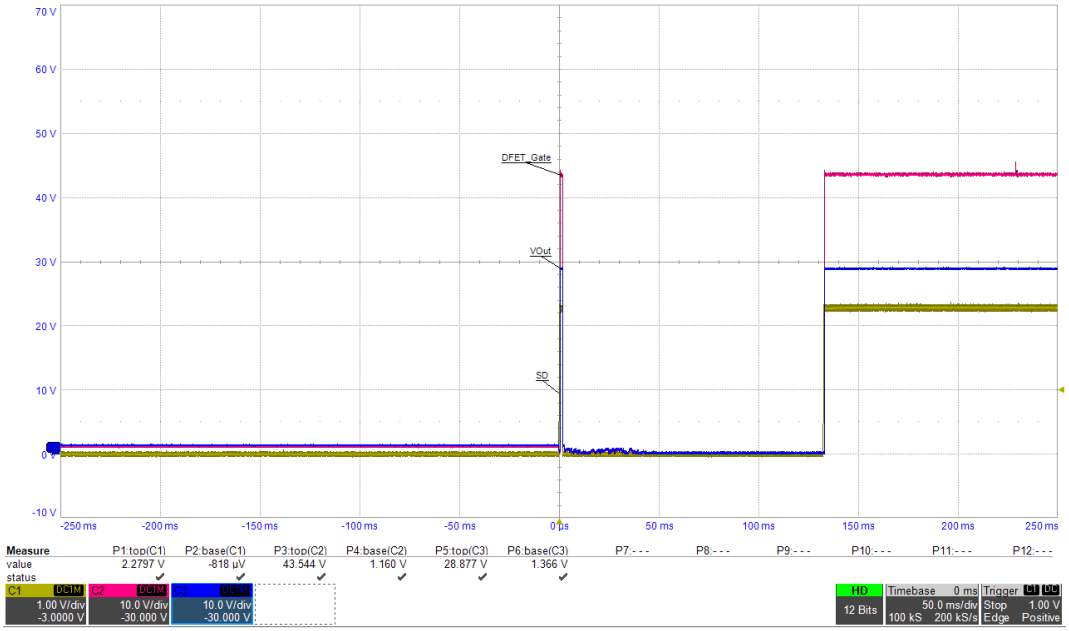

Figure 13. LDMON Detection (both)

Figure 14 is a detailed view of the first detection, V_{OUT} drops below the load detection threshold at t = 0. When this happens $\overline{SD}$ releases, the power FETs are enabled and V_{OUT} rises to the battery pack voltage. Less than 2ms later $\overline{SD}$ reasserts, Power FETs are disabled and V_{OUT} drops back below the load detection threshold.

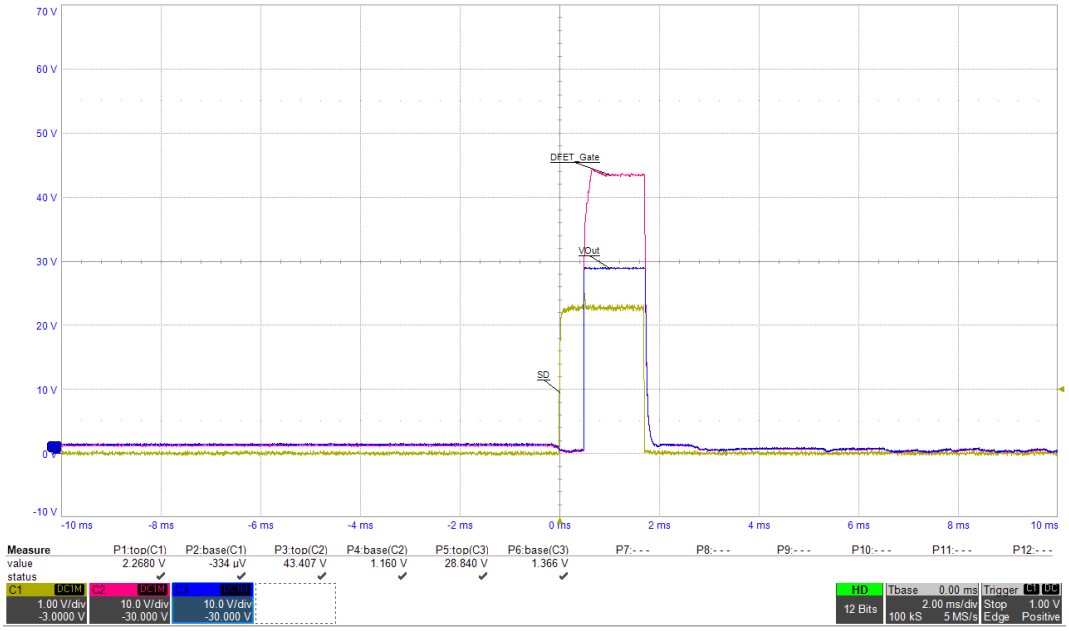

Figure 14. LDMON Detection (first)

4. Mixed Detections

The ISL94202 requires two consecutive detections to wake the device if it has been in Sleep >>50ms. It does not require two consecutive detections of the same type; this is an important feature in some applications. The most common mixed detection example is a discharged capacitor.

A discharged capacitor looks like a short to the detection circuits as can be seen in Figure 15 and Figure 16 at t = 0. This is a load detection because V_{OUT} is below the LDMON threshold. In this case, the power FETs are enabled long enough to charge the capacitor, then are shut off as in the other examples. The second detection is above the CHMON threshold and the device transitions from SLEEP to NORMAL Mode.

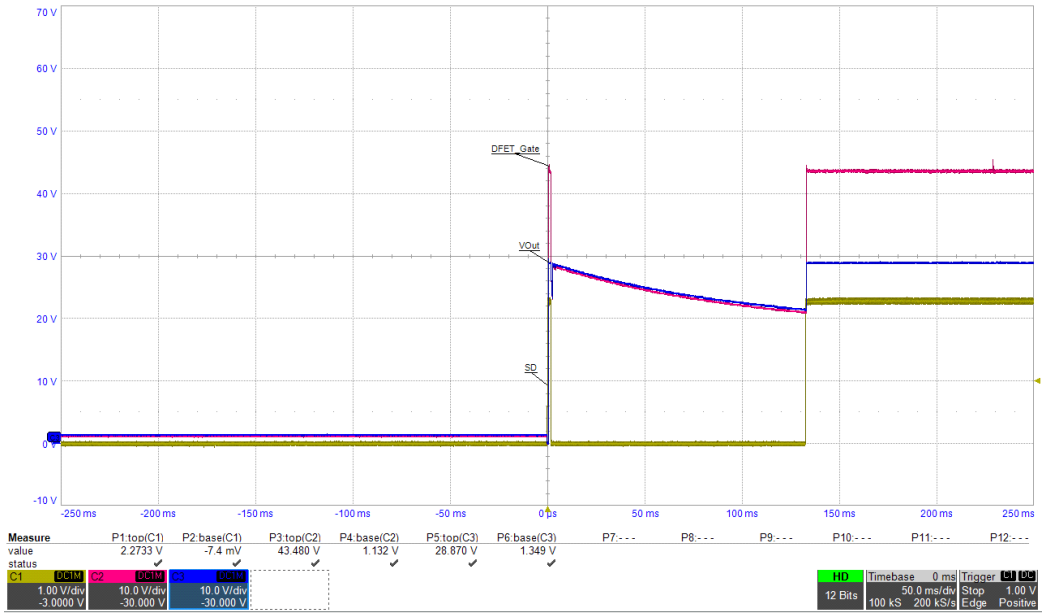

Figure 15. Discharged Cap (both)

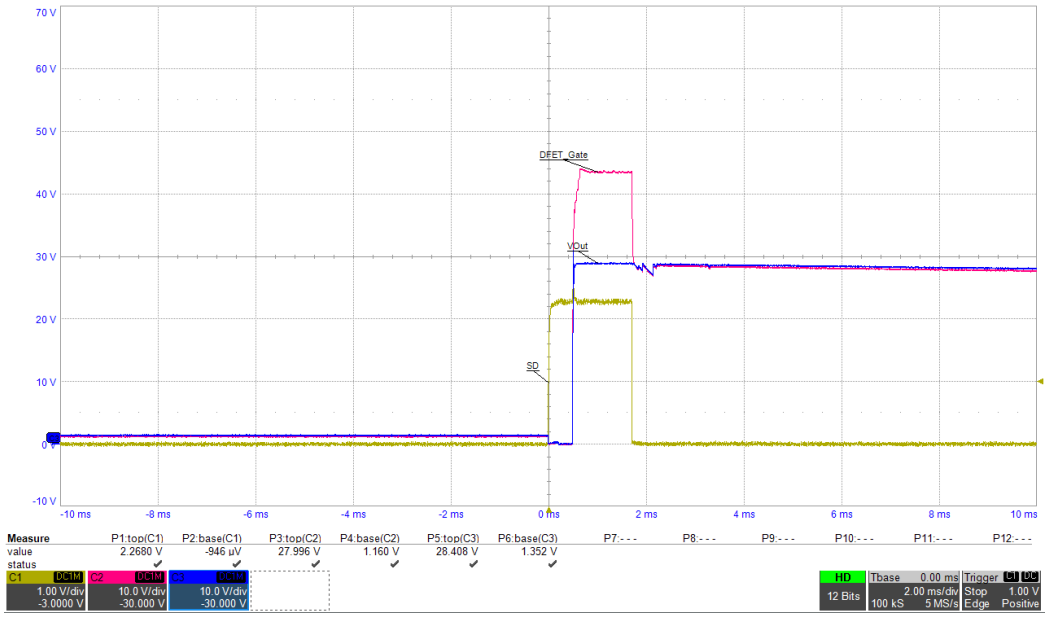

Figure 16. Discharged Cap (first)

5. Sleep Entry

The ISL94202 transitions to SLEEP Mode either by command or no detected current flow for a selected amount of time as described in the previous sections. The device remains in Sleep until either a load or charger is detected. The device waits 50ms following initial entry into Sleep before it enables the detection circuits. **Important:** If the voltage after the ~50ms delay seen at either CHMON or LDMON pins is not between ~0.7V and ~8V, the device does not stay in SLEEP Mode. If there is a large load capacitance, it may be necessary to partially discharge this capacitor before the device sleeps.

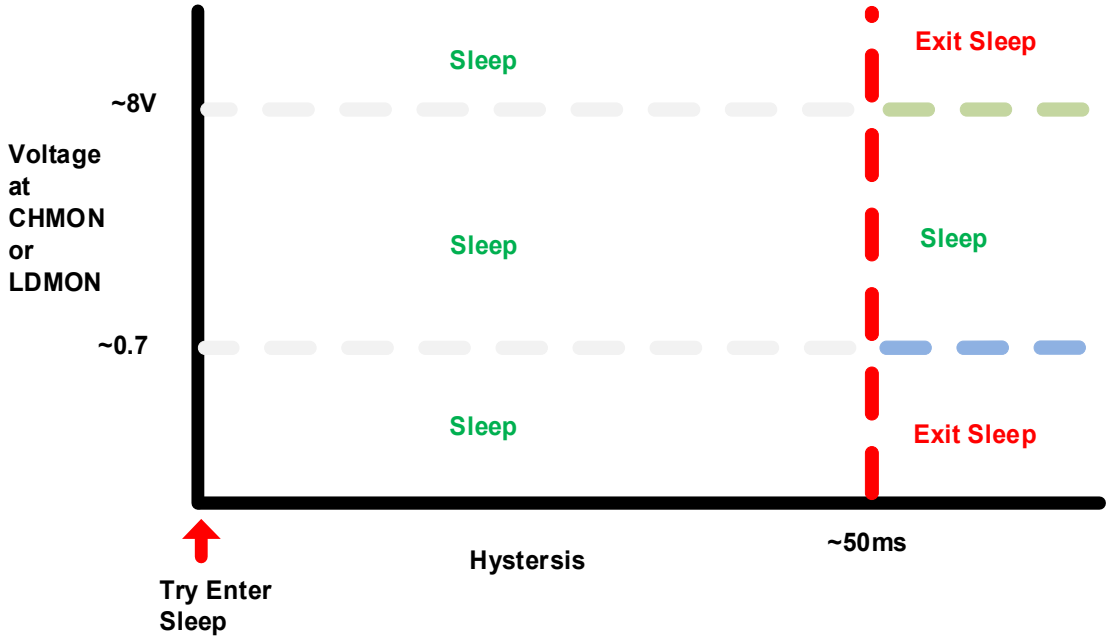

Figure 17. Sleep Qualifications

The following oscilloscope captures are provided to illustrate how the device performs under various load conditions.

Probe C1 monitors the output of the shutdown ($\overline{SD}$) pin and a falling edge is used to trigger the capture. This pin is pulled up to the device regulated voltage RGO and is Hi-z under normal operating conditions, it is pulled low to indicate the FETs are disabled and the device is in Sleep Mode.

C2 is connected to the DFET gate to show the power FETs turn off as the device attempts to enter SLEEP Mode.

C3 monitors the output node V_{OUT} (PACK+ in Figure 3), the node where the load, DFET source, LDMON and CHMON pins are tied.

Figure 18 is an example of successful entry into SLEEP Mode. At t = -50ms the device begins the transition by disabling the power FETs. Approximately 50ms later the $\overline{SD}$ pin asserts low and the first LDMON and CHMON pin voltage tests are executed by the device. With V_{OUT} at ~1.3V, the device determines there is no load or charger attached so it remains in Sleep.

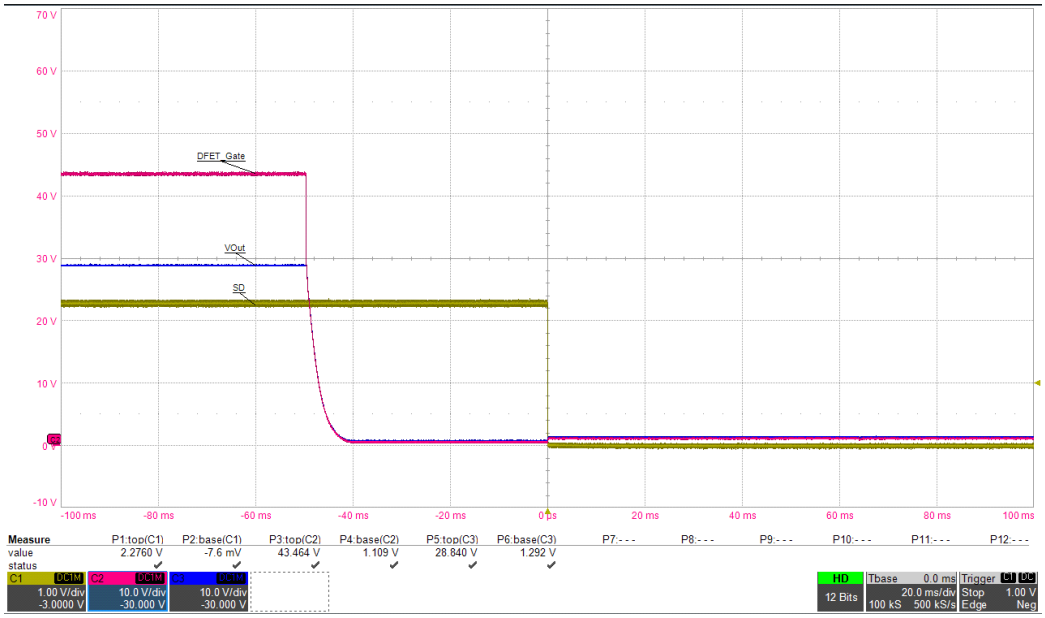

Figure 18. SLEEP Mode Entry

Figure 19 illustrates how the device behaves if a load is present when the device attempts Sleep. In this example, there is a purely resistive load of 29.8KΩ (~1mA at V_{BATT} = 30V). With a 0.001Ω current sense resistor this load current does not produce a detectable voltage across the sense resistor, therefore the device mode counters progressively step down through the modes to Sleep (t = -50ms). $\overline{SD}$ asserts low at t = 0 and the first LDMON and CHMON pin voltage tests are executed by the device. With V_{OUT} at 78mV, the device determines a load is attached so it exits Sleep and transitions to NORMAL Mode.

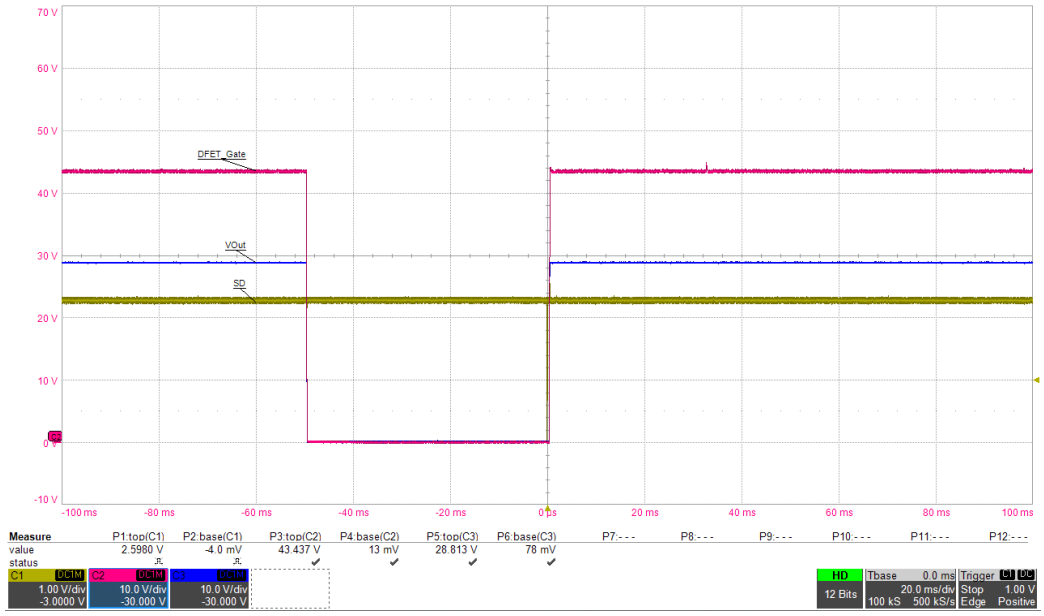

Figure 19. Sleep Failure (LDMON)

In this application, the load must be removed for the device to Sleep or an MCU can force the device to Sleep if the system includes one.

Figure 20 shows device behavior when attempting to enter Sleep if the load is purely capacitive. During the 50ms between DFET shutoff and $\overline{SD}$ assertion, the capacitive load has only discharged to ~16V. Because this voltage is well above the typical charger detection threshold, the device decides a charger is attached so it exits Sleep and transitions to NORMAL mode.

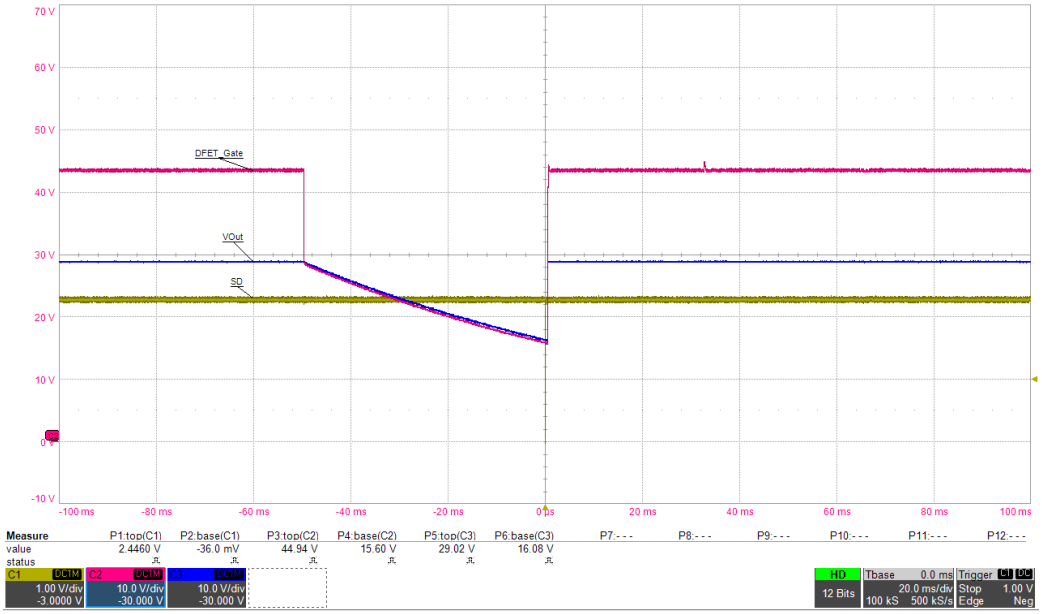

Figure 20. Sleep Failure (CHMON)

This case demonstrates that load must be discharged below the charger detection threshold for the device to remain in Sleep.

6. Revision History

Revision	Date	Description
1.00	Mar 10, 2022	Initial release.

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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