The P9222 wireless power receiver (WPC) is an integrated circuit (IC) consisting of multiple high power blocks along with noise sensitive circuits all controlled by a micro-processor. When implementing the circuit onto a printed circuit board (PCB) there are often some necessary tradeoffs associated with managing the critical current paths. In order to optimize the design, components should be placed based on circuit function to guarantee best performance when the schematic is implemented into a PCB layout. By following this guideline the P9222 circuitry should be placed and routed while occupying up to 37mm^2 of PCB area. Furthermore the thermal management of the IC is critical to the products overall performance and should be optimized while designing the PCB. At the time that the layout is started the following guidance should be used: Place the components in order of priority based on circuit function, route the power connections, route the noise sensitive connections and route the non-sensitive connections last. There are three main categories of circuitry, Power Circuits, Sensitive Circuits and Non-Sensitive Circuits.

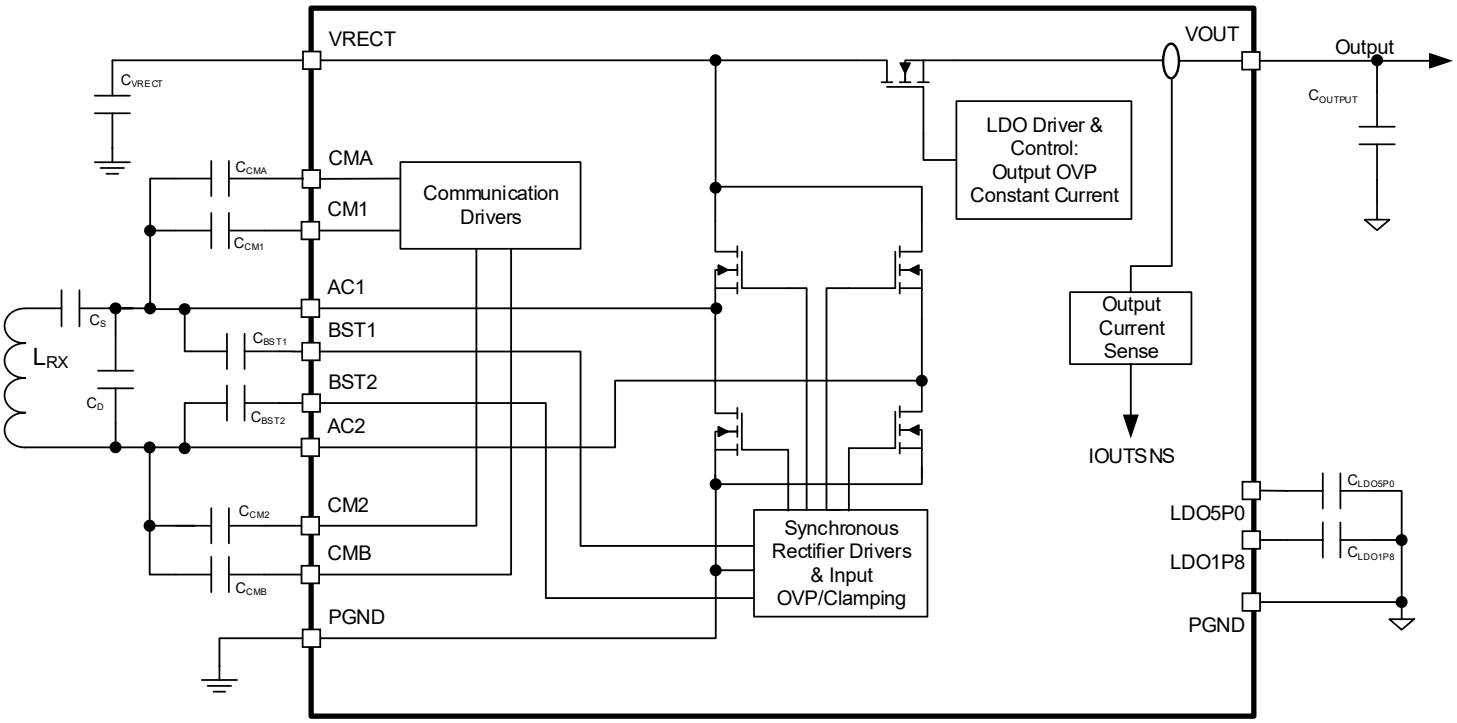
Key Points for Optimal Layout

- Route the power connections wide and on the same side of the PCB as the P9222 (≥ 2.5 mm).
- Use the first adjacent inner layer under the P9222 side of the board as a solid GND plane.
- Connect all 6 PGND pins to the GND plane(s) using vias-in-pad. Add a 'thermal tab' for the H-row GND pins.
- Avoid unnecessary layer transitions of the AC power connections (AC1, AC2, LC node, VRECT, and GND). Use 6 or more vias for all AC, V_{RECT}, and GND layer transitions.
- Place the P9222 toward the center of the board. Avoid placing along the PCB edge.
- Connect as much copper as possible to every pin of the P9222 even if they do not carry high current.
- Place in order: VRECT caps, LDO1P8 caps, BST caps, LDO5P0 caps, resonance caps (C_S, C_D), CMx caps, and VOUT capacitors; leave room to route.
- Use minimal trace-to-trace separation for all traces and planes connected to and within 0.127 mm of the P9222.
- Follow the placement and routing suggestions outlined in the remainder of this document.
- Use low ESR resonance capacitors (C_S/C_D) for the WPC LC tank (C0G preferred).

Rx Power Circuits

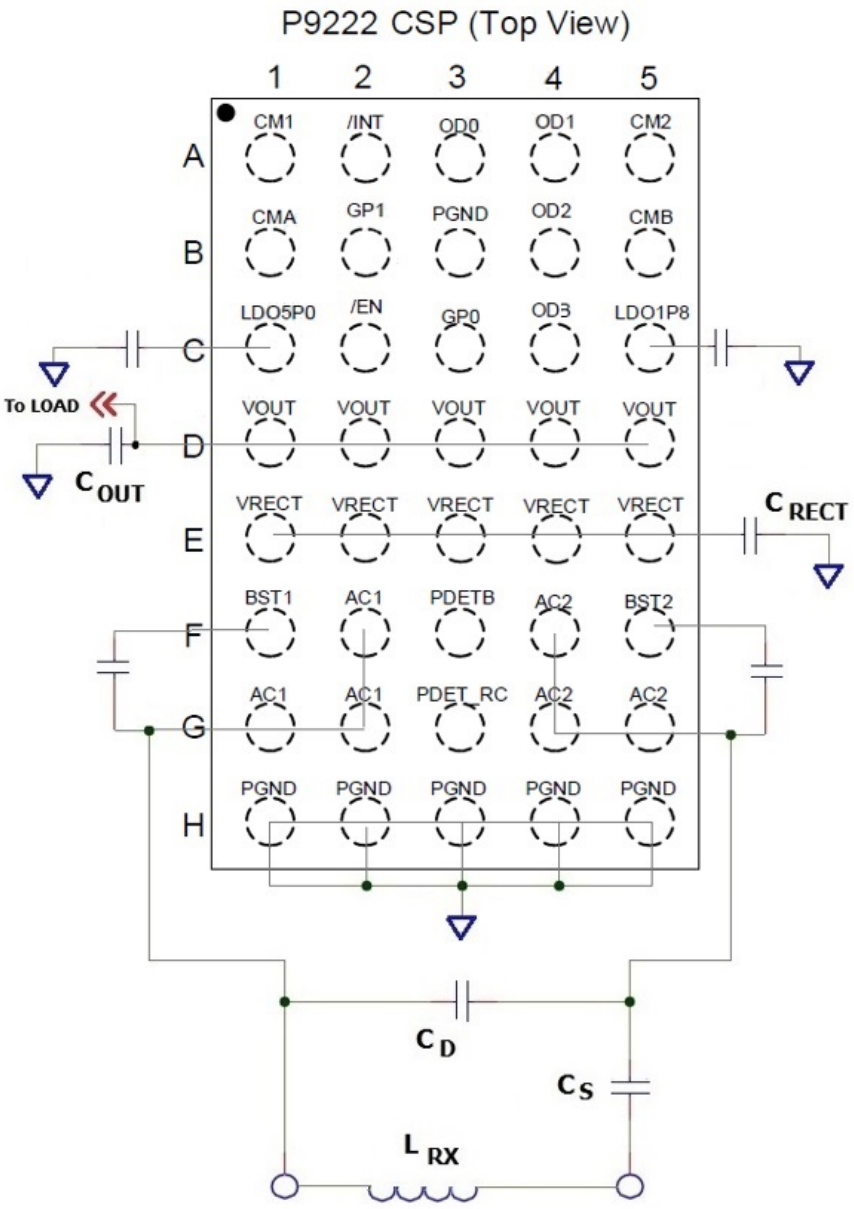
The main power circuits of the P9222 device are the resonance tank, the integrated synchronous bridge rectifier and the LDO linear regulators VOUT. Secondary power circuits are the BST and CM capacitors, and the LDO regulators LDO1P8 and LDO5P0.

Figure 1. P9222 Power Blocks



Considering mechanical requirements of the system under design it is suggested that as soon as the final shape of the production or development PCB has been determined and the power transfer coil connection point are chosen that the P9222 be placed onto the board as close to the center of the PCB as possible. With the WPC or wireless (L_{RX}) coil location determined and the P9222 placed (orientation should be determined based on the ability to route connections and place the necessary capacitors in the following order of priority: Rectifier (C_{RECT}), Bootstrap BST1/2, LDO1P8. WPC (Cs, Cd) resonance capacitors, LDO5P0, Communication CM1/2, VOUT capacitors. The main power current path is considered the connection from the Rx resonance tank to the AC1 and AC2 pins, PGND, VRECT, VOUT, CMx capacitor connections. The optimal P9222 orientation relative to the coil and output connector physical locations are presented in the following image. The P9222 orientation should be such that the PGND H-row faces the connectors for the Rx coil. If possible, place the VOUT capacitors on the side of the P9222 closest to the DC load. VOUT and VRECT capacitors must be placed next the respective pins and be placed near each other (VOUT caps together and VRECT caps together). It is suggested to place VOUT and VRECT capacitors on opposite sides of the P9222, but may be on the same side of the P9222:

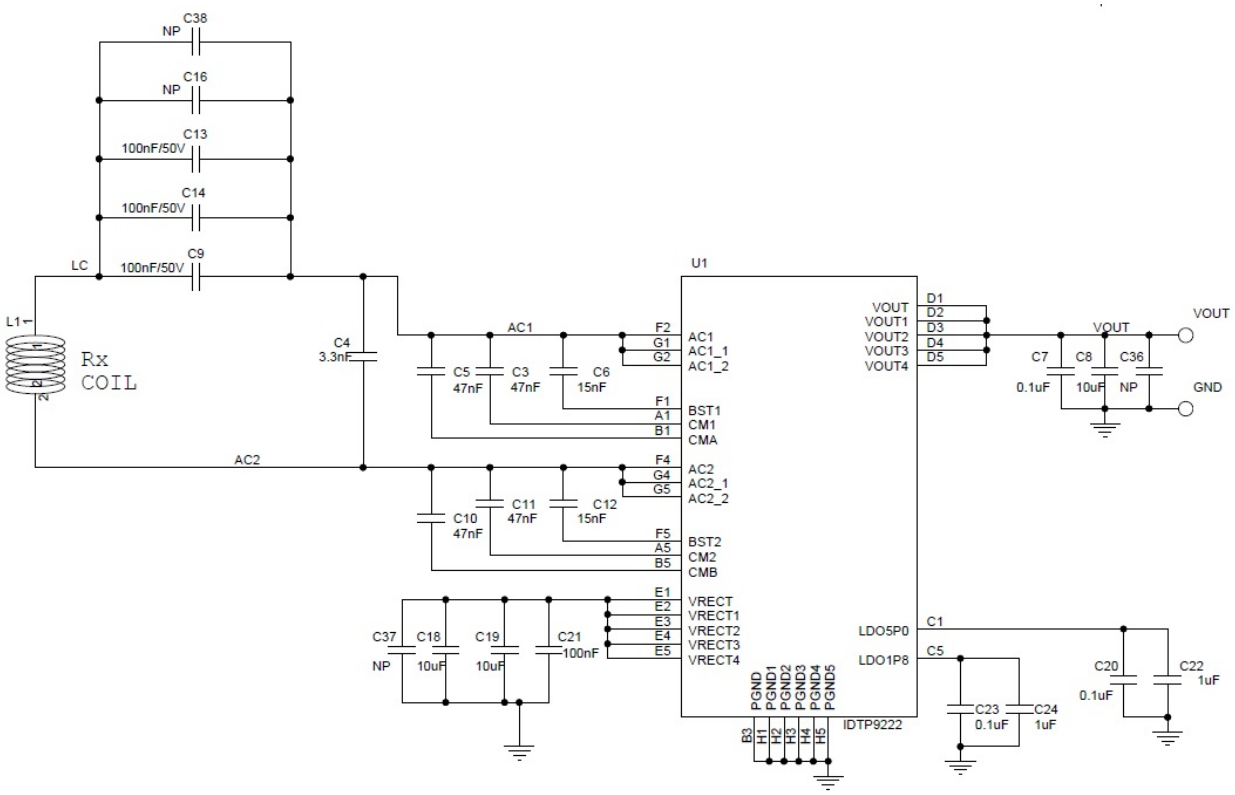
Figure 2. P9222 CSP orientation based on coil connector location and placement for critical components (Not all necessary connections are shown in this figure; refer to the P9222 datasheet Typical Application Drawing for a complete diagram of connections). Trace widths not to scale.



Power Schematic and Layout Examples

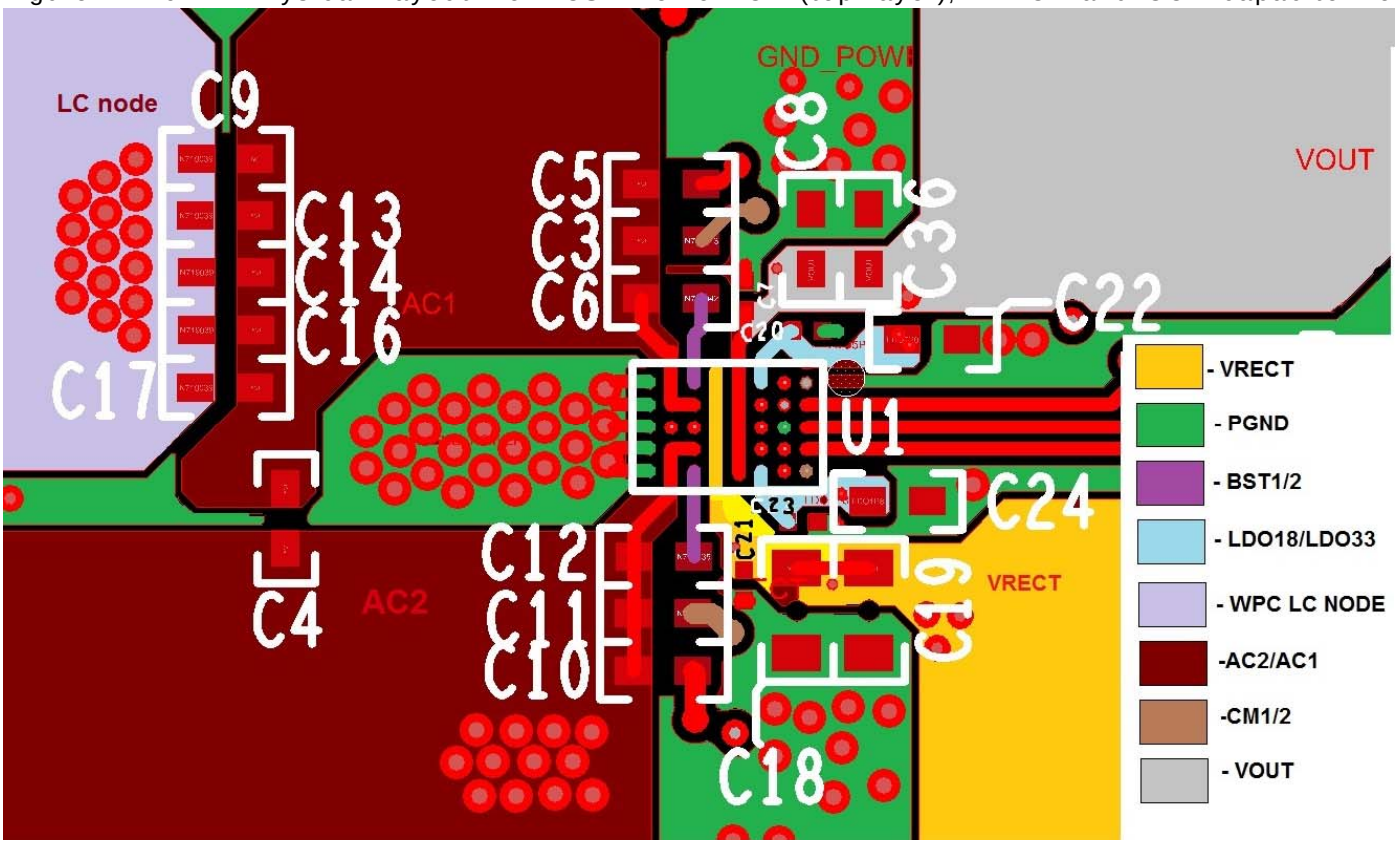
Place the VRECT output capacitors first and adjacent to the P9222 (C21,C19,C18), since they are subjected to high current charging and power transmission currents at twice the operating frequency of power transfer in addition to supplying DC current to the VOUT LDO. The power transfer switching results in dV/dt voltage steps high enough for consideration as noise generating signals at the AC1 and AC2 nodes and high di/dt current surges during normal operation. The ideal placement of the VRECT capacitors is to have them next to the VRECT pins (with all Vrect pins connected together and routed to the capacitors placed on one side of the IC) and with a direct 2nd layer connection to the H-row PGND pins. Below is a selection from the P9222 CSP DEMO PCB schematic portraying the Power Circuits and this figure will be used for reference:

Figure 3. P9222 Power Section, CSP DEMO Board Schematic (Not all connections are shown in this figure, refer to the P9222 datasheet Pin Description for the complete list of pins and recommended connections).



In the following top layer layout image the placement of the VRECT capacitors (C21,C19,C18) happens first and these are the most critical components. Then the LDO1P8 (C23, C24) capacitors should be placed next to the LDO1P8 pin. Next place the BST1/2 capacitors (C6, C12) while leaving room for the AC1 and AC2 connections to be routed. Then the LDO5P0 bypass capacitors (C20, C22) and the WPC resonance capacitors (C9, C13, C14, C16, C38) followed by the WPC communication capacitors (C3, C11, capacitors C5 and C10 are only necessary for Airfuel operation). Next the VOUT bypass capacitors (C7, C8) should be placed. Placing the above listed parts in the order they are mentioned and close to the P9222 while allowing room for routing is critical for optimal performance. It can reduce noise to add a small 0201 10 nF to 0.1 uF capacitor from each regulator (VRECT, LDO1P8, LDO5P0, VOUT) to PGND if the package is physically smaller and the lower value capacitor is placed first and closest to the P9222. It is important to keep the area of the current loop that conducts the AC current from the synchronous bridge rectifier to the VRECT capacitors and PGND (H-row) to a minimum in order to keep ripple voltages and GND bounce minimized. In the reference layout, the GND current traverses from the VRECT capacitor GND plates to a solid GND plane by using many vias spread apart slightly to allow conduction between vias on all layers. The PGND pins on the H-row of the device should all have vias-in-pad to a solid GND plane and additional copper is recommended to create a 'thermal tab' filled with vias to transfer heat from the IC to the PCB. The copper planes should be as wide as possible for the connections for VRECT from the IC to the capacitors and back to PGND. The reason for the number of capacitors is to maintain the necessary amount of effective capacitance when 4-10 V of DC bias is applied across the VRECT capacitors (see DC-bias characteristics of selected capacitors and compare with components used in the reference design when substituting).

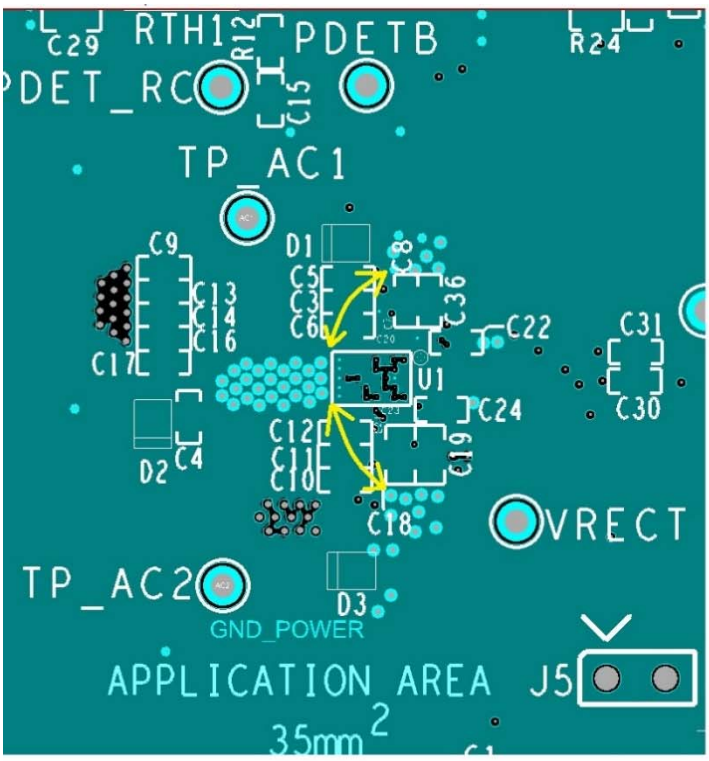
Figure 4. P9222 Physical Layout from CSP Demo PCB (top layer), VRECT and OUT capacitor focus



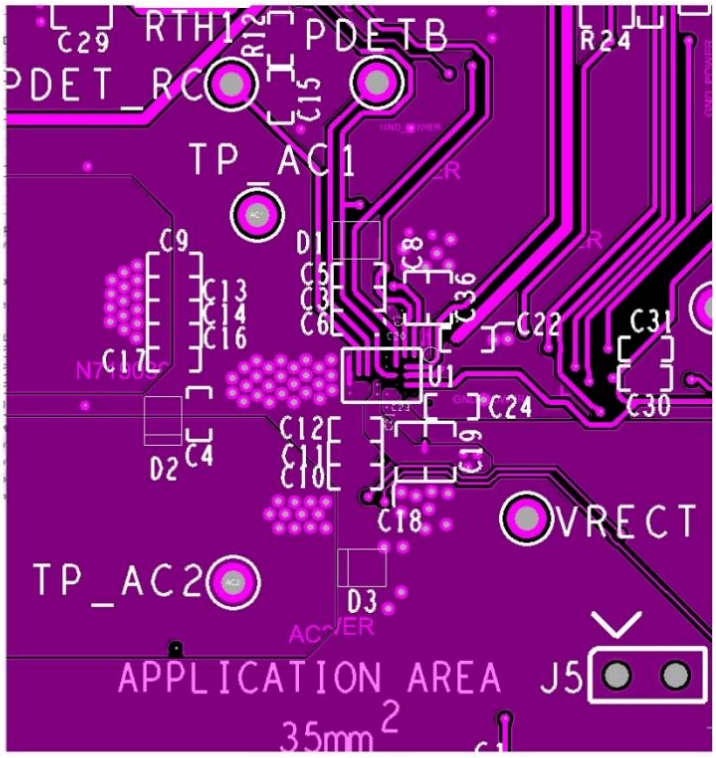
The copper shape with 26 vias directly connected to the PGND pins on the H-row found to the left of the P9222 (U1) is used as a 'Thermal Tab' and is an important connection and layout improvement because it assists with current conduction and substantially improves the IC thermal performance. The H-Row GND pins must utilize vias-in-pad for as many of the PGND pins as possible and the 'thermal tab' is highly recommended for all layouts. For best thermal performance multiple GND planes are recommended and connections should be direct and not thermally relieved. Additional thermal performance improvements can be made by connecting large copper planes to the power pins and all component side connections to the P9222 device (such as the rows 1 and 5; columns A and H pins) and by selecting Class-I dielectric capacitors or the low ESR components. C0G capacitors will offer the highest performance and are recommended for the WPC resonance circuit. Due to size and cost constraints X7R and X5R class II dielectric capacitors may be used for all components, but low ESR components should be identified and utilized. Since all of the load current and the current required to charge the VRECT/VOUT capacitors and charge the battery flows through the resonance capacitors, the heat developed within the resonance capacitors should be given opportunity to spread into large copper planes. Higher voltage ratings are recommended because higher rated components tend to have lower derating and dielectric loss factors at the working voltage which typically results in lower operating temperatures.

Effort should be made to keep the first PCB layer under the P9222 free from unnecessary connections and a solid GND plane is preferred. Since it is often impractical to not have connections on adjacent inner layers, it is recommended to have connections on the other PCB layers concentrated a single layer to improve heat transfer. By keeping multiple inner layers free of traces that isolate the shapes the copper can be more continuous and will be more suitable for heat absorption and distribution.

Figure 5. IDTP9222 Physical Layout from Demo PCB 2nd layer (MID1) – Solid GND plane and 3rd layer (MID2) GND/POWER plane after routing signal traces.



2nd Layer (MID1) - Solid GND plane recommended
PGND pins and Vrect/VOUT caps GND directly connected



3rd Layer (MID2) - Used for signal routing and planes for heat dissipation

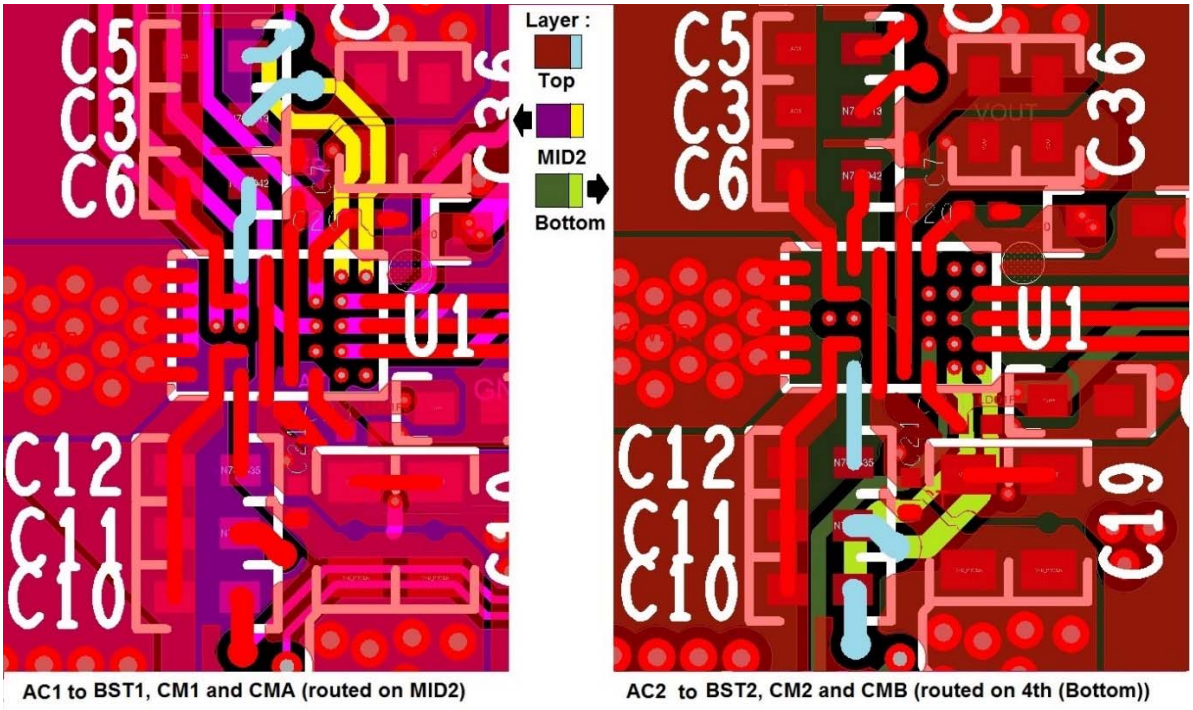
It is critical to the performance that the PGND connections from the PGND pins to the VRECT capacitor GND and VOUT GND be made using many vias (at least 8 for every layer transition and connection). The GND connection should be completed using wide copper near the P9222 and the GND plane width should be maintained leading to the load. In the above 2nd layer image from the DEMO board, the layer is solid GND plane and the GND connections for the PGND pins, VRECT capacitors and VOUT capacitors are direct and uninterrupted. On the 3rd layer, the majority of the signals are routed and copper planes are added in parallel with other layers for improved heat dissipation and lower impedance.

The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air and other objects; however, it should be realized that spreading the heat into internal layers is also effective at lowering the operating temperature. Since the thickness of most PCBs allow the thermal resistance between layers (through the FR-4 material) to be minimized all layers can effectively transfer heat along the z-axis. Internal layers are able to effectively spread heat horizontally when they are not interrupted by traces and through-holes along their surface. An ideal layout will result in the entire PCB being close to the same temperature; however, in order to obtain this result, all board layers should have planes that are fairly continuous and in direct contact with P9222 vias-in-pad or other heat sources. A single internal layer should be selected for routing the majority of the inner row/column pins to the rest of the PCB. The 3rd layer is preferred for this purpose. The required nodes to connect heat spreading planes to are PGND, VRECT, AC1, AC2, and VOUT; all other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9222.

BST and Communication Capacitors

As discussed, after the VRECT and LDO1P8/LDO5P0 capacitors are placed the BST and the CM (capacitive modulation) components should be placed. In Figure 6, the BST capacitors (C6, C12) are placed adjacent to the P9222 while leaving room for the AC1 and AC2 nodes to be routed in from the resonance tank. Then the CM1, CM2, capacitors should be placed next to the AC1, AC2 nodes near the P9222 and have fairly direct connections to the respective pins (route 0.3 to 0.5 mm wide). The CM capacitors can also be placed next to the respective pin used for the modulation pulse. When routing begins, it is recommended to route the BST capacitors on the same side of the PCB as the P9222 and use an inner layer to route to the CM pins as directly as possible. The BSTx and CMx connections are ok to route on inner layers of the PCB but should be located on layers close to the same side of the PCB as the P9222 (recommended to be within 3 layers of the component side).

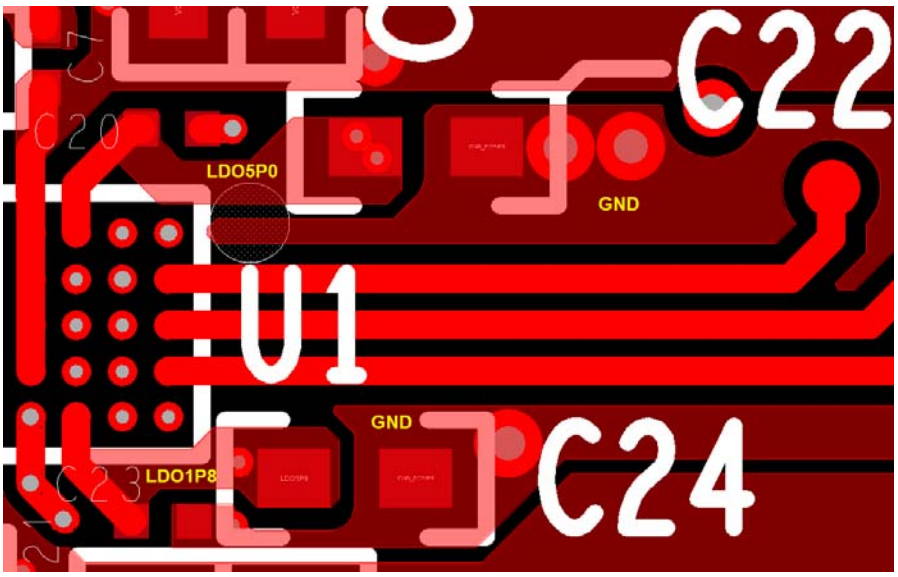
Figure 6. BST and Communication Capacitors



LDO1P8 and LDO5P0 Capacitors

The LDO1P8 (C23, C24) capacitors are used to stabilize the P9222 internal voltage supply for the ARM-M0 processor and provide stable output power capable of supporting light external loads (<10mA). This capacitor must be located close to the P9222. Optimal placement is directly next to the respective pins of the IC as shown in Figure 7. Then the LDO5P0 (C20, C22) capacitors should be placed next to the respective pins. In order to leave room for additional pins to be routed away from the P9222, the LDO GND connection is routed to the PGND pin on the P9222 side of the PCB and the GND via is placed next to the respective capacitor GND pin. It is recommended for electrical noise reduction to use the small 0201 10 nF to 0.1 uF capacitor from each regulator (LDO1P8, LDO5P0) to PGND. This additional capacitor is most beneficial when the package is physically smaller and the lower value capacitor is placed first and closest to the P9222 compared to the higher capacitance decoupling capacitors C22 and C24.

Figure 7. LDO1P8 and LDO5P0 capacitors placed next to P9222.



The following table should be used for guidance regarding minimum trace widths to use when routing the listed nets needed by the P9222:

Table 1- Minimum Trace width routing Guide

Name	PCB Pattern Width (mm (mils))
VOUT	1.0 (less than 50 squares[1]) (40)
VRECT	2.0 (expand rapidly from pins to capacitors) (80)
AC1, AC2	2.54 (100)
BST1, BST2	0.3 (12)
CMA1, CMA2, CMB1, CMB2	0.25 (10)
LDO5P0	0.2 (8)
LDO1P8*	0.25 (less than 30 squares[1]) (10)
All GPx pins, ODx pins, /INT, /EN, and PDET_RC, PDETB	0.127 (5)

Optional Transient Voltage Suppressor Diodes (TVS) –

Transient Voltage Suppressor diodes can be added to the design from the AC1 and AC2 nodes to GND or from AC1 to AC2 to add additional protection from high energy surges which can result in elevated voltages on the AC and Vrect nodes of the P9222. These components are useful to rapidly limit incoming ESD surges or situations when the Tx incoming power exceeds the expected power and Vrect voltage rises above target and over 15V in less than 10µs to aid in voltage limiting the incoming AC waveforms in conjunction with the OVP power limiting circuitry. A balance between Reverse Standoff Voltage (VRWM), Clamping Voltage (VCL), Break-down Voltage (VBR) relative to the expected Vrect operating voltage Vrect (be sure minimum VBR is less than maximum operating Vrect value and that VCL is less than Vrect Absolute maximum voltage) should be reached. The following guidance should be used for the P9222 when selecting TVS diodes:

VRWM = 10 V max (< 5W) or 13 V max (> 5W)

VBR = 12 V min @ 5mA (< 5W) or 15 V max (> 5W)

VCL = 18 V max @ 1App (< 5W) or 22 V max (> 5W)

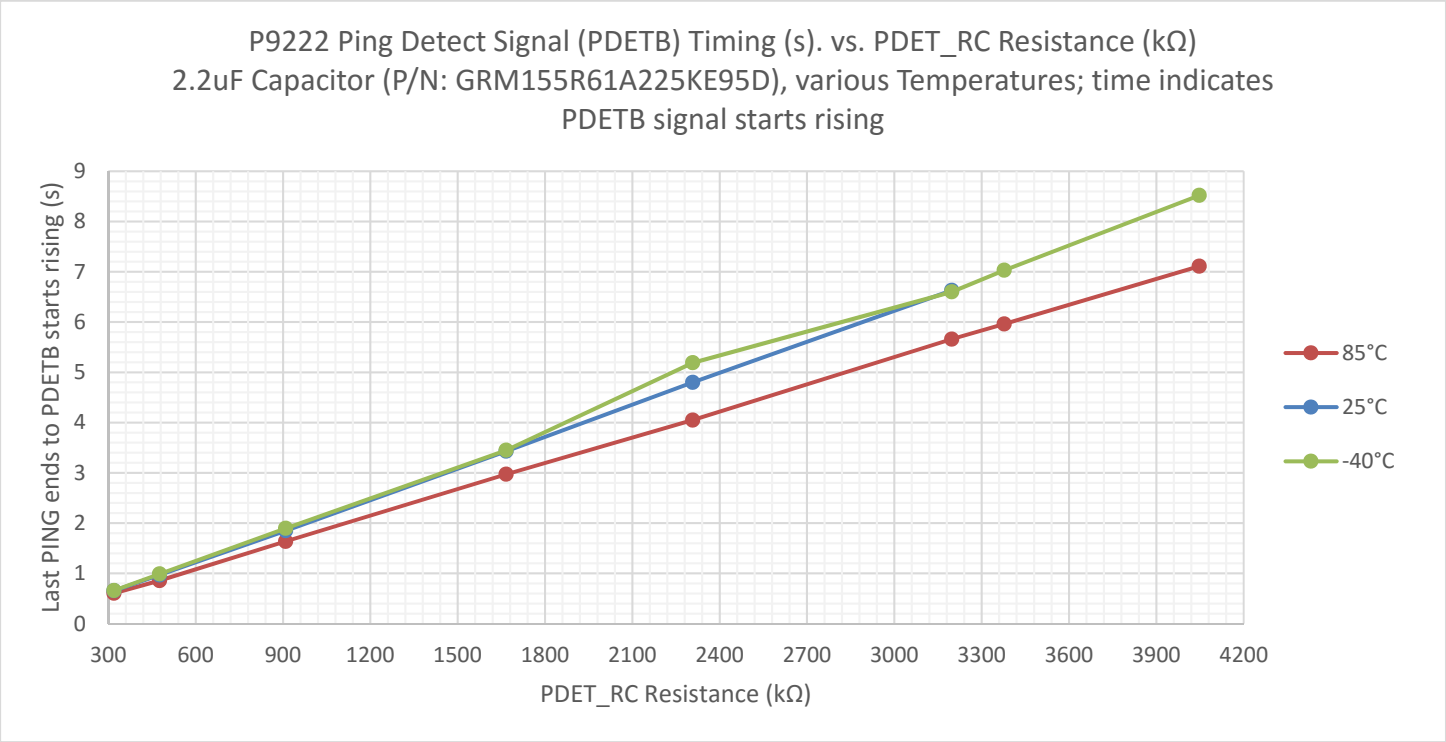
When TVS diodes are used, it is recommended to place them as close to the coil on the respective nodes as possible to shunt high voltages away from the P9222 device. Zener diodes can also be used to limit voltage levels and the zener voltage should be above the working voltage of the node and below the absolute maximum voltage of the pin connected to the node.

Sensitive Circuits

The sensitive circuits refer to noise sensitive circuits and they include the thermistor bypass capacitor, the PDET_RC node and other capacitors used to decouple noise (such as any level sensitive connections using the internal ADC). In order to optimize the signal to noise performance, it is suggested that the VOUT capacitors be placed on the side of the IC closest to any loads that will be applied to the VOUT regulator and the VRECT capacitors be placed on the opposite side of the IC from the VOUT capacitors. The Rectifier and resonance nodes generate the highest noise and are the frequencies that need to be filtered.

The Ping Detect feature (PDETB) relies on the RC time constant and decay of stored charge upon a capacitor. The RC connected to the PDET_RC pin should be selected based upon the expected ping time interval of the TX. To prevent the P9222 from waking the AP prematurely during Ping Detect mode the RC values should be selected to hold PDETB pin low until a few hundred milli-seconds after the expected Ping interval from the Tx. It is important to consider the DC bias impact on the selected capacitor because the reduction in effective capacitance caused by the DC bias will change the timing of the circuit. The following graph can be used as guidance to select the parallel resistor when using the specific capacitor listed:

Figure 8 - PDETB start rising time after Last PING using listed capacitor vs parallel resistance



The Ping Detect RC components should be placed near the P9222 but the routing and placement is not critical to performance. It is not recommended to use resistors greater than 4MΩ to avoid interference due to leakage from PCB cleaning or other contamination.

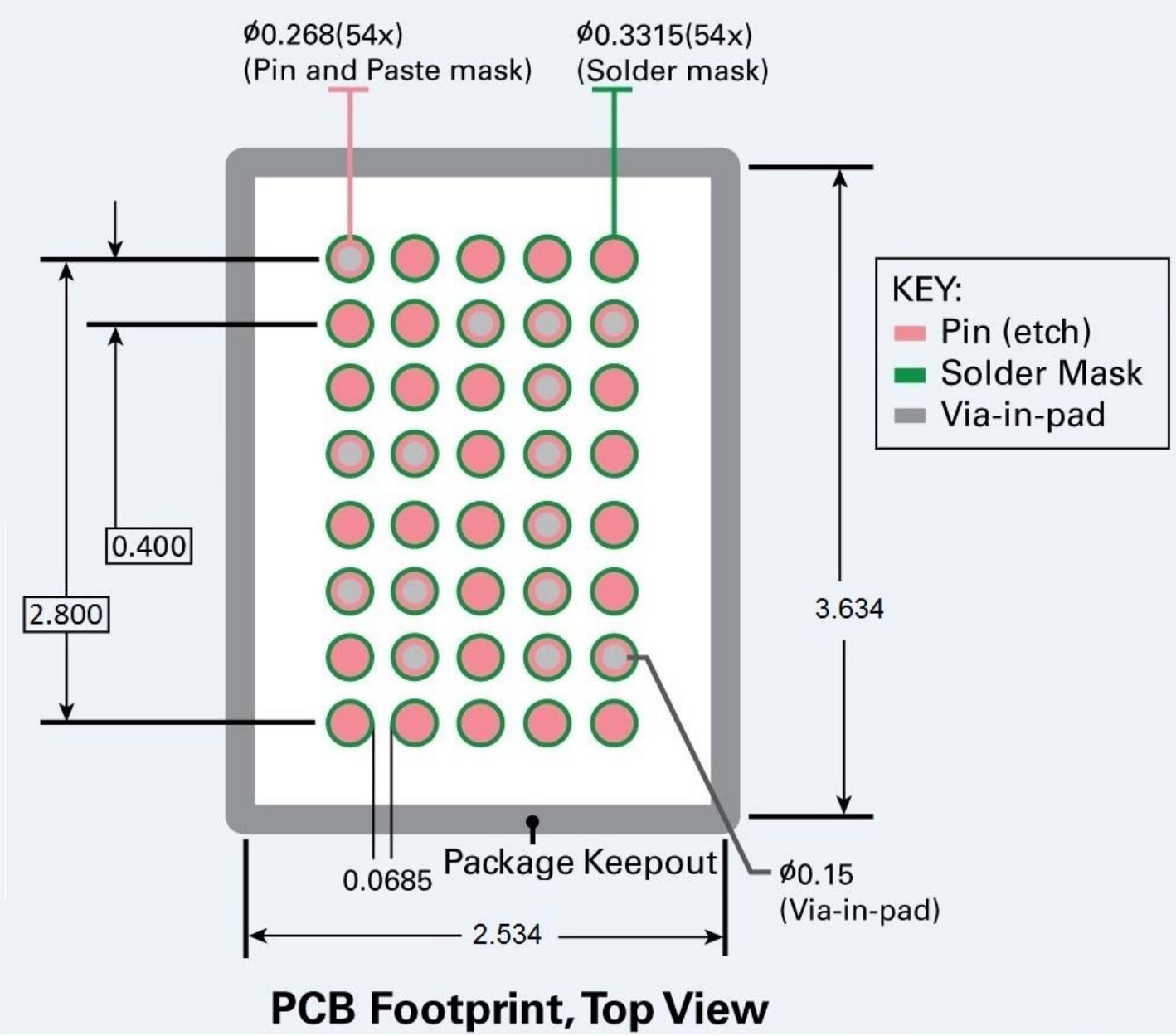
Non-Sensitive Circuits

The remaining components and pins that have not been mentioned are regarded as non-sensitive circuits and the placement and routing of these nodes is not considered critical to performance or functionality, they simply need to be present and properly connected. In most cases 0.127 mm (5 mm wide traces and any method of connectivity will suffice to complete the circuit.

PCB Footprint Design

The P9222 package is a fine pitch CSP device and the PCB footprint is an important part of production assembly yields. Improper footprint design can lead to solder shorts or open circuits. Poor PCB footprint design can also cause the performance to be degraded by limiting the robustness and diameter of the pin to board connections. In order to minimize the risk of such events, it is recommended that the PCB pin pads and via-in-pads be designed using the following guidance. Non-solder mask defined pins are recommended and solder paste should be applied with stencil openings of 0.127 – 0.268 mm (0.19 mm typical recommendation) based on stencil thickness and solder paste selected. Pin diameter should be set to 0.268 mm, solder mask should be 0.3315 mm and vias in pad should be 0.127 mm diameter holes.

Figure 9. P9222 CSP recommended PCB Footprint Design Dimensions.



Thermal Considerations

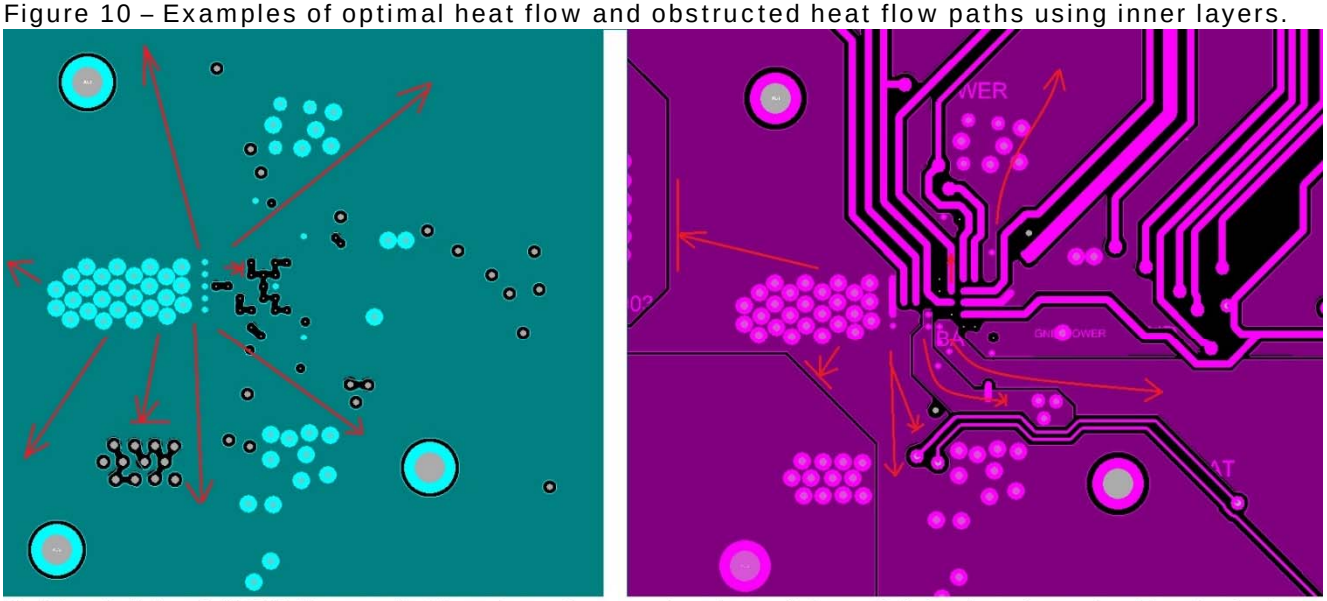
The temperature rise or thermal management of the P9222 PCB design is critical to performance and from the thermal perspective it is recommended to route the main power connections as wide as possible when connecting to the device and utilize the outer layer of the PCB for these connections. This allows for optimal electrical and thermal performance. Power connections to the P9222 using traces/planes should avoid multiple layer transitions (parallel planes are suggested when possible) in order to reduce voltage drops and thermal resistance caused by thin via walls. If these traces or planes must transfer between layers, it should be accomplished using multiple vias (6 or more) that have enough spacing such that they do not block the electrical current or heat path leading up to the via on either target layer. Furthermore, the Battery voltage and the state of charge (Constant Current mode is the state that results in the highest power consumption due to highest load current) impacts the die temperature due to power consumption. The Typical P9222 Power consumption can be estimated by the following equation and directly impact operating temperature:

P9222 Typical Power Consumption (W) = $(V_{RECT} – V_{OUT}) * I_{OUT} + 2\ RDS_{ON\_RECT}*(I_{OUT}) + I_{RECT\_IDDQ} * V_{RECT}$ Equation 1

The P9222 operating temperature will be influenced by the PCB design and power consumption. In order to minimize the IC temperature rise the following measures should be taken:

- Use Multiple GND planes directly connected to the 'Thermal Tab' added to the H-row of PGND pins.
- Use Thicker copper foil weights (1-oz minimum recommended, 2-oz preferred)
- Route wide copper planes/traces to every pin of the P9222, even for signals.
- Maximize the Copper area on the component side directly connected to P9222 pins.
- Use a thinner PCB (thinner PCBs will transfer heat through their volume more readily).
- Utilize surfaces on all layers with copper. Avoid areas of the PCB that have all copper removed by adding GND fill to all layers after routing.
- Route AC1, AC2, VRECT, VOUT on multiple layers with parallel planes connected together with multiple vias near the P9222.

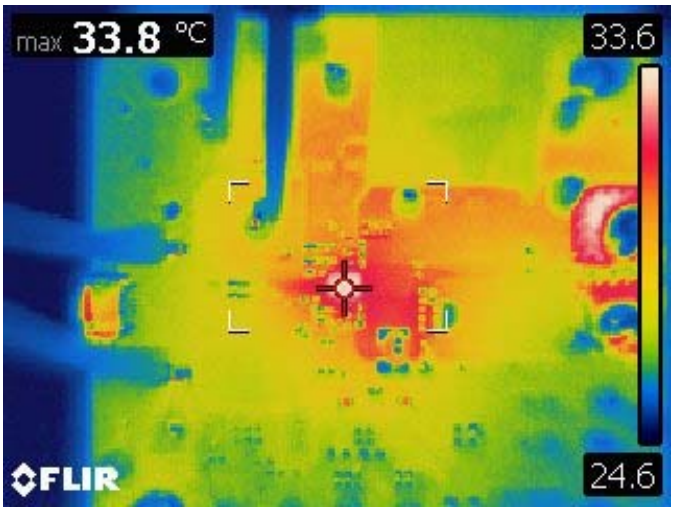
Figure 10 – Examples of optimal heat flow and obstructed heat flow paths using inner layers.



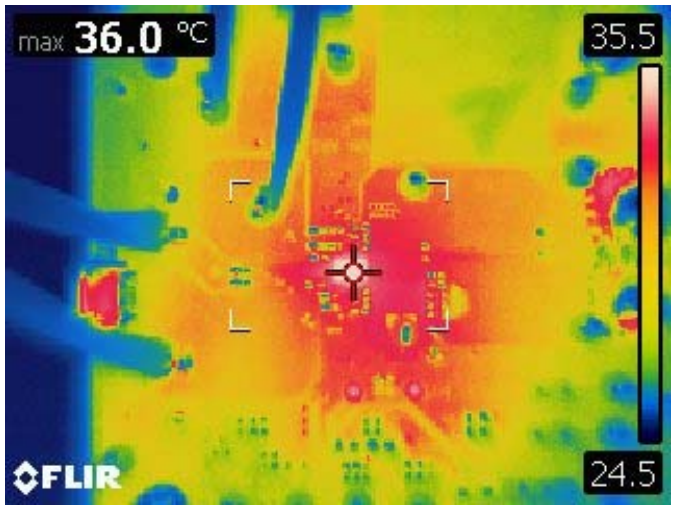
Heat Transfer Paths - Solid GND Plane, excellent thermal properties

Inner Layer with traces: Optimize shape sizes and and trace location to improve heat transfer paths

Figure 11 – Thermal Images from P9222 DEMO PCB (left BPP 5W mode, right EPP 10W mode)



BPP mode, 1A out @ 5V



EPP mode, 1A out @ 10V

Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected there are several steps that can be taken to reduce or eliminate the noise. The first priority should be identifying the source (i.e. the rectifier capacitors, the Rx coil ferrite, CM capacitors). Typically the rectifier capacitors are the components that generate the audible noise. The reason the noise is present and associated with the rectifier capacitors is due to the WPC communication signals being generating in the audible frequency range and the use of small form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses and this noise is amplified as it flexes the PCB. The primary solution to this issue is to use low-acoustic noise capacitors or tantalum capacitors. Alternately higher voltage rated components may have superior piezoelectric properties which can reduce the audible noise. Another solution is to placing the capacitors on both sides of the PCB (directly above and below each other), this counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

For any additional questions please refer them to your local Field Applications Engineer or our Marketing Department and they will be addressed as soon as possible.

Nicholaus Smith

Integrated Device Technology, Inc. - APD – Manager Applications Engineering

Revision History

Revision Date	Description of Change
November 20, 2017 V1.0	Initial release of AN-979: P9222 Wireless Power RxLayout Guide.
December 13, 2017, V1.1	Swapped OD2 pin with /INT pin.
January 17, 2018, V1.2	Swapped GP2 and /EN pin, changed pin C4 to OD3.

References

1. Spataro, Vincent. Counting squares: A method to quickly estimate PWB trace resistance. EDN Network. 2013 April 12. Web. 2016 June 3.

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