Application Note

DA9063L-A Power Management for TCC8030 Platform

AN-PM-134

Abstract

This application note describes using Dialog's flexible PMICs to produce a solution for Telechips TCC8030 (Dolphin+) platform.

Through a description of the general system configuration, power capabilities and requirements and an overview of the component interconnections, it will be shown that the DA9063L-A is highly suited as the power management system solution for Telechips TCC8030 platforms.

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DA9063L-A Power Management for TCC8030 Platform

1 Introduction

This document describes how to interconnect the DA9063L-A Power Management IC (PMIC) to the Telechips TCC8030 System on Chip (SoC). The DA9063L-A is a highly integrated chip that supports Dynamic Voltage Control (DVC) technology, enabling significant power saving: this feature supports the Dynamic Voltage and Frequency Scaling (DVFS) technology that is used by many processors.

As a result of its highly integrated features, the DA9063L-A PMIC significantly reduces the overall system cost and size compared to a discrete solution. This application note addresses only the power supply related features: discussion of other features of the optimized PMIC is beyond the scope of this document.

When VSYS is applied, the DA9063L-A automatically performs a power on/off sequence that is customized to the requirements of the TCC8030 SoC. A reset function is also de-asserted after completion of the power on sequence.

For further information on the DA9063L-A please refer to the datasheets available via your local Dialog sales office.

For information about Telechips TCC8030 SoC, please refer to Telechips website:

https://www.telechips.com/eng/product/automotive.php

2 Telechips TCC8030 SoC Description

Telechips TCC8030 is a platform for automotive systems with an SoC containing up to 7 processors (ARM®Cortex®-A7 Quad Core, ARM Cortex-A7 Single and ARM Cortex-M4) and Mali™-400 and GC300 GPUs.

Figure 1 shows a typical system block diagram of the Telechips TCC8030 application. The embedded cores require suitable power management that is readily achieved using the Dialog DA9063L-A.

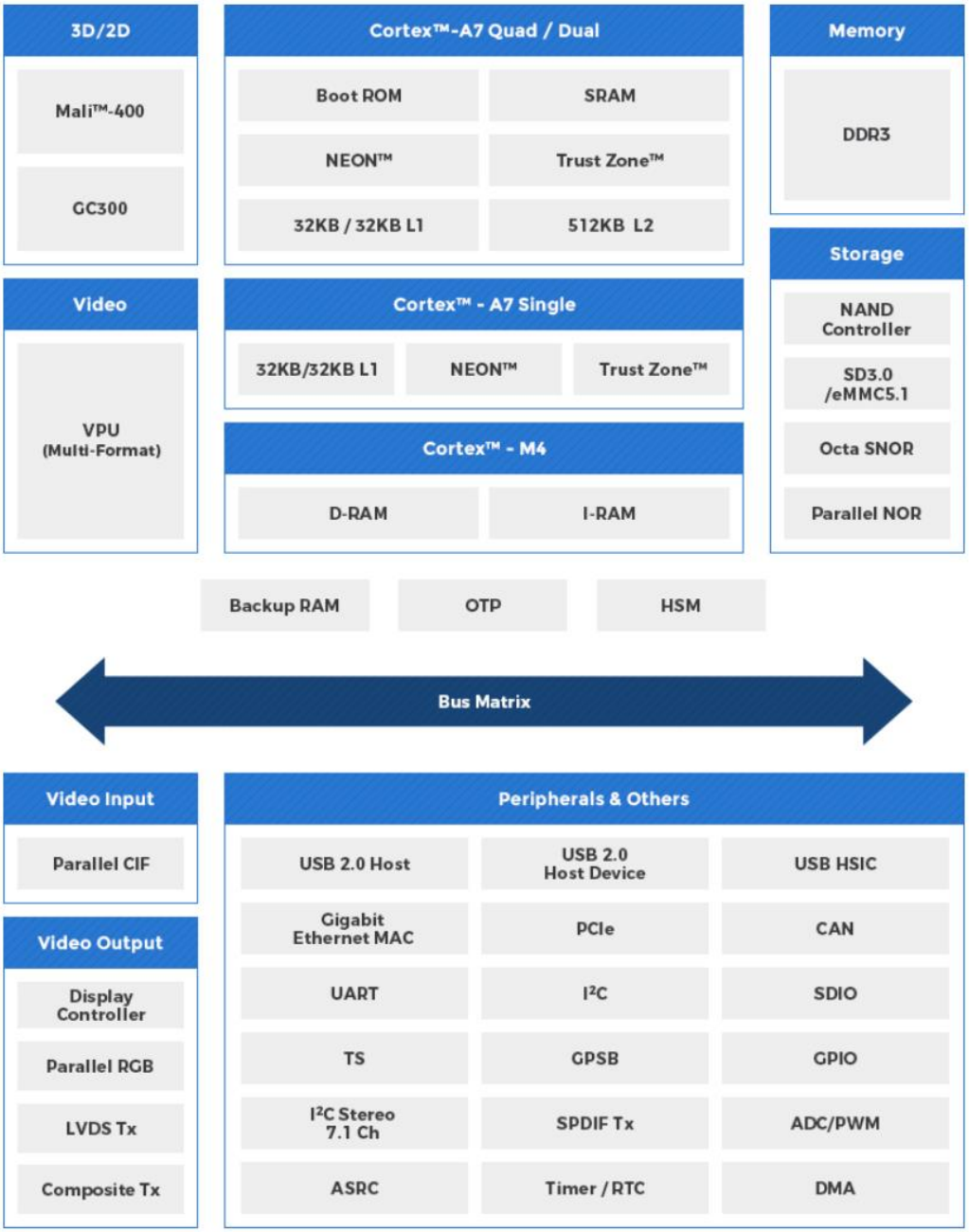


Figure 1: Telechips TCC8030 Block Diagram

3 DA9063L-A Description

The DA9063L-A, see Figure 2, is a high-current system PMIC suitable for dual- and quad-core processors that require up to 5 A core processor supply. The DA9063L-A contains:

- Six DC-DC buck converters designed to use small external 1 µH inductors, capable of supplying in total up to 12 A continuous output current (0.3 V to 3.3 V). The buck converters do not require external Schottky diodes; they dynamically optimize their efficiency depending on the load-current using an Automatic Sleep Mode (ASM) and incorporate pin and software controlled DVC to support processor load adaptive adjustment of the supply voltage. In addition BuckPro includes the facility to implement VTT memory bus termination if required.
- Five SmartMirror™ programmable low-dropout (LDO) regulators rated up to 300 mA. All support remote capacitor placement and can operate from low 1.5 V/1.8 V input supplies. This allows these LDOs to be cascaded with (in other words: supplied by) a suitable buck supply to improve overall system efficiency.
- DA9063L-A provides up to 16 flexible GPIO pins.

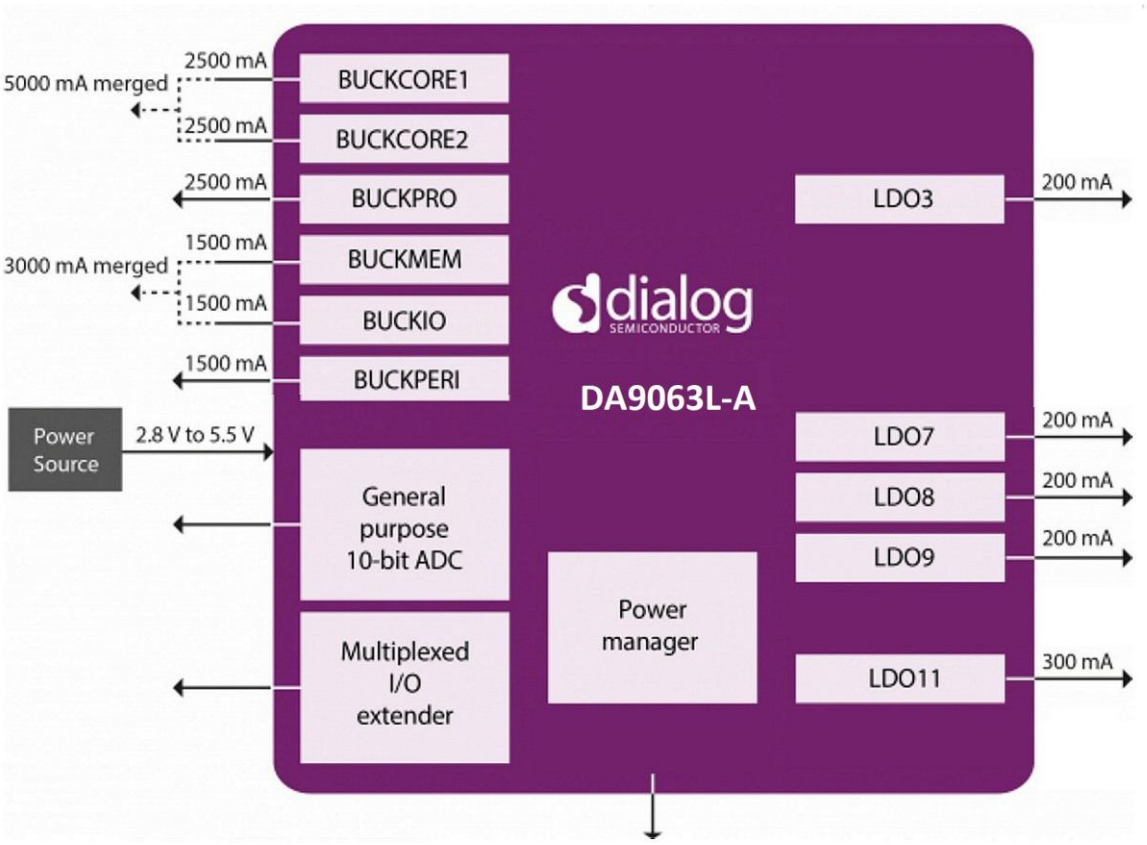


Figure 2: DA9063L-A System Block Diagram

4 TCC8030 SoC Power Requirements

Several power domains in the TCC8030 SoC platform require precise voltage management for reliable system operation:

Table 1: DA9063L-A Regulator Mappings to TCC8030 SoC

Dolphin+						DA9063L-A			Notes
Domain name	Voltage Range			Power on Slot	Power off Slot	Regulator	Vin Source	Vin Voltage (V)	
	Min	Typ	Max						
CPU_0P9V	0.86	0.92	0.95	3	4	BuckCore1	PMIC_VSYS	5.0V	
VCORE_0P8V	0.76	0.82	0.84	2	5	BuckCore2	PMIC_VSYS	5.0V	
CPU_0P8V	0.76	0.82	0.95	3	4	BuckPro	PMIC_VSYS	5.0V	
CPU_IO_1P8V	1.70	1.80	1.90	4	3	BuckMem	PMIC_VSYS	5.0V	
CPU_IO_3P3V	3.00	3.30	3.60	6	1	BuckIO	PMIC_VSYS	5.0V	
MEM_1P1V	1.05	1.12	1.16	6	1	BuckPeri	PMIC_VSYS	5.0V	
PERI_3P3V	1.7	1.8 / 3.3	3.60	6	1	LDO3	PMIC_VSYS	5.0V	
CPU_1P2V	1.14	1.20	1.26	5	2	LDO7	PMIC_VSYS	5.0V	
MEM_1P8V	1.70	1.80	1.90	5	2	LDO8	PMIC_VSYS	5.0V	Bypass Mode
PMIC_IO_3P3V	3.00	3.30	3.60	1	6	LDO9	PMIC_VSYS	5.0V	
eMMC_3V3	3.00	3.30	3.60	6	1	LDO11	PMIC_VSYS	5.0V	Bypass Mode

5 TCC8030 SoC Power Tree System Diagram

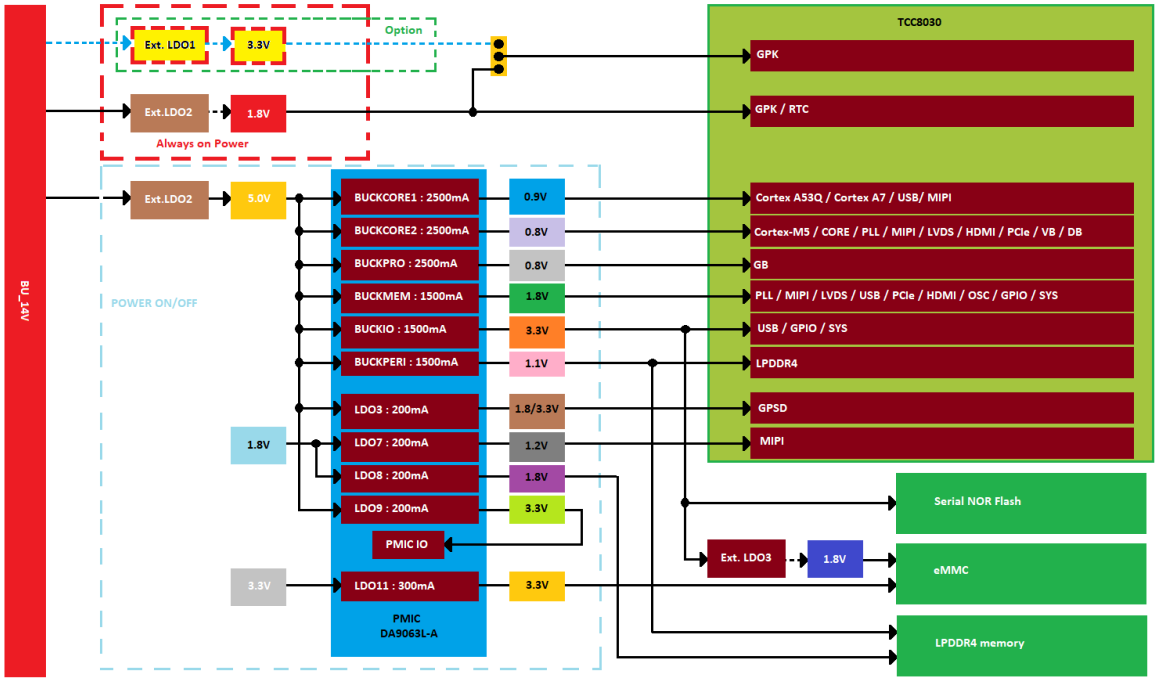


Figure 3: Telechips TCC8030 SoC and PMIC Interconnections

6 PMIC Schematic for TCC8030 Reference Board

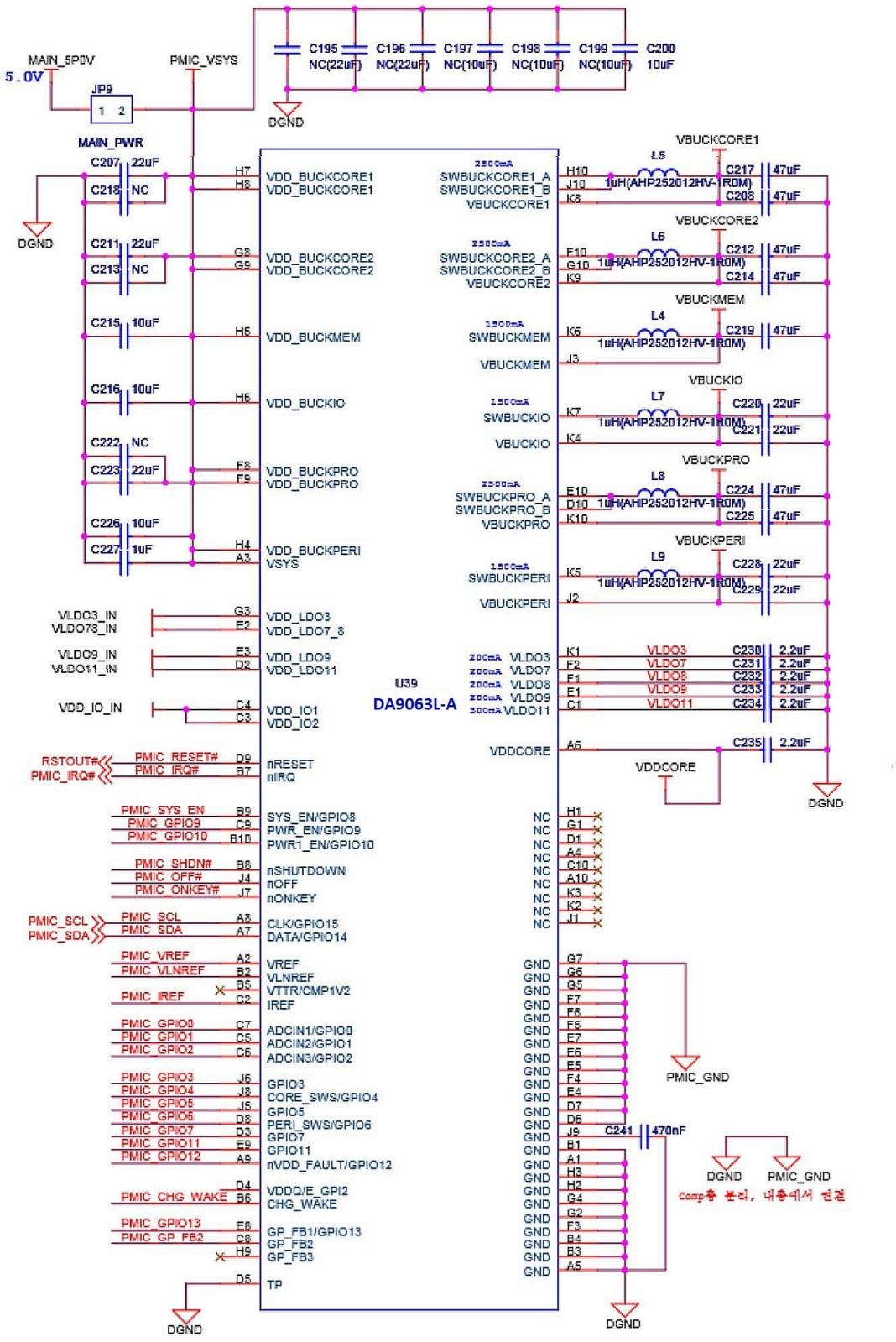


Figure 4: PMIC Schematic for TCC8030 Reference Board

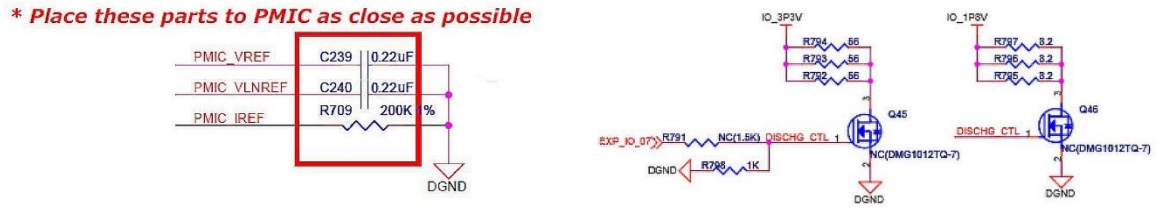


Figure 5: External Components for TCC8030 Reference Board

7 DA9063L-A Reference Design BOM

Table 2: Reference Design BOM

Reference	Value	Tolerance	Rating	Dielectric	Manufacturer	Part Number
C217, C208, C212, C214, C219, C224, C225	47u	+/-20 %	4 V	X5R		
L4, L5, L6, L7, L8, L9	1u	+/-20 %	3.5 A Isat		TDK	TFM252010 A-1R0M
C227	1u	+/-10 %	10 V	X5R		
C215, C216, C226	10u	+/-10 %	10 V	X7R		
C207, C211, C223	22u	+/-20 %	10 V	X5R		
C239	220n	+/-20 %	6.3 V	X5R		
C230, C231, C232, C233, C234, C235, C240	2u2	+/-20 %	6.3V	X5R		
R709	200k	+/-1 %	0.063 W			

8 DA9063L-A GPIO Functions for TCC8030

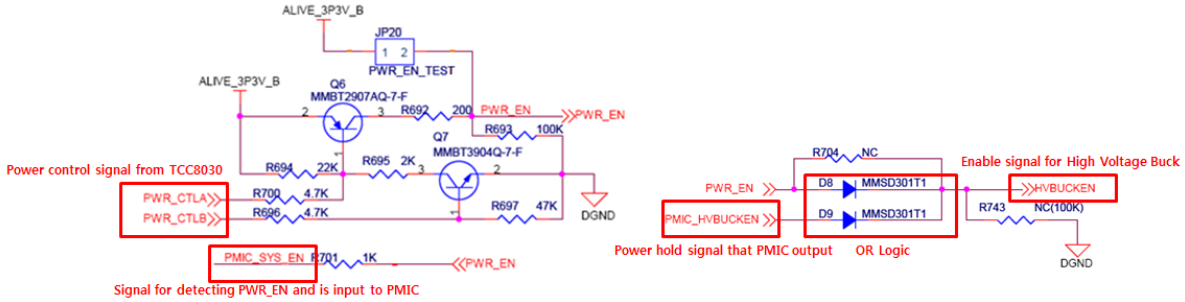
Table 3: DA9063L-A

Name	In/Out	EVB Function	Description
PMIC_GPIO0	O	DXB2_RST#	Can be used for other function
PMIC_GPIO1	O	DXB_PD1	Can be used for other function
PMIC_GPIO2	O	HVBUCK_EN	Recommended for power sequence – Note 1
PMIC_GPIO3	O	DXB_ON	Can be used for other function
PMIC_GPIO4	O	USB30_PWR_CTL	Can be used for other function
PMIC_GPIO5	O	USB20H_PWR_CTL	Can be used for other function
PMIC_GPIO6	O	USBOTG_PWR_CTL	Can be used for other function
PMIC_GPIO7	O	DISCHG_CTL	Must be used for discharging function. Leave unconnected if not used. – Note 2
PMIC_GPIO8	1	PWR_EN_DET	Recommended for power sequence – Note 1
PMIC_GPIO9	0	SYS_PWR_EN	Recommended for power sequence. This signal is included in the power sequence and used to enable power for peripheral device.
PMIC_GPIO10	0	DISP3_LCD_ON	Can be used for other function
PMIC_GPIO11	0	DXB_PD0	Can be used for other function
PMIC_GPIO12	0	DXB0_RST# / XM_RESET#	Can be used for other function
PMIC_GPIO13	0	DXB1_RST# / XM_SHDN	Can be used for other function

Note 1 Refer to Section 9: Power On/Off Sequence for TCC8030 Based on Power On/Off Sequence for TCC8030 Based on DA9063L-A.

Note 2 Refer to Section 10: PMIC GPIO7 Setting for Discharging Function.

9 Power On/Off Sequence for TCC8030 Based on DA9063L-A



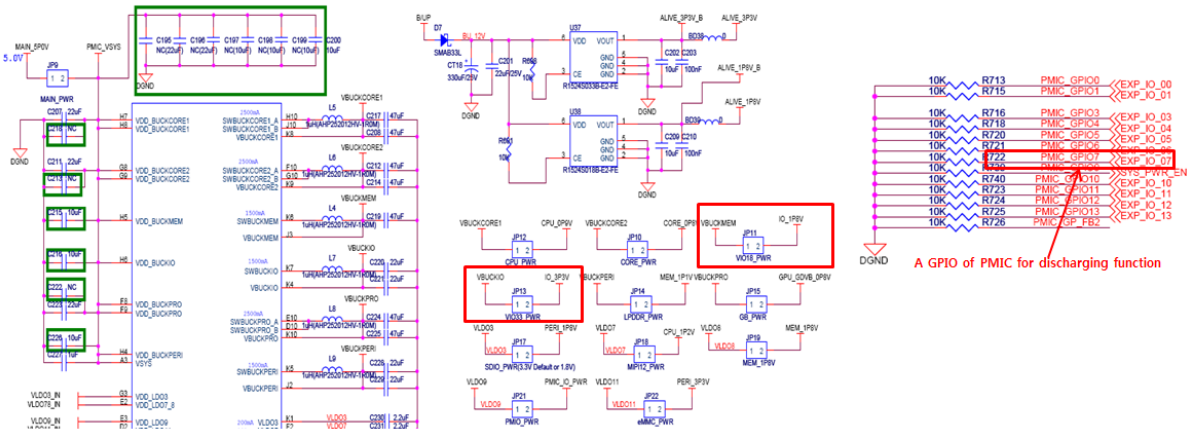
9.1 Power On and Wake-Up

1. **PWR_CTLA** & **PWR_CTLB** is controlled by TCC8030 when power on and wake up.
2. **PWR_EN** is logical High.
3. **HVBUCKEN** is logical High by **PWR_EN**:High with OR logic. (**PWR_EN**: “High” OR **PMIC_HVBUCKEN**: “Low” = High)
4. High Voltage Buck is turned on.
5. PMIC is turned on and **PMIC_HVBUCKEN** is logical High.
6. System is turned on.

9.2 Power Off and Power Down

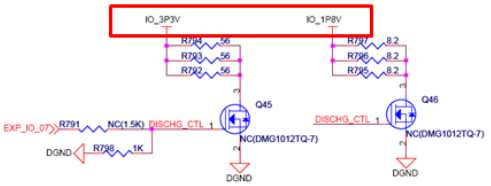
1. **PWR_CTLA** & **PWR_CTLB** is controlled by TCC8030 when power off and power down.
2. **PWR_EN** is logical Low.
3. PMIC detect **PMIC_SYS_EN**: Low by **PWR_EN**.
   PMIC process power off sequence. At this time High Voltage BUCK is still turned on by **PMIC_HVBUCKEN** High.
4. PMIC make **HVBUCKEN** Low after complete power off sequence.
5. **HVBUCKEN** is logical Low by **PMIC_HVBUCKEN**: Low with OR logic.
   (**PWR_EN**: “Low” OR **PMIC_HVBUCKEN**: “Low” = Low)
6. High Voltage Buck is turned off and then System is Power off or down status.

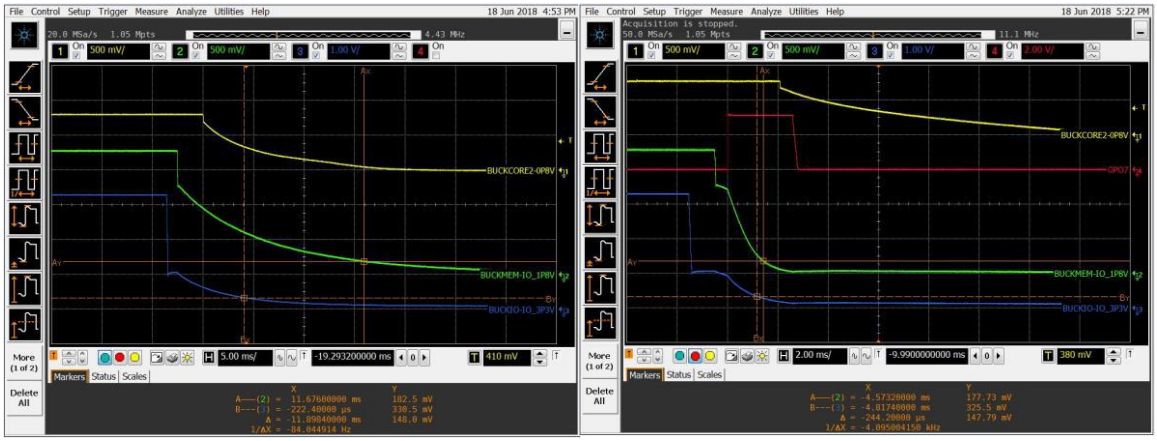
10 PMIC GPIO7 Setting for Discharging Function



- Q45 and Q46 help to discharge the IO power of the TCC8030
- PMIC GPIO7 is used to turn on the Q25 and Q46.

- **PMIC GPIO7 must be used for discharging function.**
- **If not used as the function, open.**





If the discharge function is used, IO_1P8V and IO_3P3V will be less than 10% of their respective output voltage before BUCKCORE2-0P8V is disabled.

11 DA9063L-A Power Mode Transition

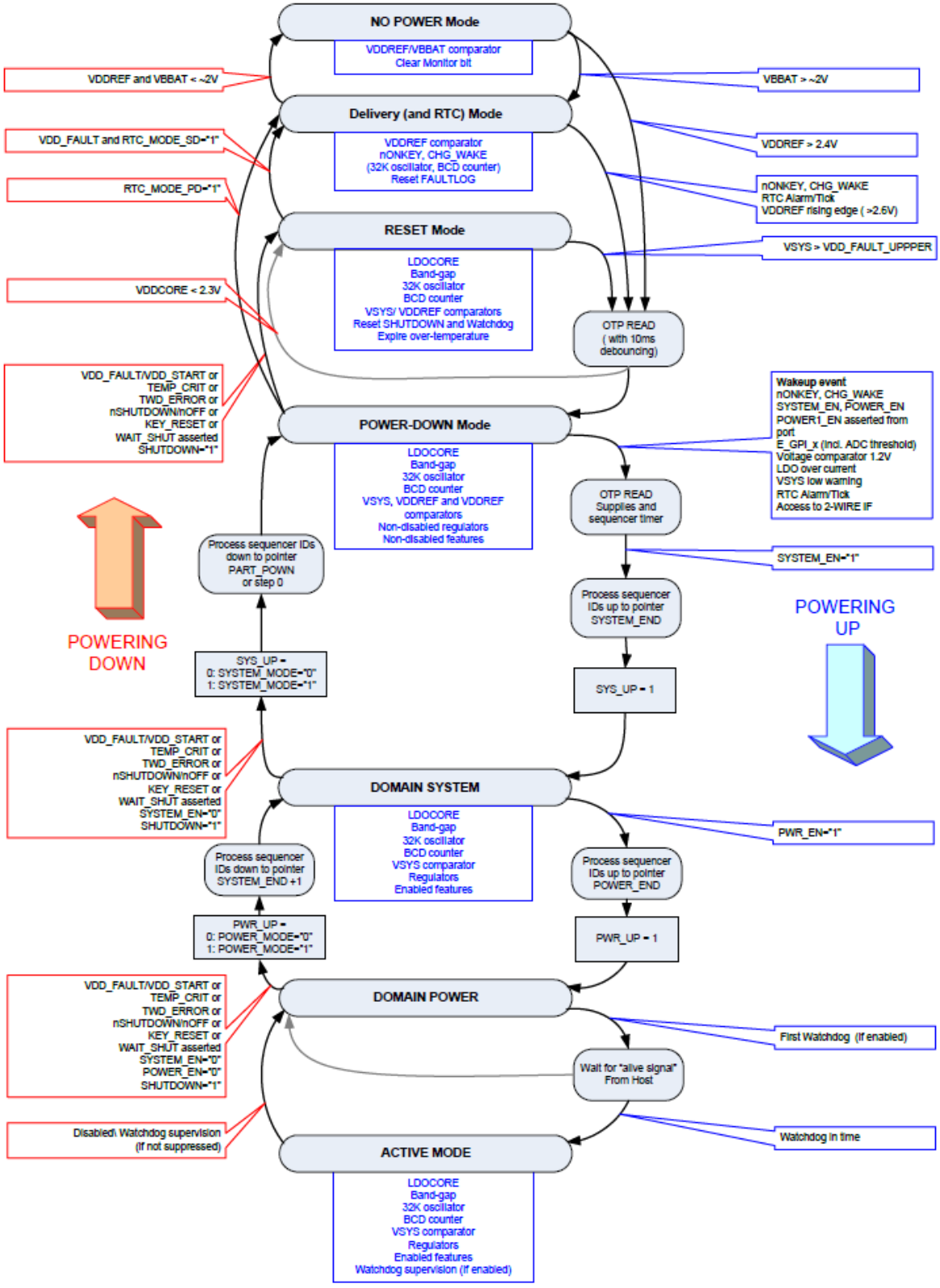


Figure 6: DA9063L-A Power Mode Transition

12 DA9063L-A Sequencer Configuration for TCC8030

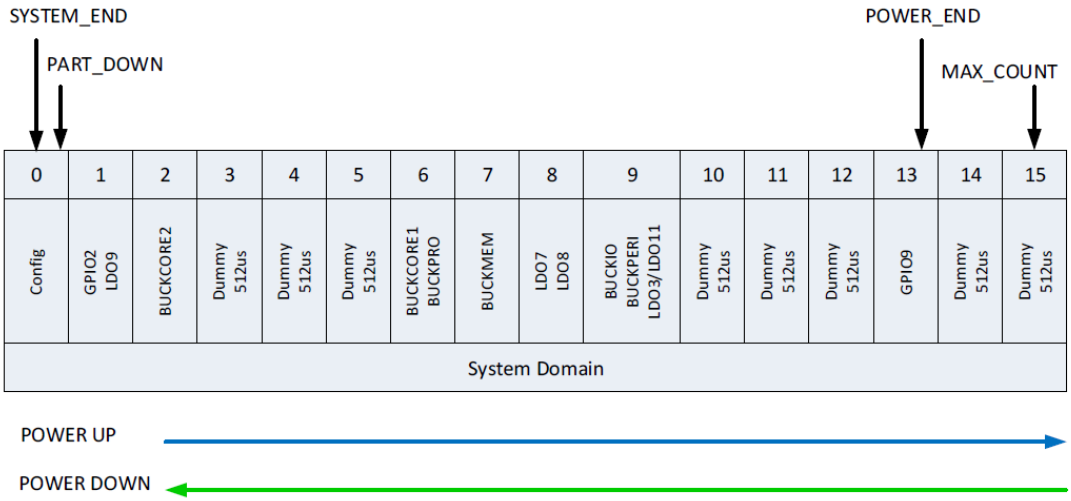


Figure 7: DA9063L-A Sequencer Configuration for TCC8030

13 DA9063L-A Power-On Sequence for TCC8030

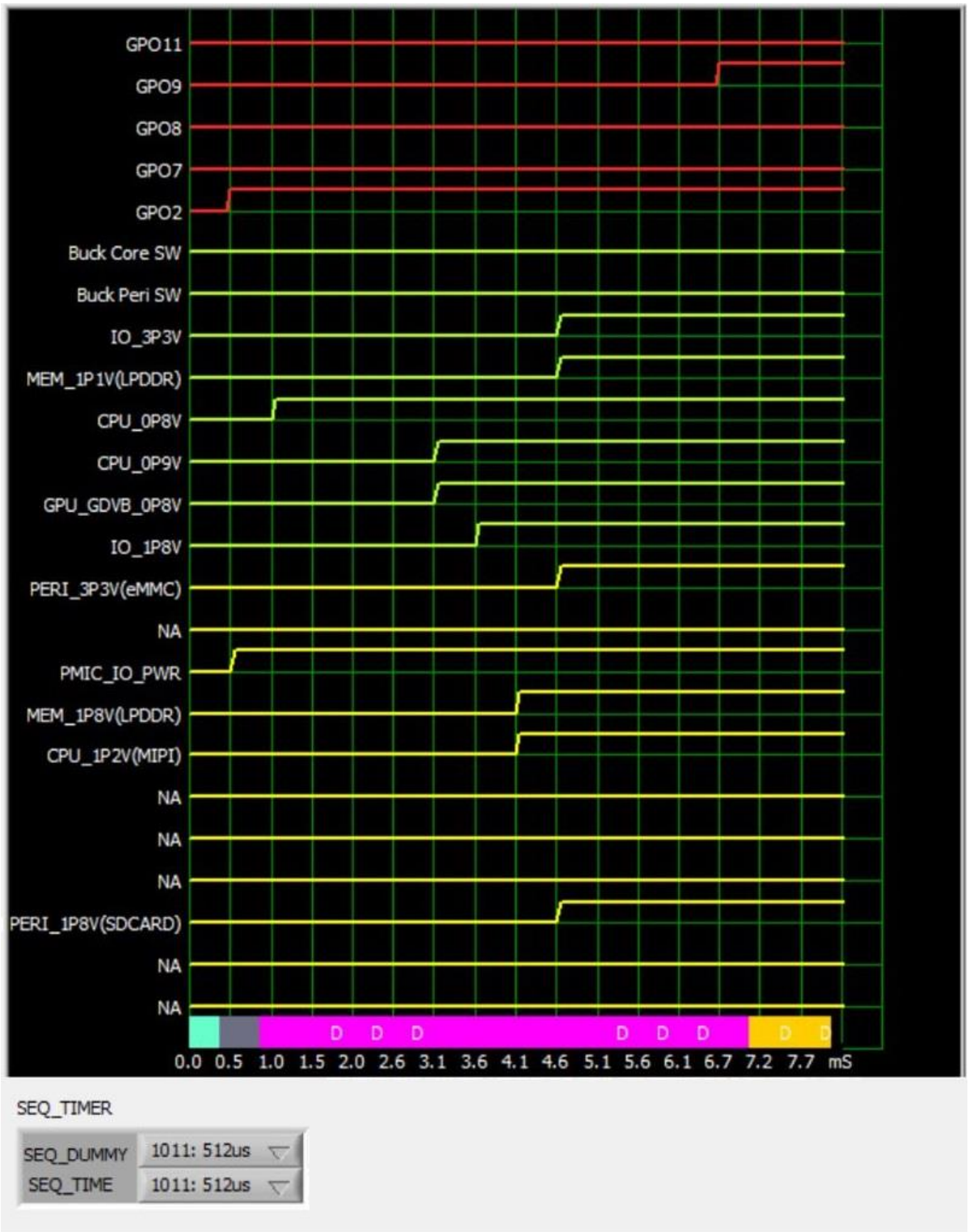


Figure 8: TCC8030 Power Up Sequence

14 DA9063L-A Register Map

14.1 GPIO Control

Table 4: GPIO0-1 Control

Register Address	Bit	Set	Type	Label	Description
0x15 GPIO0-1	7	1	R/W	GPIO1_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	0	R/W	GPIO1_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO1_PIN	PIN assigned to 00: ADCIN2/1.2 V comparator 01: GPI (optional regulator HW control) 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	4	1	R/W		
	3	1	R/W	GPIO0_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	0	R/W	GPIO0_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1	1	R/W	GPIO0_PIN	PIN assigned to 00: ADCIN1 01: GPI (optional regulator HW control) 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	0	1	R/W		

Table 5: GPIO2-3 Control

Register Address	Bit	Set	Type	Label	Description
0x16 GPIO2-3	7	1	R/W	GPIO3_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	0	R/W	GPIO3_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO3_PIN	PIN assigned to 00: ADCIN2/1.2 V comparator 01: GPI (optional regulator HW control) 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	4	1	R/W		
	3	1	R/W	GPIO2_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	0	R/W	GPIO2_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1	1	R/W	GPIO2_PIN	PIN assigned to 00: ADCIN3 01: GPI (optional regulator HW control) 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)
	0	0	R/W		

Table 6: GPIO4-5 Control

Register Address	Bit	Set	Type	Label	Description
0x17 GPIO4-5	7	1	R/W	GPIO5_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	0	R/W	GPIO5_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO5_PIN	PIN assigned to 00: Reserved 01: GPI (optional regulator HW control) 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	4	1	R/W		
	3	1	R/W	GPIO4_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	0	R/W	GPIO4_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1	1	R/W	GPIO4_PIN	PIN assigned to 00: CORE_SWS 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	0	1	R/W		

Table 7: GPIO6-7 Control

Register Address	Bit	Set	Type	Label	Description
0x18 GPIO6-7	7	1	R/W	GPIO7_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	0	R/W	GPIO7_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO7_PIN	PIN assigned to 00: Reserved 01: GPI 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)
	4	0	R/W		
	3	1	R/W	GPIO6_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	0	R/W	GPIO6_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1	1	R/W	GPIO6_PIN	PIN assigned to 00: PERI_SWS 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	0	1	R/W		

Table 8: GPIO8-9 Control

Register Address	Bit	Set	Type	Label	Description
0x19 GPIO8-9	7	1	R/W	GPIO9_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	1	R/W	GPIO9_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO9_PIN	PIN and status register bit assigned to 00: GPI with PWR_EN 01: GPI 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)
	4	0	R/W		
	3	0	R/W	GPIO8_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	1	R/W	GPIO8_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1	0	R/W	GPIO8_PIN	PIN and status register bit assigned to 00: GPI with SYS_EN 01: GPI 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)
	0	0	R/W		

Table 9: GPIO10-11 Control

Register Address	Bit	Set	Type	Label	Description
0x1A GPIO10-11	7	1	R/W	GPIO11_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	1	R/W	GPIO11_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO11_PIN	PIN assigned to 00: GPO (Open drain, with optional blinking) 01: GPI 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)
	4	1	R/W		
	3	1	R/W	GPIO10_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	1	R/W	GPIO10_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1	1	R/W	GPIO10_PIN	PIN assigned to 00: GPI with PWR_EN 01: GPI 10: GPO (Open drain) 11: GPO mode controlled (Push-pull)
	0	1	R/W		

Table 10: GPIO12-13 Control

Register Address	Bit	Set	Type	Label	Description
0x1B GPIO12-13	7	1	R/W	GPIO13_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	1	R/W	GPIO13_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO13_PIN	0: GPI: active low GPO/GP_FB1: supplied from external/VDD_IO1 1: GPI: active high GPO/GP_FB1: supplied from VDD_IO2
	4	1	R/W		
	3	1	R/W	GPIO12_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	1	R/W	GPIO12_TYPE	0: GPI: active low GPO/ nVDD_FAULT/VSYS monitor: supplied from VDD_IO1 1: GPI: active high GPO/DD_FAULT/VSYS monitor: supplied from VDD_IO2
	1	1	R/W	GPIO12_PIN	PIN assigned to 00: nVDD_FAULT (Push-pull) 01: GPI 10: GPO controlled by the state of VSYS monitor (Push-pull) 11: GPO mode controlled (Push-pull)
	0	1	R/W		

Table 11: GPIO14-15 Control

Register Address	Bit	Set	Type	Label	Description
0x1C GPIO14-15	7	1	R/W	GPIO15_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	6	1	R/W	GPIO15_TYPE	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5	1	R/W	GPIO15_PIN	PIN assigned to 00: GPO (Open drain, with optional blinking) 01: GPI 10: CLK (configured via GPIO14_PIN) 11: GPO mode controlled (Open drain)
	4	1	R/W		
	3	1	R/W	GPIO14_WEN	0: Passive to active transition triggers a wakeup 1: Wakeup suppressed
	2	1	R/W	GPIO14_TYPE	0: GPI: active low GPO: supplied from external/VDD_IO1 DATA/CLK supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2 DATA/CLK supplied from VDD_IO2
	1	1	R/W	GPIO14_PIN	PIN assigned to

Register Address	Bit	Set	Type	Label	Description
	0	1	R/W		00: GPO (Open drain, with optional blinking) 01: GPI 10: DATA (assigns GPIO15_PIN to CLK) 11: GPO mode controlled (Push-pull)

Table 12: GPIO- MODE0-7

Register Address	Bit	Set	Type	Label	Description
0x1D GPIO-MODE0-7	7	1	R/W	GPIO7_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	6	0	R/W	GPIO6_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	5	0	R/W	GPIO5_MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level
	4	0	R/W	GPIO4_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	3	0	R/W	GPIO3_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	2	1	R/W	GPIO2_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	1	0	R/W	GPIO1_MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level
	0	0	R/W	GPIO0_MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level

Table 13: GPIO- MODE8-15

Register Address	Bit	Set	Type	Label	Description
0x1E GPIO-MODE8-15	7	0	R/W	GPIO15_MODE	0: GPI: debouncing off GPO: Sets output to low level (active high for blinking) 1: GPI: debouncing on GPO: Sets output to high level (active low for blinking)

Register Address	Bit	Set	Type	Label	Description
	6	0	R/W	GPIO14_MODE	0: GPI: debouncing off GPO: Sets output to low level (active high for blinking) 1: GPI: debouncing on GPO: Sets output to high level (active low for blinking)
	5	0	R/W	GPIO13_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for GP_FB1) 1: GPI: debouncing on GPO: Sets output to high level (active high for GP_FB1)
	4	0	R/W	GPIO12_MODE	0: GPI: debouncing off GPO: Sets output to low level (active low for nVDD_FAULT, VSYS monitor state) 1: GPI: debouncing on GPO: Sets output to high level (active high for nVDD_FAULT, VSYS monitor state)
	3	0	R/W	GPIO11_MODE	0: GPI: debouncing off GPO: Sets output to low level (active high for blinking) 1: GPI: debouncing on GPO: Sets output to high level (active low for blinking)
	2	0	R/W	GPIO10_MODE	0: GPI/PWR1_EN: debouncing off GPO: Sets output to low level 1: GPI/PWR1_EN: debouncing on GPO: Sets output to high level
	1	1	R/W	GPIO9_MODE	0: GPI/PWR_EN: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI/PWR_EN debouncing on GPO: Sets output to high level (active high for sequencer control)
	0	1	R/W	GPIO8_MODE	0: GPI/SYS_EN: debouncing off GPO: Sets output to low level 1: GPI/SYS_EN: debouncing on GPO: Sets output to high level

14.2 Power Sequencer

Table 14: SEQ_TIMER

Register Address	Bit	Set	Type	Label	Description
0x82 SEQ_TIMER	7	1	R/W	SEQ_DUMMY	1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms
	6	0	R/W		
	5	1	R/W		
	4	1	R/W		
	3	1	R/W	SEQ_TIME	1001: 384 µs 1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms
	2	0	R/W		
	1	1	R/W		
	0	1	R/W		

Table 15: ID_4_3

Register Address	Bit	Set	Type	Label	Description
0x84 ID_4_3	7	0	R/W	Reserved	
	6	0	R/W		
	5	0	R/W		
	4	0	R/W		
	3	1	R/W	LDO3_STEP	Power sequencer time slot for LDO3 control
	2	0	R/W		
	1	0	R/W		
	0	1	R/W		

Table 16: ID_8_7

Register Address	Bit	Set	Type	Label	Description
0x86 ID_8_7	7	1	R/W	LDO8_STEP	Power sequencer time slot for LDO8 control
	6	0	R/W		
	5	0	R/W		
	4	0	R/W		
	3	1	R/W	LDO7_STEP	Power sequencer time slot for LDO7 control
	2	0	R/W		
	1	0	R/W		
	0	0	R/W		

Table 17: ID_10_9

Register Address	Bit	Set	Type	Label	Description
0x87 ID_10_9	7	0	R/W	Reserved	
	6	0	R/W		
	5	0	R/W		
	4	0	R/W		
	3	0	R/W	LDO9_STEP	Power sequencer time slot for LDO9 control
	2	0	R/W		
	1	0	R/W		
	0	1	R/W		

Table 18: ID_12_11

Register Address	Bit	Set	Type	Label	Description
0x88 ID_12_11	7	0	R/W	PD_DIS_STEP	Power sequencer time slot for control of blocks to be disabled/paused during POWERDOWN mode
	6	0	R/W		
	5	0	R/W		
	4	0	R/W		
	3	1	R/W	LDO11_STEP	Power sequencer time slot for LDO11 control
	2	0	R/W		
	1	0	R/W		
	0	1	R/W		

Table 19: ID_14_13

Register Address	Bit	Set	Type	Label	Description
0x89 ID_14_13	7	0	R/W	BUCKCORE2_STEP	Power sequencer time slot for BUCKCORE2 control (disabled in BUCKCORE dual phase mode)
	6	0	R/W		
	5	1	R/W		
	4	0	R/W		
	3	0	R/W	BUCKCORE1_STEP	Power sequencer time slot for BUCKCORE1 control
	2	1	R/W		
	1	1	R/W		
	0	0	R/W		

Table 20: ID_16_15

Register Address	Bit	Set	Type	Label	Description
0x8A ID_16_15	7	1	R/W	BUCKIO_STEP	Power sequencer time slot for BUCKIO control
	6	0	R/W		
	5	0	R/W		
	4	1	R/W		
	3	0	R/W	BUCKPRO_STEP	Power sequencer time slot for BUCKPRO control
	2	1	R/W		
	1	1	R/W		
	0	0	R/W		

Table 21: ID_18_17

Register Address	Bit	Set	Type	Label	Description
0x8B ID_18_17	7	1	R/W	BUCKPERI_STEP	Power sequencer time slot for BUCKPERI control
	6	0	R/W		
	5	0	R/W		
	4	1	R/W		
	3	0	R/W	BUCKMEM_STEP	Power sequencer time slot for BUCKMEM control
	2	1	R/W		
	1	1	R/W		
	0	1	R/W		

Table 22: ID_22_21

Register Address	Bit	Set	Type	Label	Description
0x8D ID_22_21	7	0	R/W	GP_FALL1_STEP	Power sequencer time slot for falling edge control of GPO2
	6	0	R/W		
	5	0	R/W		
	4	0	R/W		
	3	0	R/W	GP_RISE1_STEP	Power sequencer time slot for rising edge control of GPO2
	2	0	R/W		
	1	0	R/W		
	0	1	R/W		

Table 23: ID_24_23

Register Address	Bit	Set	Type	Label	Description
0x8E ID_24_23	7	0	R/W	GP_FALL2_STEP	Power sequencer time slot for falling edge control of GPO7
	6	1	R/W		
	5	1	R/W		
	4	0	R/W		
	3	0	R/W	GP_RISE2_STEP	Power sequencer time slot for rising edge control of GPO7
	2	0	R/W		
	1	0	R/W		
	0	0	R/W		

Table 24: ID_28_27

Register Address	Bit	Set	Type	Label	Description
0x90 ID_28_27	7	0	R/W	GP_FALL4_STEP	Power sequencer time slot for falling edge control of GPO9
	6	0	R/W		
	5	0	R/W		
	4	0	R/W		
	3	1	R/W	GP_RISE4_STEP	Power sequencer time slot for rising edge control of GPO9
	2	1	R/W		
	1	0	R/W		
	0	1	R/W		

14.3 Regulator Settings

Table 25: VBCORE2-A

Register Address	Bit	Set	Type	Label	Description
0xA3 VBCORE2_A	7	0	R/W	BCORE2_SL_A	0: Configures BUCKCORE2 to Synchronous mode, when selecting A voltage settings 1: Configures BUCKCORE2 to Sleep mode, when selecting A voltage settings
	6	0	R/W	VBCORE2_A	0101000: 0.70 V, PWM Mode range 0101001: 0.71 V 0110100: 0.82V 1010000: 1.10 V … 1110011: 1.45 V 1110100: 1.46 V 1110101: 1.47 V 1110110: 1.48 V 1110111: 1.49 V 1111000: 1.50 V
	5	1	R/W		
	4	1	R/W		
	3	0	R/W		
	2	1	R/W		
	1	0	R/W		
	0	0	R/W		

Table 26: VBCORE1_A

Register Address	Bit	Set	Type	Label	Description
0xA4 VBCORE2_B	7	0	R/W	BCORE1_SL_A	0: Configures BUCKCORE1 to Synchronous mode, when selecting A voltage settings 1: Configures BUCKCORE1 to Sleep mode, when selecting A voltage settings
	6	0	R/W	VBCORE1_A	0101000: 0.70 V, PWM Mode range 0101001: 0.71 V 0111110: 0.92V 1010000: 1.10 V … 1110011: 1.45 V 1110100: 1.46 V 1110101: 1.47 V 1110110: 1.48 V 1110111: 1.49 V 1111000: 1.50 V
	5	1	R/W		
	4	1	R/W		
	3	1	R/W		
	2	1	R/W		
	1	1	R/W		
	0	0	R/W		

Table 27: VBPRO_A

Register Address	Bit	Set	Type	Label	Description
0xA5 VBPRO_A	7	0	R/W	BPRO_SL_A	0: Configures BUCKPRO to Synchronous mode, when selecting A voltage settings 1: Configures BUCKPRO to Sleep mode, when selecting A voltage settings
	6	0	R/W	VBPRO_A	0010010: 0.71 V 0010011: 0.72 V 0010100: 0.73 V 0010101: 0.74 V 0010110: 0.75 V 0011101: 0.82V 1000011: 1.20 V … 1110011: 1.68 V 1110100: 1.69 V 1110101: 1.70 V
	5	0	R/W		
	4	1	R/W		
	3	1	R/W		
	2	1	R/W		
	1	0	R/W		
	0	1	R/W		

Table 28: VBMEM_A

Register Address	Bit	Set	Type	Label	Description
0xA6 VBMEM_A	7	0	R/W	BMEM_SL_A	0: Configures BUCKMEM to Synchronous mode, when selecting A voltage settings 1: Configures BUCKMEM to Sleep mode, when selecting A voltage settings
	6	0	R/W	VBMEM_A	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … 0010100: 1.20 V 0110010: 1.8V 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V …
	5	1	R/W		
	4	1	R/W		
	3	0	R/W		
	2	0	R/W		
	1	1	R/W		
	0	0	R/W		

Table 29: VBIO_A

Register Address	Bit	Set	Type	Label	Description
0xA7 VBIO_A	7	0	R/W	BIO_SL_A	0: Configures BUCKIO to Synchronous mode, when selecting A voltage settings 1: Configures BUCKIO to Sleep mode, when selecting A voltage settings
	6	1	R/W	VBIO_A	0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V 1111101: 3.3V 1111111: 3.34 V
	5	1	R/W		
	4	1	R/W		
	3	1	R/W		
	2	1	R/W		
	1	0	R/W		
	0	1	R/W		

Table 30: VBPERI_A

Register Address	Bit	Set	Type	Label	Description
0xA8 VBPERI_A	7	0	R/W	BPERI_SL_A	0: Configures BUCKPERI to Synchronous mode, when selecting A voltage settings 1: Configures BUCKPERI to Sleep mode, when selecting A voltage settings
	6	0	R/W	VBPERI_A	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V 0010000: 1.12V 0110010: 1.80 V ... 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V …
	5	0	R/W		
	4	1	R/W		
	3	0	R/W		
	2	0	R/W		
	1	0	R/W		
	0	0	R/W		

Table 31: VLDO3_A

Register Address	Bit	Set	Type	Label	Description
0xAB VLDO3_A	7	0	R/W	LDO3_SL_A	0: Configures LDO to half-current mode, when selecting A voltage settings 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	1	R/W	VLDO3_A	
	5	1	R/W		
	4	1	R/W		
	3	1	R/W		

Register Address	Bit	Set	Type	Label	Description
	2	0	R/W		
	1	0	R/W		
	0	0	R/W		

Table 32: VLDO7_A

Register Address	Bit	Set	Type	Label	Description
0xAF VLDO7_A	7	0	R/W	LDO7_SL_A	0: Configures LDO to half-current mode, when selecting A voltage settings 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	0	R/W	Reserved	
	5	0	R/W	VLDO7_A	000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V
	4	0	R/W		
	3	1	R/W		
	2	0	R/W		
	1	0	R/W		
	0	0	R/W		

Table 33: VLDO8_A

Register Address	Bit	Set	Type	Label	Description
0xB0 VLDO8_A	7	0	R/W	LDO8_SL_A	0: Configures LDO to half-current mode, when selecting A voltage settings 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	0	R/W	Reserved	
	5	0	R/W	VLDO8_A	010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V
	4	1	R/W		
	3	0	R/W		
	2	1	R/W		
	1	0	R/W		
	0	0	R/W		

Table 34: VLDO9_A

Register Address	Bit	Set	Type	Label	Description
0xB1 VLDO9_A	7	0	R/W	LDO9_SL_A	0: Configures LDO to half-current mode, when selecting A voltage settings 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	0	R/W	Reserved	
	5	1	R/W	VLDO9_A	101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V
	4	1	R/W		
	3	0	R/W		
	2	0	R/W		
	1	1	R/W		
	0	0	R/W		

Table 35: VLDO11_A

Register Address	Bit	Set	Type	Label	Description
0xB3 VLDO11_A	7	0	R/W	LDO11_SL_A	0: Configures LDO to half-current mode, when selecting A voltage settings 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	0	R/W	Reserved	
	5	1	R/W	VLDO11_A	101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V
	4	1	R/W		
	3	0	R/W		
	2	0	R/W		
	1	1	R/W		
	0	0	R/W		

Table 36: CONFIG_F

Register Address	Bit	Set	Type	Label	Description
0x10B CONFIG_F	7	1	R/W	LDO11_BYP	0: LDO11 is configured for regulator mode 1: LDO11 bypass mode enabled
	6	1	R/W	LDO8_BYP	0: LDO8 is configured for regulator mode 1: LDO8 bypass mode enabled
	5	0	R/W	LDO7_BYP	0: LDO7 is configured for regulator mode 1: LDO7 bypass mode enabled
	4	0	R/W	Reserved	

Register Address	Bit	Set	Type	Label	Description
	3	0	R/W	LDO3_BYP	0: LDO3 is configured for regulator mode 1: LDO3 bypass mode enabled
	2	1	R/W	LDO11_AUTO	Selects LDO11 (during powering up): 0: configured from LDO11_CONF 1: enabled
	1	0	R/W	Reserved	
	0	1	R/W	LDO9_AUTO	Selects LDO9 (during powering up): 0: configured from LDO9_CONF 1: enabled

The register map describes GPIOs, power sequencer and regulator settings (BUCKs and LDOs output voltage levels and bypass mode LDOs) for the TCC8030 reference board.

All other register values are default setting and can be verified directly through I2C interface.

15 Conclusion

The approved OTP configuration is “DA9063L-A-1F_Telechips_v04_4533.ini”

Revision History

Revision	Date	Description
1.0	22-Oct-2019	Initial version
1.1	24-Feb-2022	File was rebranded with new logo, copyright and disclaimer

DA9063L-A Power Management for TCC8030 Platform

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