

RYZ024

Power Consumption Measurements on RYZ024-Based Modules

Contents

1. Introduction	2
1.1 RYZ024 Platform Power States.....	2
1.2 RRC Idle Mode With or Without eDRX and PSM	3
1.2.1 RRC Idle Mode	3
1.2.2 eDRX.....	4
1.2.3 PSM.....	5
2. Setup	5
2.1 List of Required Equipment	5
2.2 Setup Overview.....	5
2.3 Modem Basic Settings.....	6
2.3.1 Checking Modem Boot Up and AT Channel.....	6
2.3.2 Checking Attach.....	7
2.3.3 Checking Signal Conditions.....	7
2.3.4 Modem Wake Sources	8
2.3.5 Timers Configuration	8
2.3.6 Get URCS	9
3. Power Measurement Use Cases	10
3.1 Boot with CFUN=0	10
3.2 PSM Mode.....	11
3.2.1 Setting PSM Timers	11
3.2.2 Test Procedure with UDP Traffic	12
3.2.3 Tracking Area Update	13
3.2.4 PSM and TCP Traffic	14
3.3 eDRX Mode	15
3.3.1 Setting eDRX Parameters	15
3.3.2 Test Procedure	15
3.3.3 Tracking Area Update	17
3.3.4 SMS Reception	17
3.3.5 eDRX and TCP Traffic.....	18
3.4 Relaxed Monitoring	19
4. Troubleshooting Check List.....	19
5. Abbreviations.....	20
6. Appendix A – Power Monitor Tools.....	20
Revision History.....	21

1. Introduction

This manual is intended to help end users of Renesas' solutions to evaluate the power consumption of RYZ024 (LTE-M) module.

It is used as a guide to configure the software and run the tests on the live network to achieve the expected power consumption numbers in active transmission, RRC Idle Mode, eDRX and PSM. eDRX and PSM are two new protocols introduced by LTE Releases 12 and 13 for the User Equipment (UE) in RRC Idle Mode and which can bring dramatic improvements on the power consumption.

The prerequisite for using this document is that the setup is ready to measure power consumption. See the power consumption section of the user manual of the Evaluation Kit that you are using to identify the required operations and prepare the setup for power measurement.

1.1 RYZ024 Platform Power States

The RYZ024 platform operates in four different power states (please refer to the Software Release Note for the power consumption of each state):

Mode	Wake-up latency
Deep sleep	< 2 s
Sleep	< 15 ms
Active standby	< 1 ms
Modem active	< 1 ms

When the platform is in Sleep or Deep Sleep mode, the UARTs are turned off.

The PS_STATUS signal of the platform indicates to the host MCU which state the platform is in. The following pictures show how PS_STATUS behaves when the platform wakes from:

- Sleep mode:

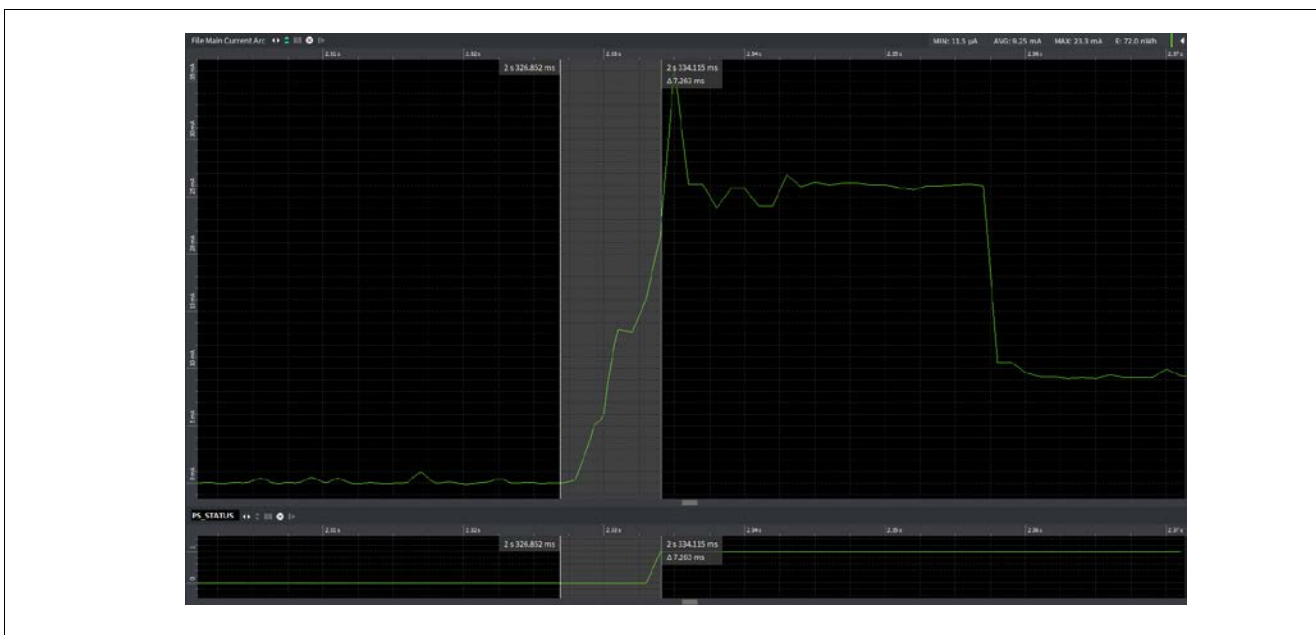


Figure 1. Sleep mode

- Deep Sleep mode:



Figure 2. Deep Sleep Mode

Please refer to the *RYZ024 Module System Integration Guide* for more details.

Several conditions must be met before the platform can enter Sleep or Deep Sleep modes:

- No data or URC pending in the UARTs buffers;
- No wake source active;
- RRC connection released (RRC connection release message received from the network).

1.2 RRC Idle Mode With or Without eDRX and PSM

Once the UE is attached to the eNB and registered in the network, when it has no more data to receive or transmit, the eNB sends an RRC Connection Release message. After this message, the UE changes its RRC state from Connected to Idle mode. The time between the last message sent from the UE and the transmission of the RRC Connection Release message depends on the settings of the network (inactivity timer value).

This section provides an overview of the differences between the available protocols and how they can bring a significant benefit on the power consumption while in stand-by.

1.2.1 RRC Idle Mode

When in RRC Idle Mode with PSM or eDRX off, the UE listens for a paging message every paging cycle. The UE is reachable at every paging window. The paging cycle period is network dependent; while the maximum value is 2.56 s, it is usually set to 1.28 s.

Between each paging opportunity, the RYZ024 platform enters Sleep mode.

When in RRC Idle Mode with PSM or eDRX off, the UE listens for a paging message every paging cycle. The UE is reachable at every paging window. The paging cycle period is network dependent; while the maximum value is 2.56 s, it is usually set to 1.28 s.

Between each paging opportunity, the RYZ024 platform enters Sleep mode.

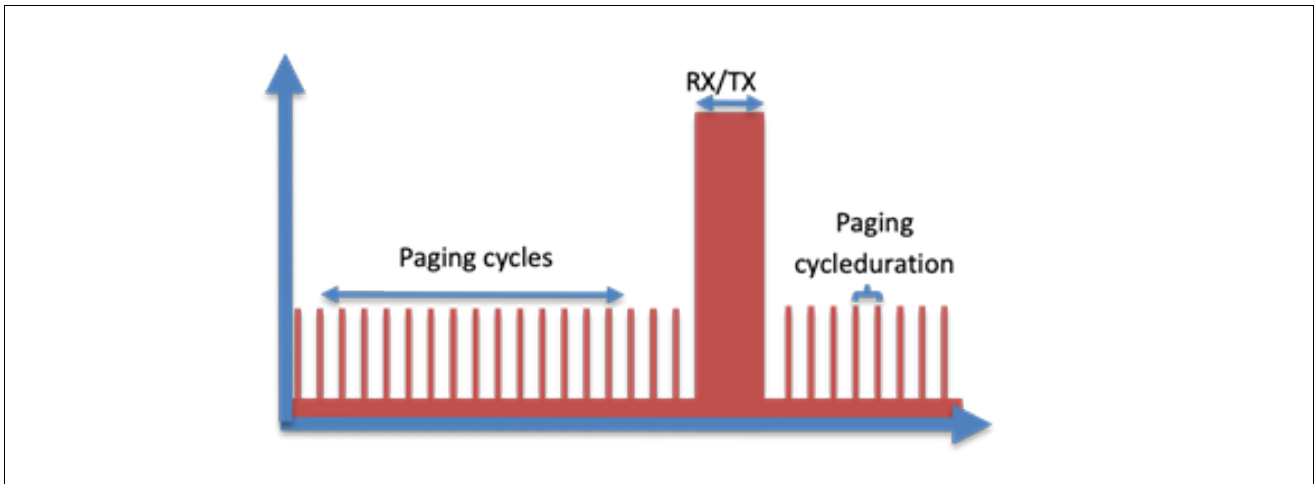


Figure 3. Paging Cycles

1.2.2 eDRX

In extended Discontinuous Reception (eDRX) mode, the UE is allowed to monitor only the paging cycles falling within a specific interval named Paging Time Window (PTW). The duration of the PTW is set to multiples of 1.28 seconds.

Once the PTW has elapsed, the UE enters eDRX sleep state. In this case, if the RYZ024 platform has no task pending, it goes into Deep Sleep to save power.

After one eDRX cycle, the UE wakes up and monitors the paging cycles during the next PTW.

The period of one eDRX cycle must be a multiple of 10.24 s, since a 10.24 s period corresponds to one hyper-frame. Thus, the minimum value of the eDRX cycle is 10.24 s and the maximum value is 2621.44 s (around 44 min).

The network side can reach the UE only during a PTW. On the UE side, transmission can resume any time, for instance if data from a sensor must be sent to a cloud server.

Note that in eDRX, the UE performs Tracking Area Update (TAU) every T3412's duration. Unlike the PSM, T3412's value in eDRX is set by the network and cannot be overridden.

Renesas' optimized implementation of eDRX, called 'eco-Paging', allows the RYZ024 platform to reach extremely low levels of power consumption, as low as 1 μ A in eDRX sleep.

Eco-Paging is activated only for eDRX cycles longer than 20.48 s. Shorter eDRX cycles (10.24 s) put the modem into Sleep mode rather than Deep Sleep mode.

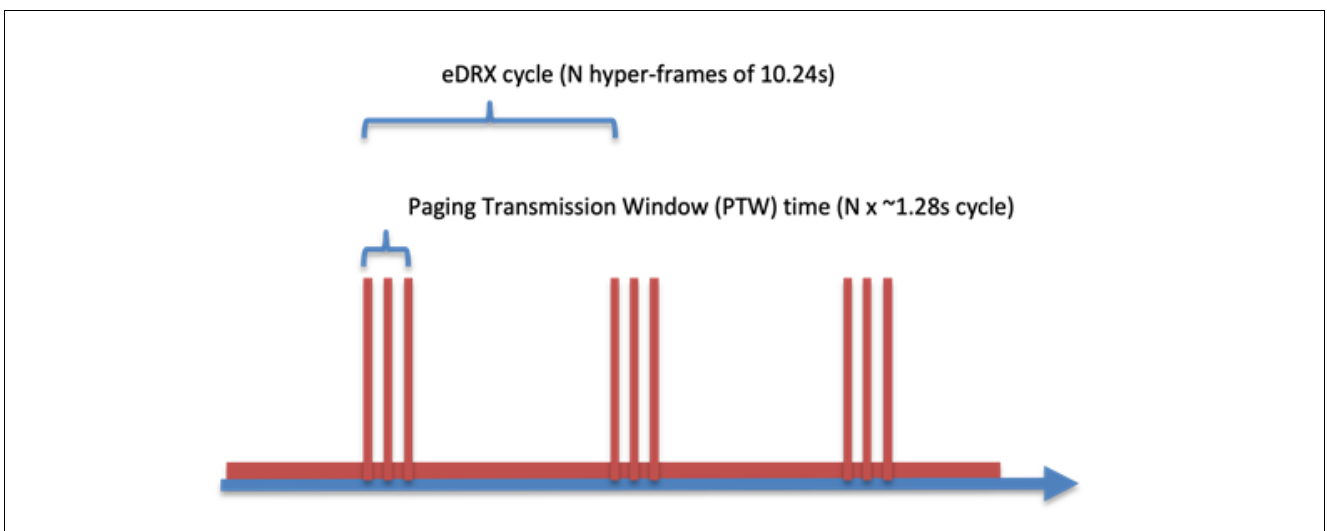


Figure 4. Paging Transmission Window

1.2.3 PSM

PSM is activated on the UE by specifying two timer values in the NAS Attach Request message or the Tracking Area Update (TAU).

The first timer, T3324, controls how long the UE remains in idle mode after an Attach or TAU procedure. In other words, the UE monitors paging as long as T3324 is counting down. It then switches to PSM sleep state.

The second timer, called extended T3412, defines the extended period between two consecutive TAU procedures.

The difference T3412 - T3324 corresponds to the PSM sleep time.

The RYZ024 platform goes into Deep Sleep mode while the UE is in PSM sleep state if no wake lock is active and the AT UARTs have no more data/URC to deliver.

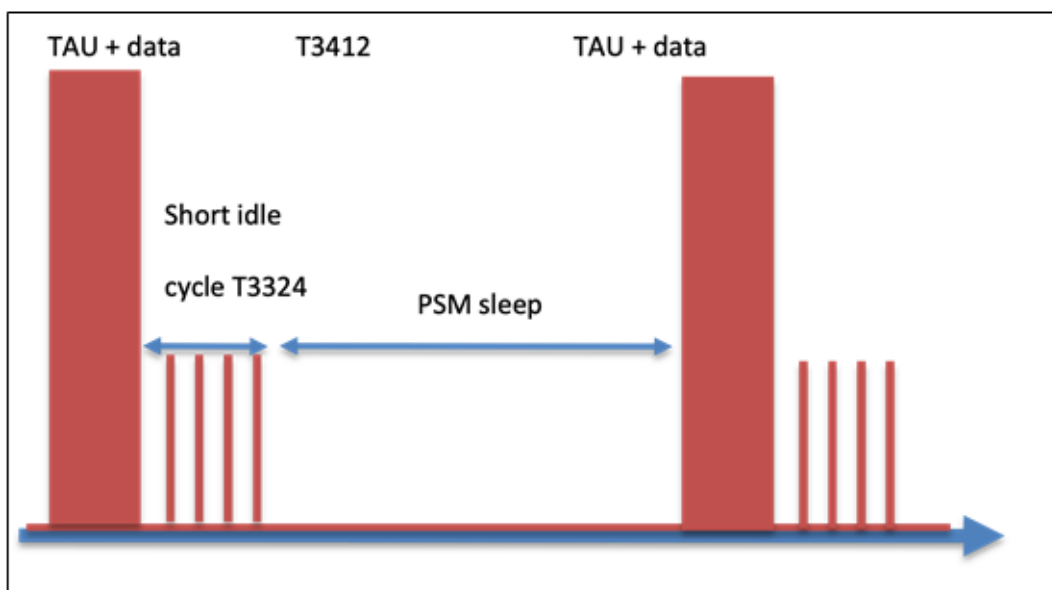


Figure 5. Power Saving Mode Cycles

2. Setup

2.1 List of Required Equipment

Measurements require the following hardware:

- The PMOD is a standalone cellular modem board based on Renesas RYZ024
- Several USB-mini cables
- A USIM, 3FF micro size
- An LTE tester such as CMW500 or Anritsu MD8430A simulator with an RF cable, if you do not have access to an LTE-M network
- A 2.5 V to 5.5 V lab power supply and power analyzer. It can be one combined device (for example the *OTII Power Monitor* from *Qoitech*) or two separate devices. The ammeter's accuracy should be on par or under 1 μ A. This document assumes the use of a combined power supply- ammeter device. Annex B provides device overview.
- A computer.

2.2 Setup Overview

Figure 6 shows how to connect the power supply and the computer with RTKY024A0B00000BE, the PMOD Expansion Board of RYZ024A module. The RTKY024A0B00000BE board was chosen as an example. The same setup works with any other RYZ024 module's PMOD.

RTKY024A0B00000BE board has PMOD Interface as UART0 and USB Interface as UART1.

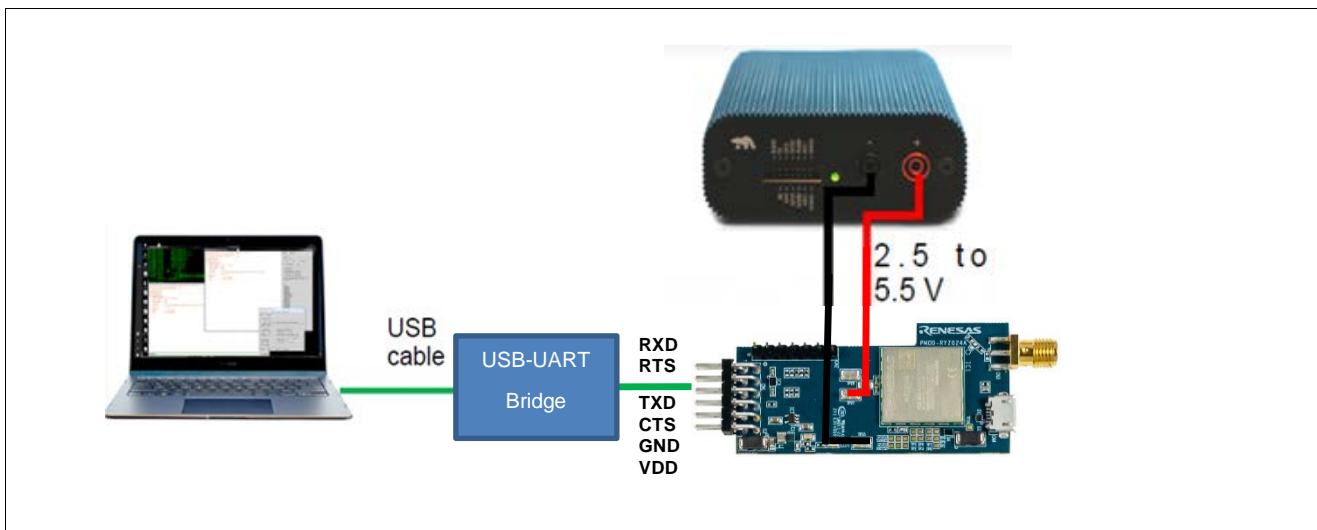
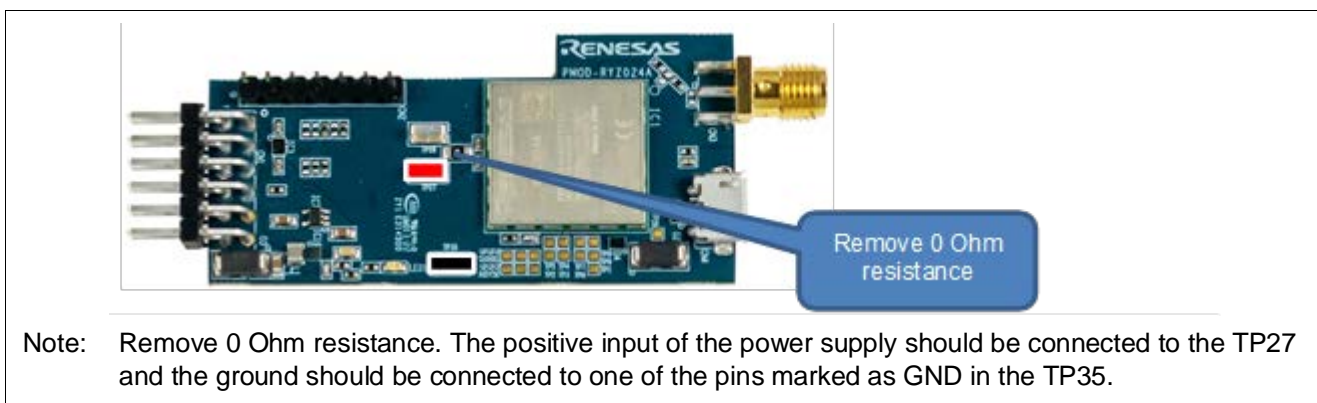


Figure 6. PMOD Expansion Board of RYZ024A module Setup



Note: Remove 0 Ohm resistance. The positive input of the power supply should be connected to the TP27 and the ground should be connected to one of the pins marked as GND in the TP35.

Figure 7. TP27 and TP35 to Connect an External Power Supply

2.3 Modem Basic Settings

The software activates the low power mode by default.

2.3.1 Checking Modem Boot Up and AT Channel

First check that the PMOD is connected to the PC. Open a serial emulator (Windows: Teraterm or PuTTY; Linux/MacOS: screen) and use one window for each UART provided by the PMOD (please refer to the PMOD user manual to perform this step).

Then, apply a 3.8 V DC supply to the RYZ024A module.

Even if the device is GCM powered with an external power supply, please connect the USB cable to your PC to keep the PMOD’s USB chip (Serial to USB converter) at a correct level, allowing the chipset to enter Low Power mode.

Once the external supply is connected, you should see the modem boot messages displayed in the console UART. On the AT UART you should see +SYSSTART printed out.

Then send the following AT commands to check that the modem receives AT commands and enable remote echo. Both commands should return ‘OK’.

- AT
- ATE1

When using in Console mode on UART1 as shown in Figure 8. Modem Bootup Log, please do the following:
 AT+SQNHWCFG="uart1", "enable", "none", "115200", "8", "none", "1", "console"
 AT+SQNHWCFG="uart2", "enable", "rtscts", "921600", "8", "none", "1", "dcp"
 AT+SQNHWCFG="wakeRTS1", "disable"

```

[000000000] boot: Switched to flash, timeout 10000, proto thp
[000000000] Running on Windbond flash sector 0x1C030000
[000000000] RBBombx 11.11052104 '8.0.0.3 [52104]'
[000000004] Reset cause 'BUTTON'(real 'BUTTON' ) (bootWDG : '0') [rawRst '0x0000001']
[000000012] regConfig 0xD88A7A63E1
[000000015] boot: Current flash, timeout 10000, proto thp
[000000020] boot: FFF mode
[000000019] elf: ELF format selected
[000000019] elf: Header finished
[000000019] elf: Waiting for 480 bytes
[000000020] elf: PH 0x00351E20, 28 bytes
[000000020] elf: Note 0x63727A04
[000000020] elf: PH 0x00000000, 20 bytes
[000000021] elf: Note 0x4D415000
[000000021] elf: PH 0x00001000, 86 bytes
[000000021] elf: PH 0x00001060, 1696 bytes
[000000022] elf: PH 0x00001700, 117576 bytes
[000000023] elf: PH 0x0001E248, 8 bytes
[000000023] elf: PH 0x0001E250, 56 bytes
[000000023] elf: PH 0x0001E288, 100 bytes
[000000024] elf: PH 0x0001E2EC, 684 bytes
[000000024] elf: PH 0x0001E598, 2672 bytes
[000000024] elf: PH 0x00354000, 32 bytes
[000000025] elf: PH 0x00710000, 200336 bytes
[000000026] elf: PH 0x00750000, 130728 bytes
[000000026] elf: PH 0x007A0000, 330720 bytes
[000000028] elf: PH 0x00352000, 8192 bytes
[000000028] elf: Program Header finished
[000000028] sbp: no ACPU found
[000000029] sbp: MCPU Booting at 0x1C0E02F0...
user: Loading application
fs: Mounting /flash0...done
fs: Overlay filesystem mounted on /fs

[IDC0] [mem] calibration @0x0038c720
>INFO> DCP : Init over='serial'
eem: Memory initialized
#WARN# ATF : can't find device related to id=4?
[PSP] initializing
fs: Mounting upgrade filesystem ...
fs: Mounting done
QRI pools init...done

```

Figure 8. Modem Bootup Log

2.3.2 Checking Attach

Before starting power measurements, we recommend to first check that the modem can attach to the eNB and that IP connectivity is up with AT+PING.

If you connect to a public network or if you are using an eNodeB simulator that can access the internet, you can use for example AT+PING="www.renesas.com".

In this document, we assume that the SIM is unlocked and SIM PIN is disabled. If not, use AT+CPIN command to enter the PIN code.

The SIM which supports Rel-13 UICC deactivation feature is not required to perform the tests described in this document.

Once the attachment is verified, we recommend disabling the +CEREG URC (Unsolicited Result Code) with AT+CEREG=0, so that unexpected URC will not prevent the platform from entering Sleep or Deep Sleep modes. Doing so is fully acceptable for a test using the PMOD with a laptop as it is difficult to monitor the incoming URC. For the final product, CEREGR URC should not be disabled. These URCs are very useful for the host application to track if there are any network connectivity issues. The RING line will toggle for any incoming URC or data, warning the host application that the UART buffer needs to be flushed so that the modem can go back to sleep.

If you would like to avoid disabling CEREGR URCs and monitor them or any other URCs while performing power consumption measurements, see section 2.3.6.

2.3.3 Checking Signal Conditions

Signal conditions at the UE location can have a significant impact on the performances of the modem regarding the power consumption. In particular, the following values should be checked: RSRP (signal strength), RSRQ (signal quality) and CINR (Carrier to Interference and Noise Ratio).

Before starting power measurement tests, we recommend finding a test spot with a good quality of signal, so that the measurements shown in this user guide could be reproduced.

The following table gives some guidance to estimate the signal condition and should not be taken as an absolute rule.

Signal condition	Signal Strength	Signal quality
Good signal	RSRP > -90 dBm	CINR > 15 dB
Average Signal	-110 dBm < CINR < -90 dBm	0 dB < CINR < 15 dB
Bad Signal	RSRP < -110 dBm	CINR < 0 dB

The following AT commands can be used to monitor the signal level and quality:

- AT+CESQ
- AT+SQNMONI=9

2.3.4 Modem Wake Sources

The modem can be configured with 4 different external wake sources: RTS0, RTS1, Wake0, Wake1, Wake2, Wake3 and Wake4. These wake sources are used to wake the modem up from low power mode. When enabled and active, the wake sources will also prevent the modem from going into low power mode. It is possible to check the current wake source configuration, enable/disable them with AT+SQNHWCFCG command while in manufacturing mode (AT+CFUN=5). See the *Use cases with AT commands* document for further details on the command.

On the RYZ014A PMOD, RTS0 and RTS1 are the default wake sources.

In addition, both UART0 and UART1 are configured in AT mode with flow control enabled (at 115,200 and 921,600 bps respectively). Any pending UART0 or UART1 URC prevents the modem from going into 'deep sleep'. To avoid this, set UART1 in debug (DCP) mode with the following commands, so that no more URC are sent to it. Then use UART0 for controlling the modem via USB-UART bridge.

```
AT+CFUN=5
AT+SQNHWCFCG="uart1","enable","rtscts","921600","8","none","1","dcp"
AT^RESET
```

Note: RTKY024A0B00000BE board has PMOD Interface as UART0 and USB Interface as UART1.

2.3.5 Timers Configuration

The power consumption depends on different timers:

The UART inactivity timer: it controls how long the module should wait, after the reception of the last character by the UART, before entering low power mode. It can be modified with AT+SQNIPSCFG. The power graphs shown in this document were obtained with an inactivity timer lowered to 100 ms with AT+SQNIPSCFG=1,100.

The authorised wake-up latency: the maximum time for the module to resume operational mode when the host MCU needs access to modem services again. A latency shorter than two seconds typically prevents the module from entering deep sleep mode. The default value for the wake-up latency is 5,000 ms and can be changed with the AT+SQNPSCFG command. This timer was left to its default value to record the power graphs of this document.

The ring line duration: the ring line toggles when URC or data are received. The ringing time defaults to five seconds. This value can be decreased using the AT+SQNRICFG command. The modem platform remains active when the ring line is asserted. The same AT command also allows for choosing either URC or data as the only triggering source, or for turning the ring line off altogether. Default settings were not changed to record the power graphs of this document.

2.3.6 Get URCs

The platform does not enter low power if any data or URC are present in the UART buffers. It is therefore important to ensure that no URCs are pending in the modem AT UART buffers.

By default, flow control is activated on the main AT UART. As explained in section 2.3.4, this UART RTS line serves as a wake-up signal. For the modem to sleep, the RTS line thus needs to be inactive. However, since flow control is activated, the modem will then buffer data/URCs and stay in an active standby state until the RTS line is set again. On a production device, the host MCU monitors the RING line and sets RTS accordingly. This behavior is unpractical during testing. A possible workaround consists in disabling flow control support on the modem side using:

```
AT+CFUN=5
AT+SQNHWCFG="uart0","enable","none","115200","8","none","1","at"
AT^RESET
```

After this, the modem does not buffer URCs or data anymore when the RTS line is low. It can thus be used as an ordinary wake source.

In *Teraterm* version 4.94 or later, it is possible to clear/set the RTS line as follows: First create two .ttl files in the *Teraterm* folder:

The first script (`clearrts.ttl`) clears RTS:

```
; change flow control to "none"
setflowctrl 3

; RTS off
setrts 0
```

The second script (`setrts.ttl`) sets RTS:

```
; change flow control to none
setflowctrl 3

; RTS on
setrts 1
```

Then toggle the RTS line by selecting **Control > Macro > clearrts.ttl** or **setrts.ttl**

Note: The RTS line is active low whereas in the above script, setting it high will wake the platform up. The USB chip on the PMOD inverts the RTS signal's polarity.

3. Power Measurement Use Cases

This chapter describes how to conduct tests for evaluating the power consumption of RYZ024A module in different use cases and how to analyze the power graph measurements.

3.1 Boot with CFUN=0

We recommend always starting power consumption measurements with this use case.

- Prerequisite
 - Prepare the setup as described in section 2
- Test procedure:
 - Apply power to the modem
 - Connect to the main AT UART and wait for the +SYSSTART URC to appear on the terminal
 - Connect to the debug console UART
 - Close/Disconnect all Tera term windows beside the console UART or toggle the RTS line of the main AT UART
 - Wait for a few seconds and check that when the modem is in deep sleep mode, the power consumption is around 1 μ A and you should see a log `eem: suspending...` on the console UART .

If you do not see the log, please refer to the troubleshooting section below.

When using in Console mode on UART1 as shown in Figure 9 Power Consumption Log, please do the following:

```
AT+SQNHWCFG="uart1","enable","none","115200","8","none","1","console"
```

```
AT+SQNHWCFG="uart2","enable","rtscts","921600","8","none","1","dcp"
```

```
AT+SQNHWCFG="wakeRTS1","disable"
```

```
File Edit Setup Control Window Help
[FEEDS] : Init enter LWM2M
[FEEDS] : Init leave LWM2M
[FEEDS] : Init enter MQTT
[FEEDS] : Init leave MQTT
[FEEDS] : Init enter SQNSMS
[FEEDS] : Init leave SQNSMS
[FEEDS] : Init enter SUPL
[FEEDS] : Init leave SUPL
[PSP] initialized
[PSP] starting
reserved room 7/150
SLO started
--shell terminal:
-> [ZSP0] started after 2 ms, version 259.7
[ZSP1] started after 1 ms, version 257.6
LPU boot confirmation
[LLP] started
HP: hpStart hpExitFromPsp=0
hp: Started
[FEEDS] : Start enter EAPPS
[FEEDS] : Start leave EAPPS
[FEEDS] : Start enter LWM2M
[FEEDS] : Start leave LWM2M
[FEEDS] : Start enter MQTT
[FEEDS] : Start leave MQTT
[FEEDS] : Start enter SQNSMS
[FEEDS] : Start leave SQNSMS
[FEEDS] : Start enter SUPL
[FEEDS] : Start leave SUPL
[PSP] started
[hwid] Error: No pin for hwid1
eem: Suspending...
```

Figure 9. Power Consumption Log

You should record the following time profile:



Figure 10. Power Graph in CFUN=0 Mode

- The UART inactivity timer is set to five seconds by default. It means that the UE waits five seconds after the *Teraterm* window is closed before going to Sleep or Deep Sleep mode. The delay can be shortened to 100 ms with the `AT+SQNIPSCFG` command (see section 2.3.5.)
- The *Teraterm* window is disconnected after the `+SYSSTART` URC is received
- During the context saving phase, the modem salvages some specific configuration (operator mode, socket) before going to ‘deep sleep’ mode. The context saving phase’s duration depends on the amount of data to be saved. Typically, there’s a small penalty when the modem enters it for the first time after booting.

3.2 PSM Mode

3.2.1 Setting PSM Timers

See the PSM section of the *Use cases with AT command* document for more details.

PSM is disabled by default in the software. It can be activated with `AT+CPSMS`. This command also allows setting PSM timers.

Note that the timers set through `AT+CPSMS` command can get rejected by the network. To verify the final configuration that was accepted by the network, you can activate CEREGR URC with `AT+CEREGR=4` before sending `AT+CFUN=1`.

PSM parameter values are detailed in *3GPP TS 24.008 Table 10.5.163a* and *10.5.172*: T3412-Extended value is transmitted as a string containing an 8-bit binary number: the three upper bits code for the unit, the remaining five for the value

xxx.....	000: Unit is 10 minutes
	001: Unit is 1 hour
	010: Unit is 10 hours
	011: Unit is 2 seconds
	100: Unit is 30 seconds
	101: Unit is 1 minute
	111: Timer disabled
...xxxxx	Timer value, from 0 to 31

T3324 follows the same coding rule than T3412-Extended:

xxx.....	000: Unit is 2 seconds 001: Unit is 1 minute 010: Unit is 6 minutes 111: Timer disabled
...xxxxx	Timer value, from 0 to 31

For instance, to set T3412-Extended to 120 hours and T3324 to two minutes, use:

```
AT+CPSMS=1,,, "01001100" , "00100010"
```

It is strongly recommended to set T3412-Extended to a value greater than the interval between two consecutive wake-ups of the platform by the host application. Efficient power management dictates that a device in PSM should not wake up to perform TAU, as much as possible.

3.2.2 Test Procedure with UDP Traffic

During this test, the UE will send a 1500 bytes UDP packet before entering PSM idle mode. You can replace the UDP packet sending by a simple ping with `AT+PING="www.renesas.com"` command.

- Prerequisite
 1. A setup prepared as described in section 2.;
 2. A network supporting the PSM feature;
 3. An access to a UDP server to check that packets are correctly received.
- Instructions:
 1. Apply power to the modem;
 2. Connect to the main AT UART and wait for the `+SYSSTART` URC to appear on the terminal;
 3. Disable eDRX with `AT+SQNEDRX=0`;
 4. Activate PSM with `AT+CPSMS=1,,, "10000110" , "00001000"`;
T3324: 16 s, T3412-Extended: 3 min;
T3412 is set to a small value to facilitate testing.
 5. `AT+CEREG=4`;
 6. `AT+CFUN=1`;
 7. Check that you receive the `+CEREGURC` and that the timer settings are as expected:
`+CEREG: 1, "0002" , "01A2D004" , 7,,, "00001000" , "10000110"`
 8. Configure the UDP socket and send a 1,500-byte UL packet:
Refer to the *Use cases for AT commands* document for more details on how to send the packet.
Below is an example:

```
AT+SQNSCFG=1,1,0,90,600,50
```

```
AT+SQNSCFGEXT=1,0,0,0
```

```
AT+SQNSD=1,1,12345, "192.168.10.173" ,0,8000,1
```

```
AT+SQNSSENDEXT=1,1500
```

- Send 1,500 bytes to the server;
- After the command, the modem sends a ">". Enter the data to be sent;
- The AT command loops until all data has been received.

```
AT+SQNSH=1
```

9. Close/Disconnect all *Teraterm* windows other than the console UART or toggle the RTS line of the main AT UART;
10. Wait a few minutes and check that the modem has entered low power mode. Power consumption should drop to around 1 μ A. You should see a *"eem: Suspending..."* line in the console UART. If not, please refer to the troubleshooting section.
11. Open the main AT UART again, or toggle the RTS line of the main AT UART, and send another UDP packet with:


```
AT+SQNSD=1,1,12345,"192.168.10.173",0,8000,1
```

 - Send a 1,500-byte packet to the server

```
AT+SQNSH=1
```

 - No need to configure the socket again there
12. Repeat from step 9.
You should record the power graph shown on the following page.

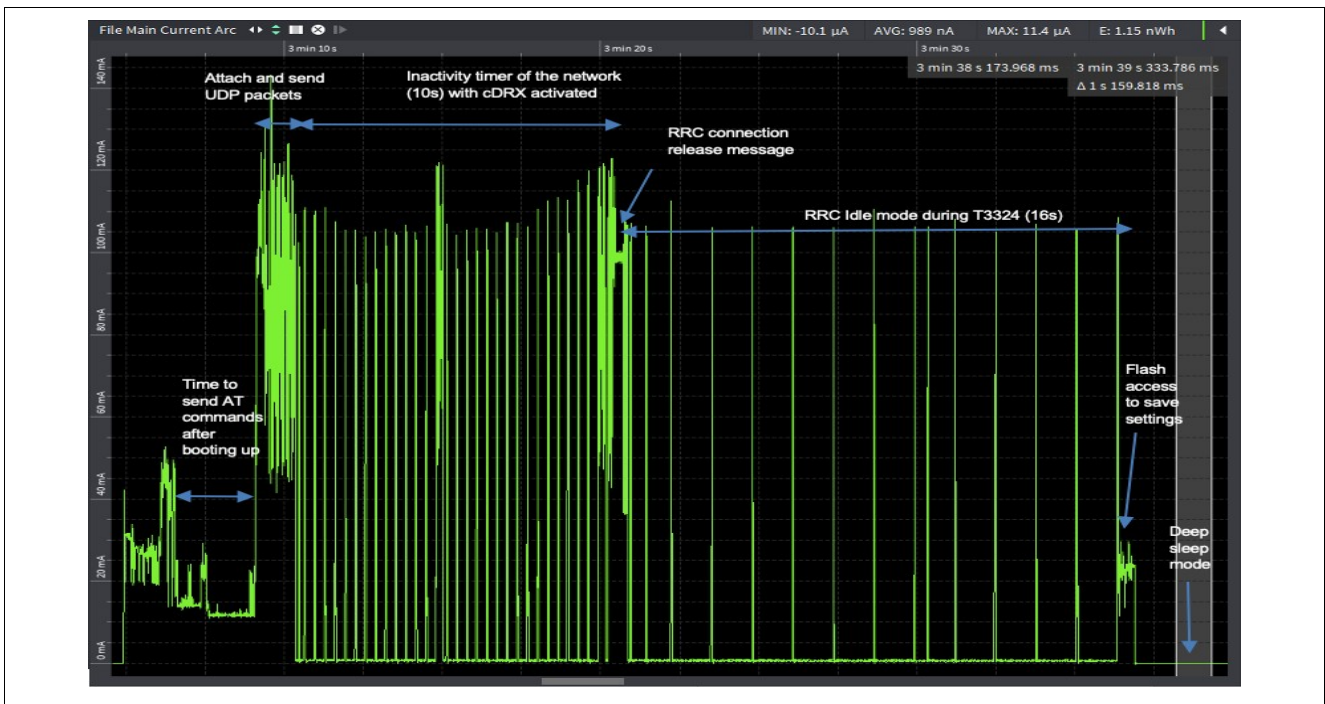


Figure 11. UDP Traffic Power Graph

In this example:

- The inactivity timer was set to 10 seconds on the network side;
- cDRX is supported by the network.

When cDRX is not supported by the network, the UE draws an average of 85 mA (at 3.8 V) until the inactivity timer runs out. The overall power consumption thus strongly depends on the inactivity period set by the network.

3.2.3 Tracking Area Update

In PSM Idle mode, the UE only wakes up on a GPIO toggle or for a tracking area update (TAU). The TAU settings (T3412-Extended) should be set to avoid the latter case. In the procedure detailed in section 4.3.2., T3412-Extended is set to three minutes for sole testing purposes.

The following graph corresponds to the power consumption during TAU:

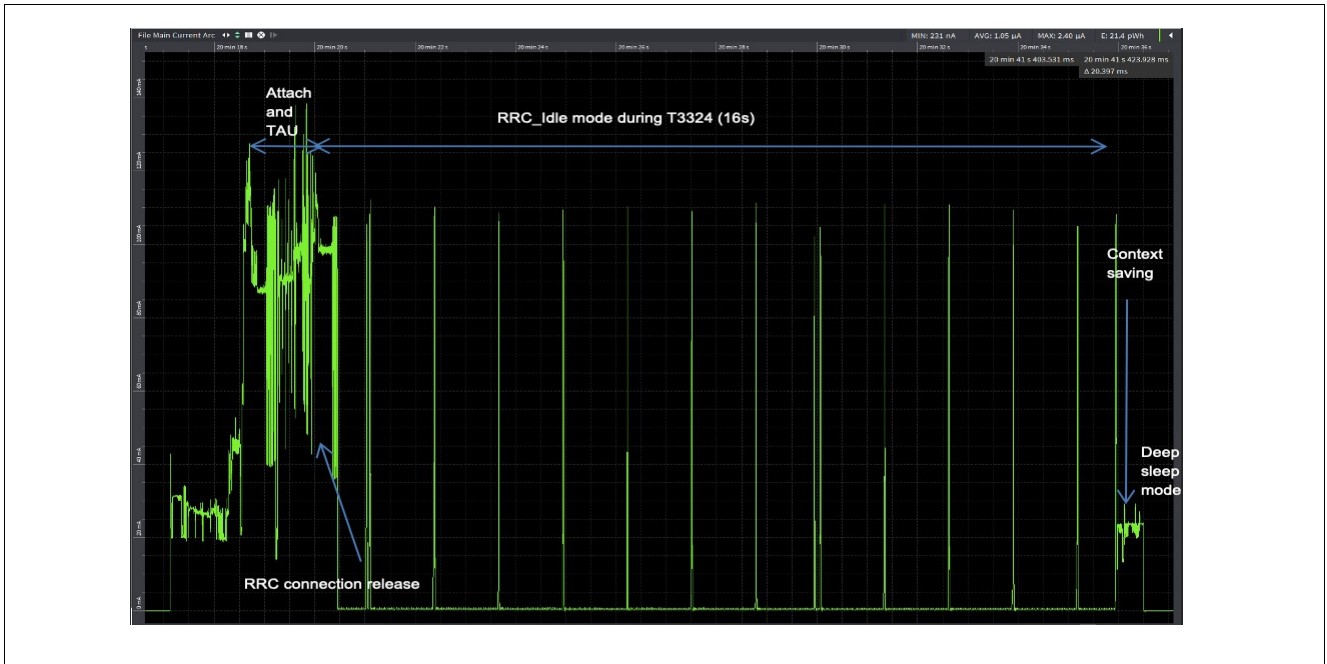


Figure 12. Tracking Area Update

3.2.4 PSM and TCP Traffic

In the following example the modem sends 1 kB TCP packets every seventy seconds. At each transmission slot, the modem boots up, sends the packet, waits for the RRC connection release message from the network (in this example the inactivity timer is set to ten seconds). It then remains in IDLE mode, monitoring paging opportunities as long as T3324 doesn't run out, then finally enters 'deep sleep' mode until the next TCP packet has to be sent.

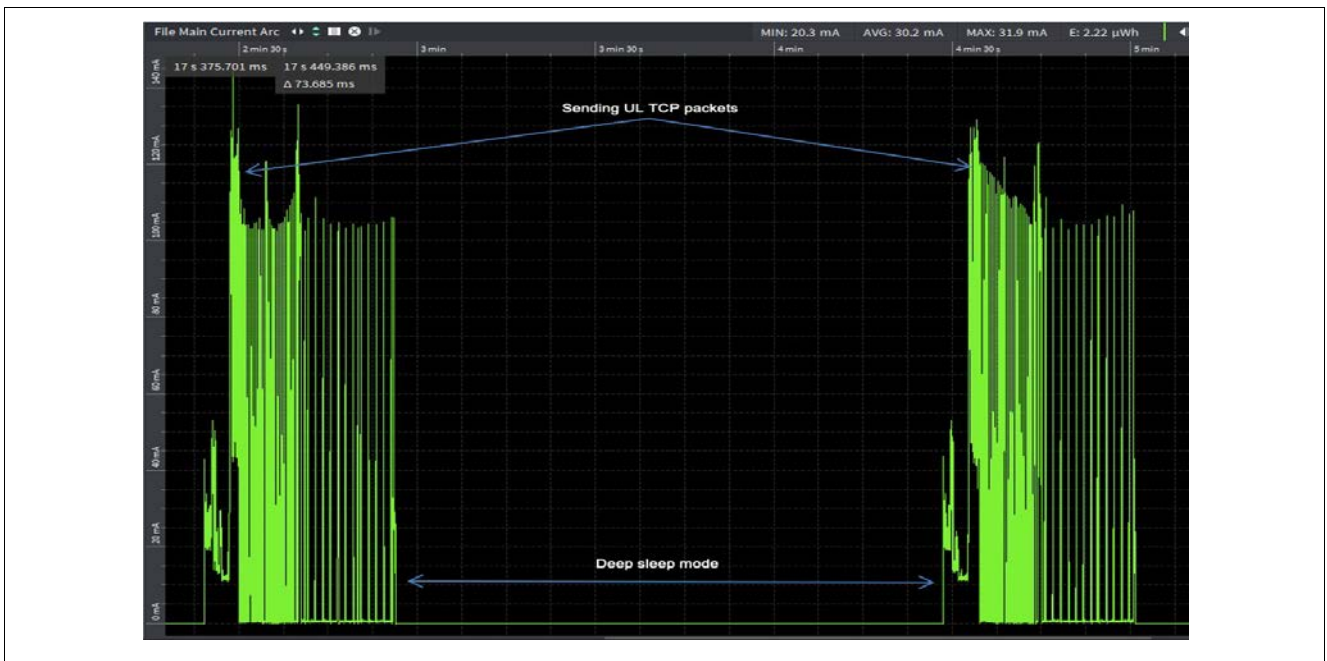


Figure 13. PSM and TCP Traffic

3.3 eDRX Mode

This chapter describes how to measure the power consumption in eDRX mode.

3.3.1 Setting eDRX Parameters

Please refer to the PSM section of the *Use cases for AT commands* document for more details.

eDRX is disabled by default. It can be activated with the `AT+SQNEDRX` command. This command can also set the eDRX cycle period and the paging window length.

The parameters set with the `AT+SQNEDRX` command can be rejected by the network. To check the settings negotiated with the network, you can activate the `+CEDRXP` URC by setting the mode parameter of `AT+SQNEDRX` to 2 before sending `AT+CFUN=1`.

eDRX parameters values are given in *3GPP TS 24.008 Table 10.5.5.32*:

bit	E-UTRAN eDRX cycle length duration	bit	Paging Time Window length
4 3 2 1		8 7 6 5	
0 0 0 0	5,12 seconds (NOTE 4)	0 0 0 0	1,28 seconds
0 0 0 1	10,24 seconds (NOTE 4)	0 0 0 1	2,56 seconds
0 0 1 0	20,48 seconds	0 0 1 0	3,84 seconds
0 0 1 1	40,96 seconds	0 0 1 1	5,12 seconds
0 1 0 0	61,44 seconds (NOTE 5)	0 1 0 0	6,4 seconds
0 1 0 1	81,92 seconds	0 1 0 1	7,68 seconds
0 1 1 0	102,4 seconds (NOTE 5)	0 1 1 0	8,96 seconds
0 1 1 1	122,88 seconds (NOTE 5)	0 1 1 1	10,24 seconds
1 0 0 0	143,36 seconds (NOTE 5)	1 0 0 0	11,52 seconds
1 0 0 1	163,84 seconds	1 0 0 1	12,8 seconds
1 0 1 0	327,68 seconds	1 0 1 0	14,08 seconds
1 0 1 1	655,36 seconds	1 0 1 1	15,36 seconds
1 1 0 0	1310,72 seconds	1 1 0 0	16,64 seconds
1 1 0 1	2621,44 seconds	1 1 0 1	17,92 seconds
		1 1 1 0	19,20 seconds
		1 1 1 1	20,48 seconds

3.3.2 Test Procedure

- Prerequisites:

1. A setup prepared as described in section 2
2. A network supporting eDRX feature
3. A good RF signal strength (refer to section 2.3.3.)
4. An eDRX cycle set to the proper value (refer to chapter 3.3.1.) and PSM mode disabled.

Note: If the RF field strength is low, the modem performs RSRP measurements of the neighboring cells, which increases power consumption. In such conditions, you can check section 3.4. on relax monitoring to limit the number of measurements.

- Instructions:

1. Apply power to the modem
2. Connect to the main AT UART and wait for the `+SYSSTART` URC to appear on the terminal
3. Disable PSM with `AT+CPSMS=0`
4. Activate eDRX using your test parameters:
`AT+SQNEDRX=2,4,"0101","0000"` (eDRX cycle length is 81.92 s, PTW is 1.28 s);
5. Enable the `+CEREG` URC: `AT+CEREG=2`
6. Attach to the network: `AT+CFUN=1`
7. Wait for `+CEDRXP` and `+CEREG` URCS if enabled
8. Disable all UARTs apart from the debug console UART, or toggle the RTS line of the main AT UART
9. Wait a few seconds and check that the modem has entered deep sleep mode. The power consumption should drop to around 1 μ A. You should see the message "eem: Suspending..." on the console UART. If not, please refer to the troubleshooting section.

Note that for eDRX cycles shorter than 20.48 s, the ecoPaging feature won't be activated and the "eem: Suspending..." message won't show up on the console UART.

10. Wait for the next eDRX cycle and watch the debug console UART:

- If you get a "Booting ecopaging" message, the modem has performed one cycle in eco-Paging mode and the average power should be close to the expected target value;
- If you get a block of several lines starting with "boot" and ending with "eem: Suspending", the modem has performed extra tasks besides monitoring paging messages, for example a neighbour scan (triggered by a drop in RSRP value) or a cell reselection;
- During eDRX sleep, the modem remains in 'deep sleep' mode (1 μ A).

You should get the following power consumption profile:

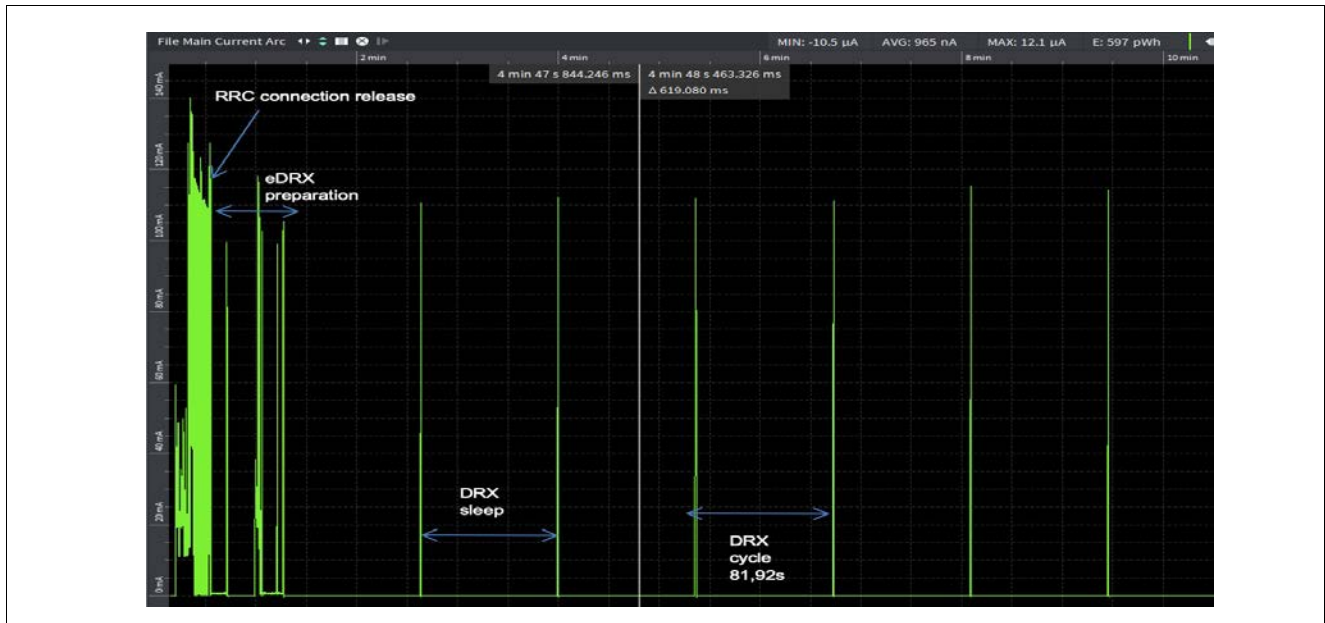


Figure 14. Power Graph in eDRX Mode

During the eDRX preparation phase, the UE will wake up now and then.

Power consumption measurement must begin after the first five DRX cycles and averaged over ten cycles, as the UE ends the eDRX preparation phase during the first five DRX cycles.

The graph below zooms on a paging opportunity during eDRX with eco-Paging feature:



Figure 15. Paging Opportunity during eDRX with Eco-Paging Feature

3.3.3 Tracking Area Update

While in eDRX, the UE must still perform TAU. The network sets the interval between two TAUs using T3412 Extended. In eDRX mode, unlike in PSM mode, the UE cannot request a specific timer.



Figure 16. Tracking Area Update

3.3.4 SMS Reception

The network informs the UE of a pending SMS at every paging occasion. After receiving the paging notification, the UE boots up, attaches to the network and decodes the SMS payload. It then remains attached to the network for the duration of the inactivity timer (10 s in the graph below) until the network

sends the RRC connection release message. Thereafter the modem enters eDRX IDLE as soon as the eDRX preparation phase is over, as explained in the previous eDRX examples.

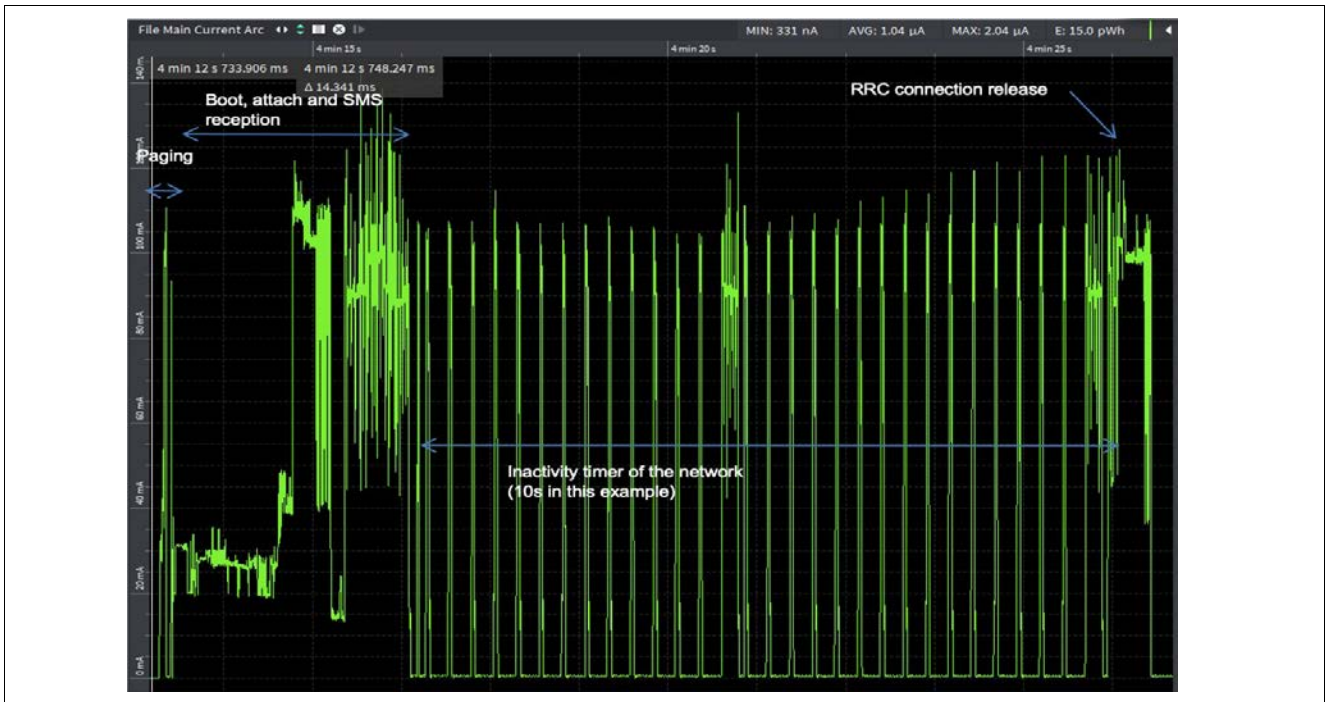


Figure 17. SMS Reception

3.3.5 eDRX and TCP Traffic

In the following example, some TCP traffic is initiated while the UE is in eDRX mode. UL TCP packets of 1 KB are sent every 180 seconds. The DRX cycle is unchanged (81,92s) as well as the PTW (1,28s).

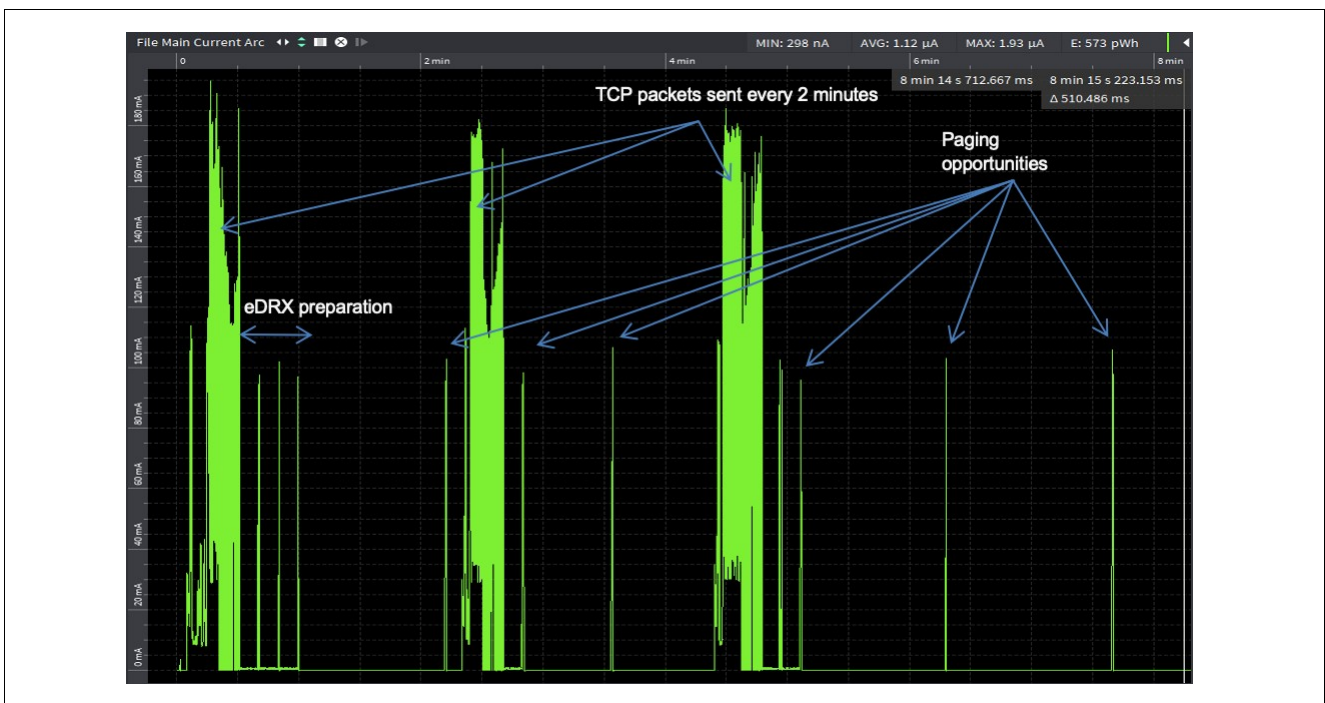


Figure 18. eDRX and TCP Traffic

3.4 Relaxed Monitoring

All power consumption figures, for eDRx mode, shared in this document or in Renesas' software release notes are measured in good radio conditions without any cell reselections.

If relaxed monitoring is not supported by the network, it is possible to totally deactivate the neighbor scanning and therefore change cells only when the current cell is lost, by applying the following parameters to the `AT+SQNRMON` command:

- `<rsrp_hyst>`: 20 dB
- `<cinr_thold>`: -9 dB
- `<resel_before_tx_timer>`: 8290 ms

4. Troubleshooting Check List

The modem cannot enter Deep Sleep mode if:

- RTS0 line is asserted:
- UART0 should be disconnected (*Teraterm* window closed/disconnected) to allow the platform to enter Deep Sleep mode
- Ensure that only the debug console UART is connected when performing power consumption measurements.
- There is data stuck in the UART buffer
 - Make sure to disconnect the UART0 only after receiving the `+CEREG` URC
 - You can disable `+CEREG` URC with `AT+CEREG=0`
- SIM is waiting for a PIN code:
 - Make sure that `AT+CPIN` returns `READY` after `AT+CFUN=1`

The UART inactivity timer is set to five seconds by default. It means that the UE will wait five seconds after the *Teraterm* window is disconnected before going to Sleep or Deep Sleep mode. This delay can be shortened down to 100 ms with the `AT+SQNIPSCFG` command.

When attached to the network, the power consumption depends on the inactivity timer and the cDRX configuration of the network. The UE cannot set any of these and simply adopts the network's configuration.

According to the RSRP level at test location, the UE may perform cell reselection or may have to monitor the RSRP level of adjacent cells, which increases the power consumption. Ensure a good RSRP level to reproduce the power consumption figures published in this document.

Although it is possible to enable both PSM and eDRX, disable PSM while testing eDRX and vice-versa to reproduce the power consumption figures given in the software release note.

In eDRX, the UE cannot set the T3412 Extended timer and is required to perform TAU procedures regularly. If T3412 value set by the network is low, the eDRX power consumption increases drastically.

The 'EcoPaging' feature is activated for eDRX cycles longer than 20.48 s. For shorter eDRX cycles, the modem chooses Sleepmode (around 300 μ A) between paging opportunities, instead of Deep Sleep mode.

5. Abbreviations

AT command	Modem-type (Hayes) commands prefixed with AT characters.
LTE-M	LTE Category M
CINR	Carrier to Interference and Noise Ratio
eDRX	Extended Discontinuous Reception
eco-Paging™	Proprietary Renesas’ algorithm for optimized eDRX power consumption
EVK	Evaluation Kit
FW	Firmware
RYZ014	Renesas Cat M module platform name
NW	Network
PSM	Power Saving Mode
PTW	Paging Time Window
RSRP	Reference Signal Receive Power
RF	Radio Frequency
SMA	Type of RF connector
SIM	Subscriber Identity Module
Tera term	A free terminal emulator software running on Windows PC and used to control the modem through AT commands
µA	Micro Ampere
UE	User Equipment
URC	Unsolicited Result Code

6. Appendix A – Power Monitor Tools

- OTII Power Monitor from Qoitech (<https://www.qoitech.com>)
It can provide power and display power measurement on a graph with an accuracy of 1 µA.



- Keithley 2701 precision multimeter
It can be used in combination with a power monitor like the one from Monsoon for measuring very low current, around 1 µA, accurately when the UE is in Deep Sleep mode.



- Keysight N6705B Power Analyzer
This is a lab power supply than can be used with separate Analyzer software on a PC. It can provide good accuracy for measuring current as low as 1 µA.



Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.10.22	-	Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
 4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
 5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
 6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
- Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
 8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
 9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
 11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
 12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
 13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.