PMIC Solution for RZ/G3E SMARC

Power Tree

This document describes the register settings of the RAA215300, SLG7RN47061 and SLG7RN47054 for supplying power for the RZ/G3E SMARC board.

The RAA215300 is a high-performance, low-cost 9-channel PMIC designed for 32-bit and 64-bit MCU and MPU applications. It supports DDR3, DDR3L, DDR4, and LPDDR4 memory power interfaces. The internally compensated regulators, built-in Real-Time Clock (RTC), 32kHz crystal oscillator, and coin cell battery charger provide a highly integrated, small footprint power solution ideal for System-On-Module (SOM) applications.

The SLG7RN47061 is a low power and small form device. The SoC is housed in a 3mm×3mm MSTQFN package which is optimal for using with small devices.

The SLG7RN47054 is a low power and small form device. The SoC is housed in a 2mm×3mm STQFN package which is optimal for using with small devices.

Target Device

- RZ/G3E

Contents

1. Terms and Definitions

- ABS – Audio Band Suppression
- DVS – Dynamic Voltage Scaling
- LDO – Low drop out linear regulator
- SR – Slew Rate
- QFN – Quad flat-pack no-lead (package)

2. References

- RAA215300 - High Performance 9-Channel PMIC Supporting DDR Memory, with Built-In Charger and RTC | Renesas
- SLG46585 - GreenPAK™ Programmable Mixed-Signal Matrix with Asynchronous State Machine, LDOs, and DC/DC Converter | Renesas
- SLG46537 - GreenPAK™ Programmable Mixed-signal Matrix with Asynchronous State Machine | Renesas

3. Power Tree Diagram

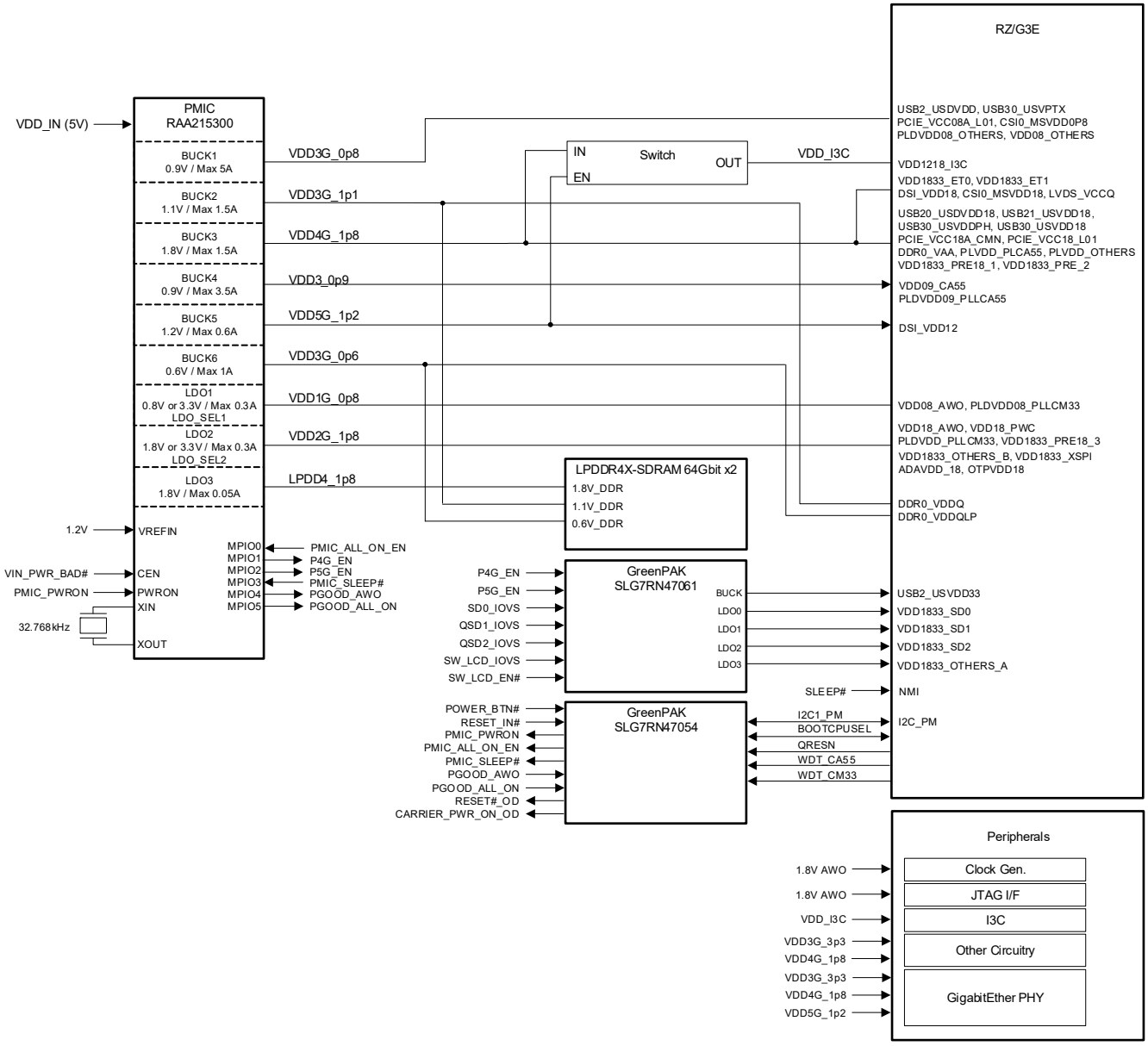
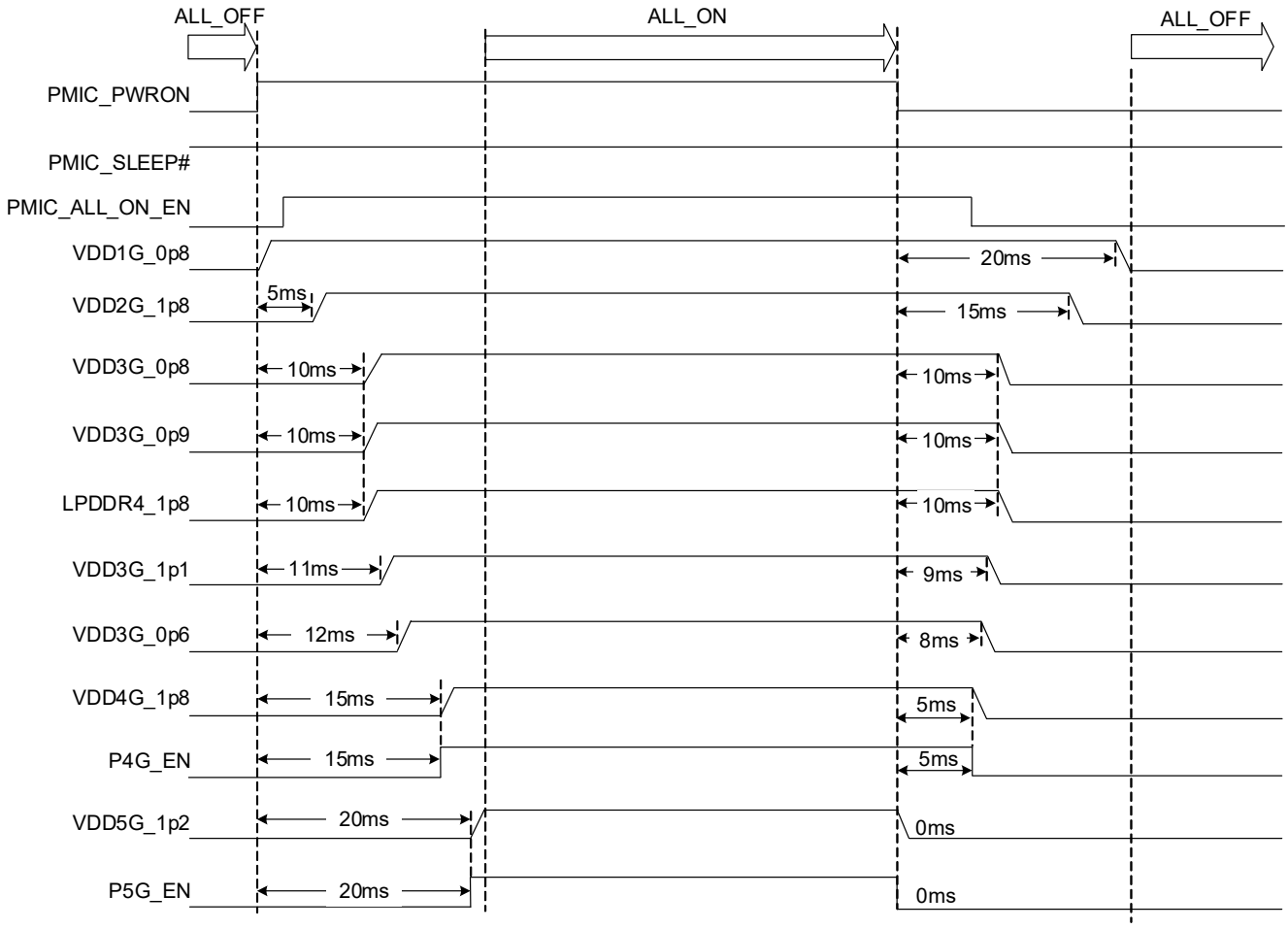


Figure 1. RAA215300, SLG7RN47061, SLG7RN47054 – RZ/G3E Power Tree

4. Power Requirements

All rails are sequenced from the PMIC_PWRON signal.



Power-on sequence paused if PMIC_ALL_ON_EN assertion > 7ms from PMIC_PWRON

Power-off sequence paused if PMIC_ALL_ON_EN deassertion > 13ms from PMIC_PWRON

Figure 2. CA55 Power-On/Off Sequence

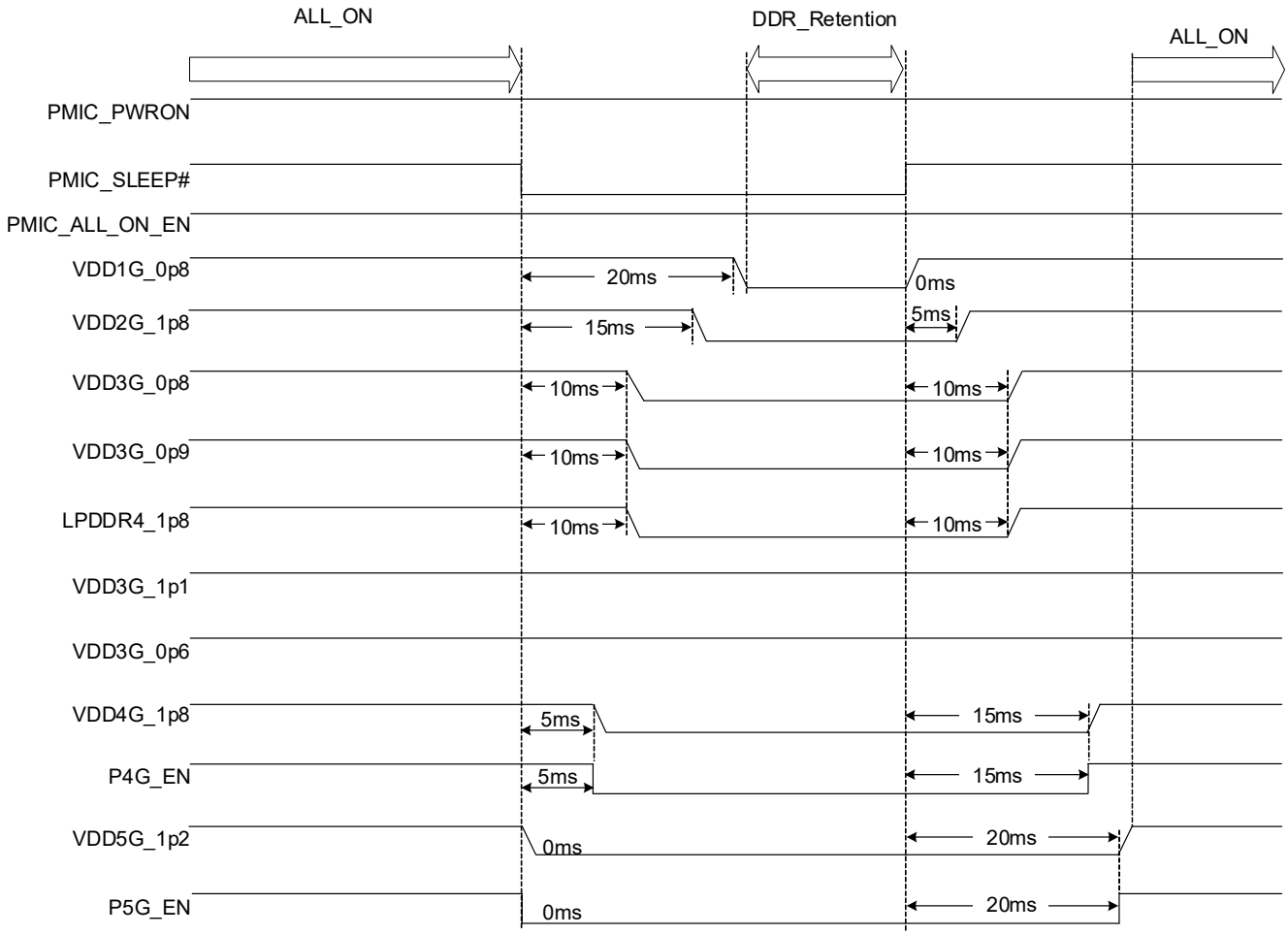


Figure 3. DDR Retention

5. Variant Table and Ordering Information

Table 1. Variant Table

Part Number	Package	Size	Shipment Form	Pack Quantity
RAA215300A2GNP#HA8	56 Lead, 8.8mm QFN	5×5 mm Exposed Paddle	Tape & Reel	1000
SLG7RN47061	29-Pin MSTQFN	3×3×0.55 mm	-	-
SLG7RN47054	20-pin STQFN	2×3 mm	-	-

6. Detailed Description

Table 2. Register Settings RAA215300A2GNP#HA8

Register Address	Function	Default Value	Description
0x1E	Main Slave Address	0x00	Main Slave Address = 0x12
0x1F	RTC Slave Address	0x00	RTC Slave Address
0x20	Buck1 Enable	0x05	BK1 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled

Table 2. Register Settings RAA215300A2GNP#HA8 (Cont.)

Register Address	Function	Default Value	Description
0x21	Buck1 ACTIVE	0x00	Buck1 Output in Active state = 0.8V (Auto)
0x22	Buck1 SLEEP	0x00	Buck1 Output in Sleep state = 0.8V (Disabled)
0x23	Buck1 Power On	0x0A	Buck1 Power-on Delay = 10ms
0x24	Buck1 Power Off	0x0A	Buck1 Power-off Delay = 10ms
0x25	Buck1 SR	0xAA	Buck1 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x26	Buck1 Config	0x0B	Buck1 Switching frequency = 0.833MHz Output discharge = Fast
0x27	Buck2 Enable	0x07	Buck2 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x28	Buck2 ACTIVE	0x00	Buck2 Output in Active state = 1.1V (Auto)
0x29	Buck2 SLEEP	0x00	Buck2 Output in Sleep state = 1.1V (Auto)
0x2A	Buck2 Power On	0x0B	Buck2 Power-on Delay = 11ms
0x2B	Buck2 Power Off	0x09	Buck2 Power-off Delay = 9ms
0x2C	Buck2 SR	0xAA	Buck2 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x2D	Buck2 Config	0x07	Buck2 Switching Frequency = 0.769MHz Output discharge = Fast
0x2E	Buck3 Enable	0x05	Buck3 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x2F	Buck3 ACTIVE	0x00	Buck3 Output in Active state = 1.8V (Auto)
0x30	Buck3 SLEEP	0x00	Buck3 Output in Sleep state = 1.8V (Disabled)
0x31	Buck3 Power On	0x0F	Buck3 Power-on Delay = 15ms
0x32	Buck3 Power Off	0x05	Buck3 Power-off time = 5ms
0x33	Buck3 SR	0xAA	Buck3 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x34	Buck3 Config	0x1B	Buck3 Switching Frequency = 1.54MHz Output discharge = Fast
0x35	Buck4 Enable	0x05	Buck4 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x36	Buck4 ACTIVE	0x02	Buck4 Output in Active state = 0.9V
0x37	Buck4 SLEEP	0x02	Buck4 Output in Sleep state = 0.9V (Disabled)
0x38	Buck4 Power On	0x0A	Power-On delay = 10ms
0x39	Buck4 Power Off	0x0A	Power-Off delay = 10ms
0x3A	Buck4 SR	0xAA	Buck4 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x3B	Buck4 Config	0x07	Switching Frequency = 0.769MHz Output discharge = Fast

Table 2. Register Settings RAA215300A2GNP#HA8 (Cont.)

Register Address	Function	Default Value	Description
0x3C	Buck5 Enable	0x05	Buck5 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x3D	Buck5 ACTIVE	0x00	Buck4 Output in Active state = 1.2V
0x3E	Buck5 SLEEP	0x00	Buck4 Output in Sleep state = 1.2V (Disabled)
0x3F	Buck5 Power On	0x14	Power-On delay = 20ms
0x40	Buck5 Power Off	0x00	Power-Off delay = 0
0x41	Buck5 SR	0xAA	Buck5 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x42	Buck5 Config	0x1B	Switching Frequency = 1.54MHz Output discharge = Fast
0x43	Buck6 Enable	0x07	Buck6 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x44	Buck6 ACTIVE	0x57	Buck6 Output set to 1.8V in Active state, but VTTREF is enabled so output = VREFIN/2 FPWM Independent soft-start, not linked to buck2
0x45	Buck6 SLEEP	0x91	Buck6 Output set to 1.8V in Sleep state, but VTTREF is enabled so output = VREFIN/2 FPWM Independent soft-start, not linked to buck2 Medium pull-down resistor on VTTREF
0x46	Buck6 Power On	0x0C	Power-On delay = 12ms
0x47	Buck6 Power Off	0x08	Power-Off delay = 8ms
0x48	Buck6 SR	0xAA	Buck6 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x49	Buck6 Config	0x03	Switching Frequency = 1.54MHz Output discharge = Fast
0x4A	LDO1 ACTIVE	0x40	LDO1 Enabled in Active state Active 0 setting = 0.8V Active 1 setting = 0.8V Bypass operation disabled
0x4B	LDO1 SLEEP	0x00	LDO1 disabled in Sleep state
0x4C	LDO1 Power On	0x00	LDO1 Power-on delay = 0
0x4D	LDO1 Power Off	0x14	LDO1 Power-off delay = 20ms
0x4E	LDO1 SR	0xAA	LDO1 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x4F	LDO2 ACTIVE	0x64	LDO2 Enabled in Active state Active 0 setting = 1.8V Active 1 setting = 1.8V Bypass operation disabled
0x50	LDO2 SLEEP	0x04	Sleep setting = 1.8V
0x51	LDO2 Power On	0x05	LDO2 Power-on delay = 5ms

Table 2. Register Settings RAA215300A2GNP#HA8 (Cont.)

Register Address	Function	Default Value	Description
0x52	LDO2 Power Off	0x0F	LDO2 Power-off delay = 15ms
0x53	LDO2 SR	0xAA	LDO2 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x54	LDO3 ACTIVE SLEEP	0xE4	LDO3 Enabled in Active and Sleep states Active setting = 1.8V Sleep setting = 1.8V
0x55	LDO3 Power On	0x0A	LDO3 Power-on delay = 10ms
0x56	LDO3 Power Off	0x0A	LDO3 Power-off delay = 10ms
0x57	LDO3 SR	0xAA	LDO3 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/µs
0x58	LDOs Config	0x3F	LDO1, LDO2, LDO3 discharge = Fast
0x64	nINT Mask 1	0x00	Undervoltage fault on each buck regulator is not masked from INT#.
0x65	nINT Mask 2	0x00	VIO PGOOD fault is not masked from INT#. Undervoltage fault on each LDO is not masked from INT#.
0x66	nINT Mask 3	0x00	Overvoltage fault on each buck regulator is not masked from INT#.
0x67	nINT Mask 4	0x00	Buck1 high current fault is not masked from INT#.
0x68	nINT Mask 6	0x00	The following faults are not masked from INT#. PGOODCCBAT. VREFIN UVLO. AVDD UVPD. NVM. CRST Triggered. WDT Error. Over temperature warning.
0x69	Fault Config 1	0x3F	Shut down all regulators if any buck regulator is under voltage.
0x6A	Fault Config 2	0x07	Shut down all regulators if any LDO is under voltage.
0x6B	Fault Config 3	0x7F	Shut down all regulators if VREFIN is under voltage. Shut down all regulators if any buck regulator is over voltage.
0x6C	Block EN	0x00	VBAT comparator enabled. Watchdog timer enabled. Power down when watchdog timer expires. Reset when watchdog timer expires. Power down when CRST_IN# is asserted.
0x6F	Config 1	0x9A	Battery charge current = 60µA. Temperature warning = 105°C. Buck1 high current warning = 6A. AVDD UVPD threshold = 2.7V. PWRON = on/off switch.
0x70	Config 2	0xF8	VCCBAT = 3.3V.
0x71	Config 3	0x17	VIO Timeout = 1ms. Cold reset delay = 255ms.

Table 2. Register Settings RAA215300A2GNP#HA8 (Cont.)

Register Address	Function	Default Value	Description
0x72	MPIO0 Power On	0x07	MPIO0 Power-on Delay = 7ms
0x73	MPIO0 Power Off	0x0D	MPIO0 Power-off Delay = 13ms
0x74	MPIO1 Power On	0x0F	MPIO1 Power-on Delay = 15ms
0x75	MPIO1 Power Off	0x05	MPIO1 Power-off Delay = 5ms
0x76	MPIO2 Power On	0x14	MPIO2 Power-on Delay = 20ms
0x77	MPIO2 Power Off	0x00	MPIO2 Power-off Delay = 0
0x78	MPIO3 Power On	0x00	MPIO3 Power-on Delay = 0
0x79	MPIO3 Power Off	0x00	MPIO3 Power-off Delay = 0
0x7A	MPIO4 Power On	0x07	MPIO4: LDO2 PGOOD output
0x7B	MPIO4 Power Off	0x00	Redundant
0x7C	MPIO5 Power On	0x0A	MPIO5: AND of all regulators PGOOD output
0x7D	MPIO5 Power Off	0x00	Redundant
0x80	MPIO Assertion	0x3F	A reset output will be asserted in Sleep state.
0x89	Shutdown Config	0x02	Shut down all regulators, applying discharge resistors and respective shutdown time settings
0x8A	MPIO0 Config	0x22	External VR PGOOD input, Active High
0x8B	MPIO1 Config	0x3E	External VR EN output, Full CMOS
0x8C	MPIO2 Config	0x3E	External VR EN output, Full CMOS
0x8D	MPIO3 Config	0x01	SLEEP# input, Active Low
0x8E	MPIO4 Config	0x3C	PGOOD output, Full CMOS
0x8F	MPIO5 Config	0x3C	PGOOD output, Full CMOS
0x90	PWRON Polarity Config	0x01	Active High

Table 3. Register Settings for SLG7RN47061

Register Address	Function	Default Value	Description
0x28	Chip address	0101000	-

Table 4. Register Settings for SLG7RN47054

Register Address	Function	Default Value	Description
0x38	Chip address	0111000	-

7. Revision History

Revision	Date	Description
1.00	Jul 2, 2024	Initial release.

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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